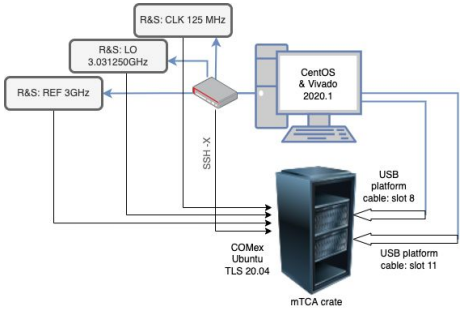
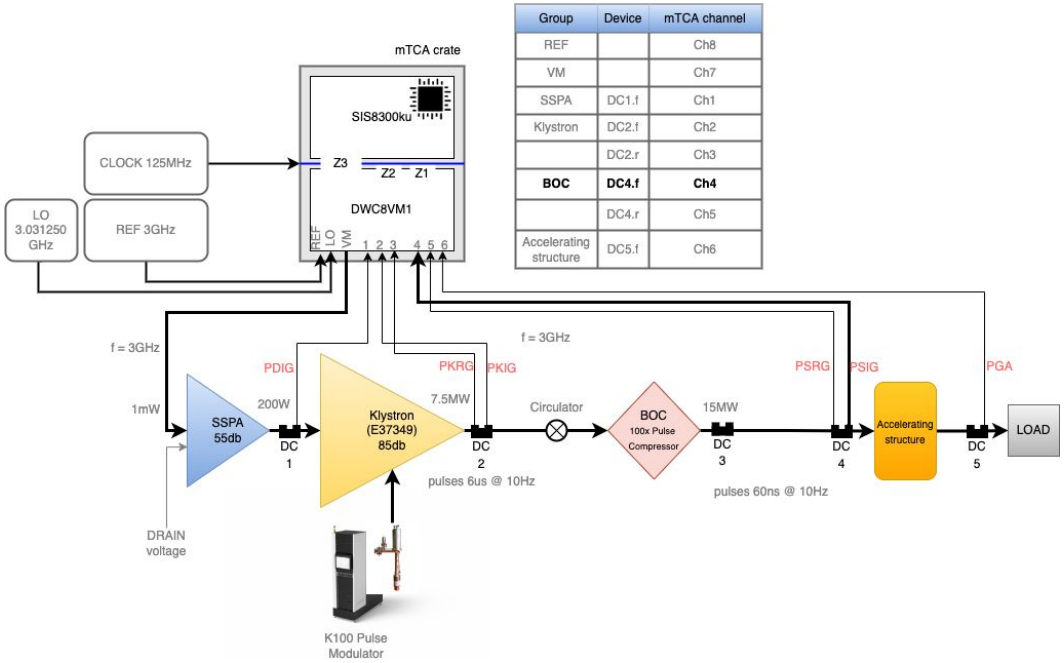
LLRF (Phase I, 33-50%).

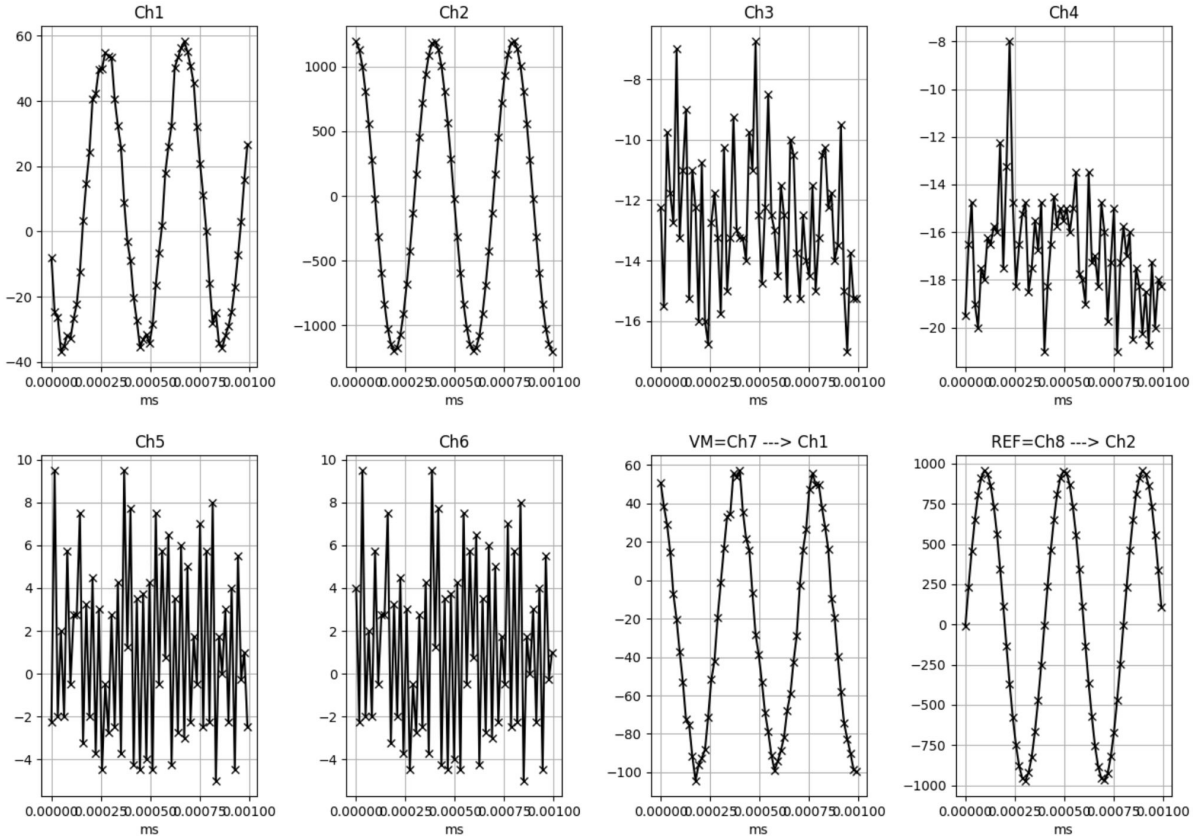
1. Basic LLRF implementation based on DESY tools (2015..).
2. Version 0.1 of manual.
3. I/Q sampling is core (2 sample reconstruction).
4. Clocking and timing.
5. DESY-RDL (for Memmap).



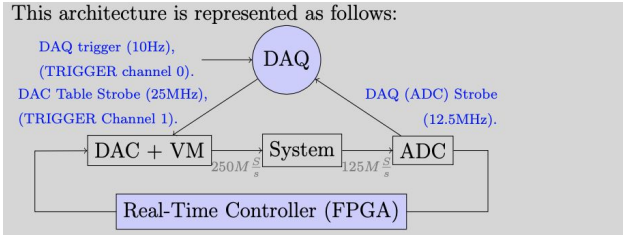


Group	Device	mTCA channel
REF		Ch8
VM		Ch7
SSPA	DC1.f	Ch1
Klystron	DC2.f	Ch2
	DC2.r	Ch3
BOC	**DC4.f**	**Ch4**
	DC4.r	Ch5
Accelerating structure	DC5.f	Ch6

Example: ADC → DAQ → DDR4 → PCIe → COMex



- Clock: 125MHz.
- IF: 5MHz.
- DAQ strobe divider: 1.
- Last 32 samples (*continuous mode*) of 8 channels.
- Delay of cable: ok.
- Noise floor: ok.
- Scale glitch: ?? (Ch7 → Ch1).



Questions:

1. LLRF-trigger + warning (‘*A pulse is coming*’): how?
2. FB control: for SISO (PID) which signals to use, or SIMO?
3. How long is the filling time (0.5 us)?
4. How many samples in DAC table for FF control (1024)?
5. When to phase-reverse for BOC pulse?
6. Which device has saturation effects (need for anti-windup filter)?
7. List of perturbations:
    a. Repetitive: feedforward or pulse-to-pulse.
    b. Non-repetitive: feedback and disturbance rejection.