UNIVERSITÉ DE GENÈVE
FACULTÉ DES SCIENCES
Département de physique nucléaire et corpusculaire

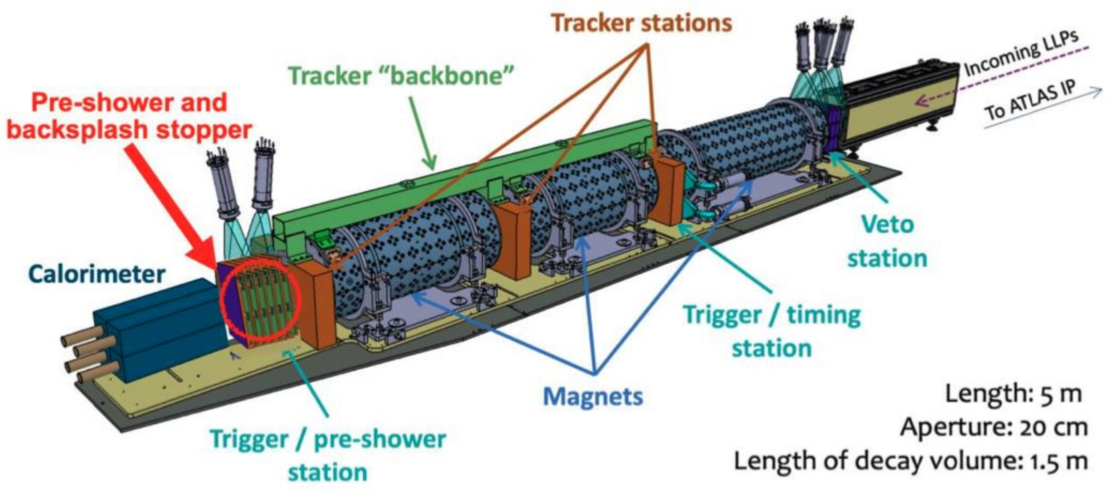
FASER

An Upgraded Preshower Detector for the FASER Experiment at the LHC

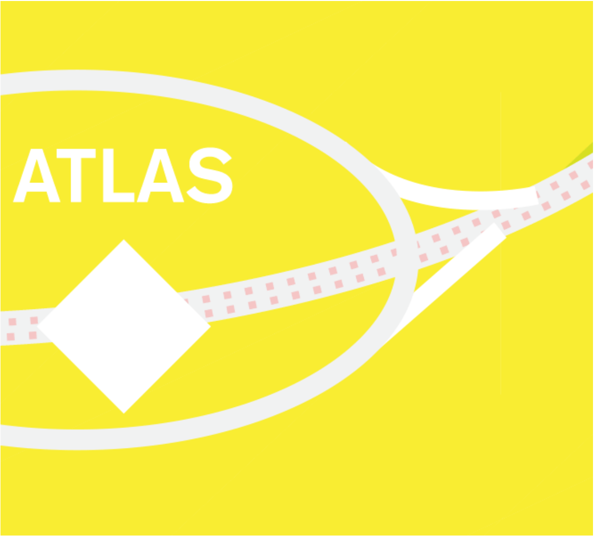
CHIARA MAGLIOCCA

CHIPP Winter School 2023| Leukerbad, January 2023

The FASER Experiment at LHC



- **F**orw**A**rd **S**earch **E**xpe**R**iment
- Designed to search for **light and weakly-interacting particles**



Picture taken from symmetry magazine. Artwork by Sandbox Studio, Chicago with Ana Kova.

- Fluxes of high-energy SM particles are supressed
- Muons and neutrinos only exception

Zero degrees angle → huge LLPs flux

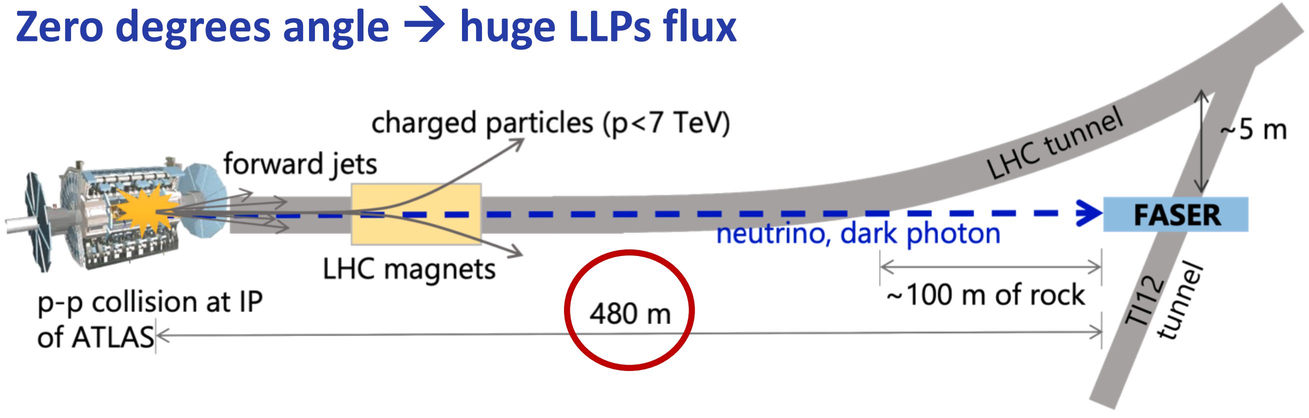
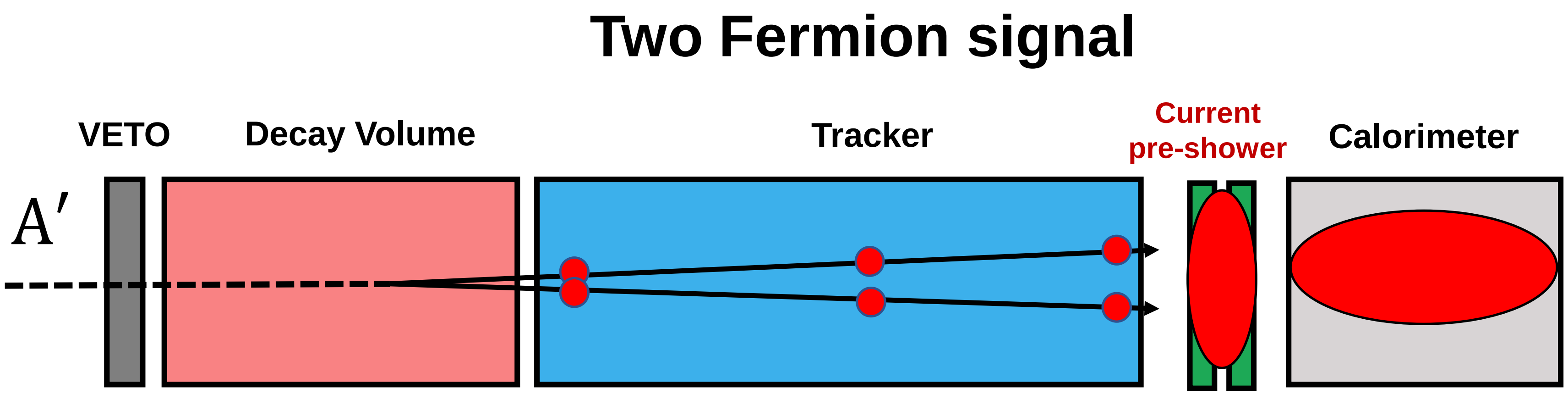
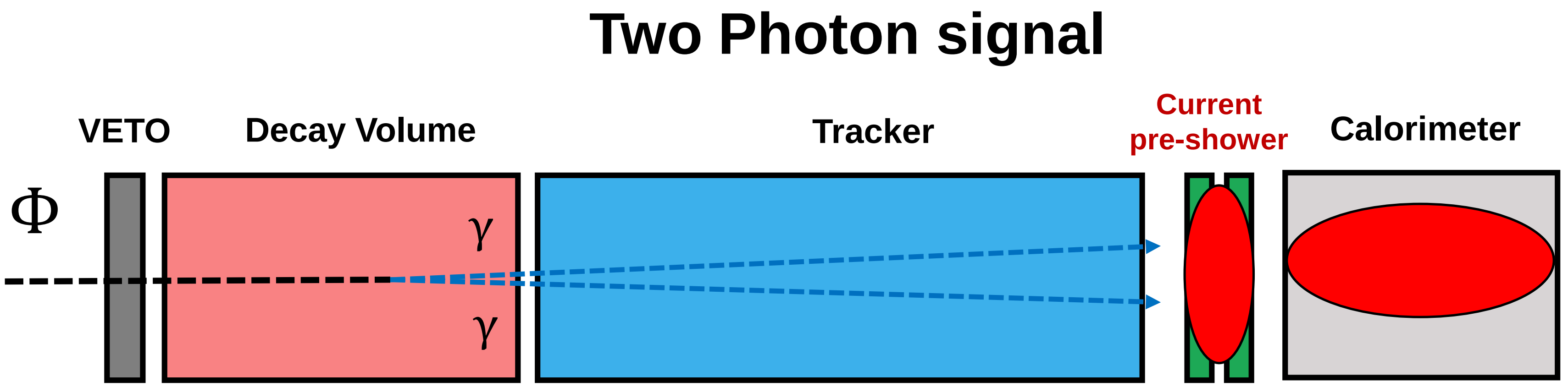


Figure: Location of FASER in the tunnel - schema is not in scale.

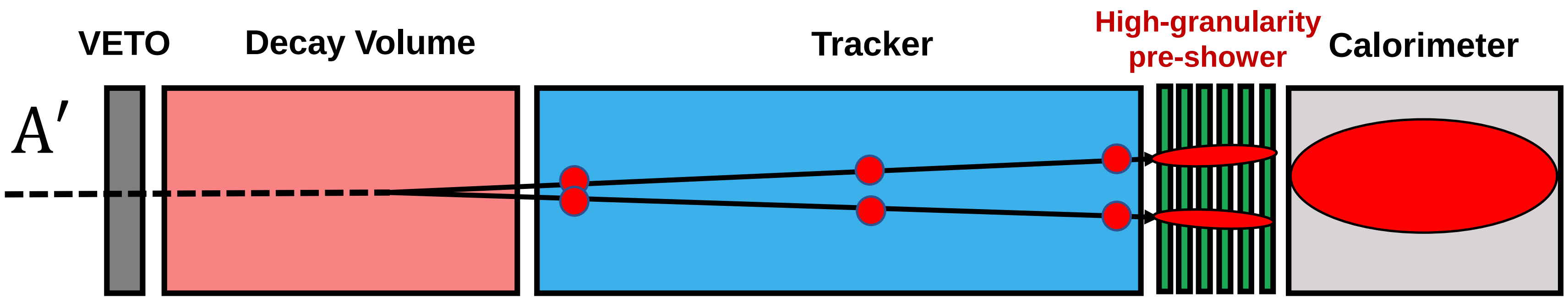
What Are We Able to Detect Well: Two Fermion Signal



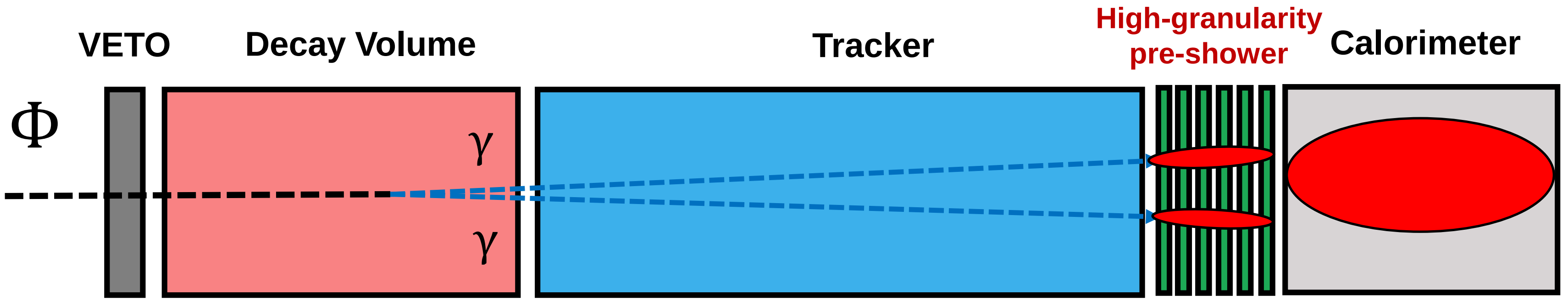


What Are We Willing to Detect: Two Photon Signal

Two Fermion signal



Two Photon signal



What Are We Willing to Detect: Two Photon Signal

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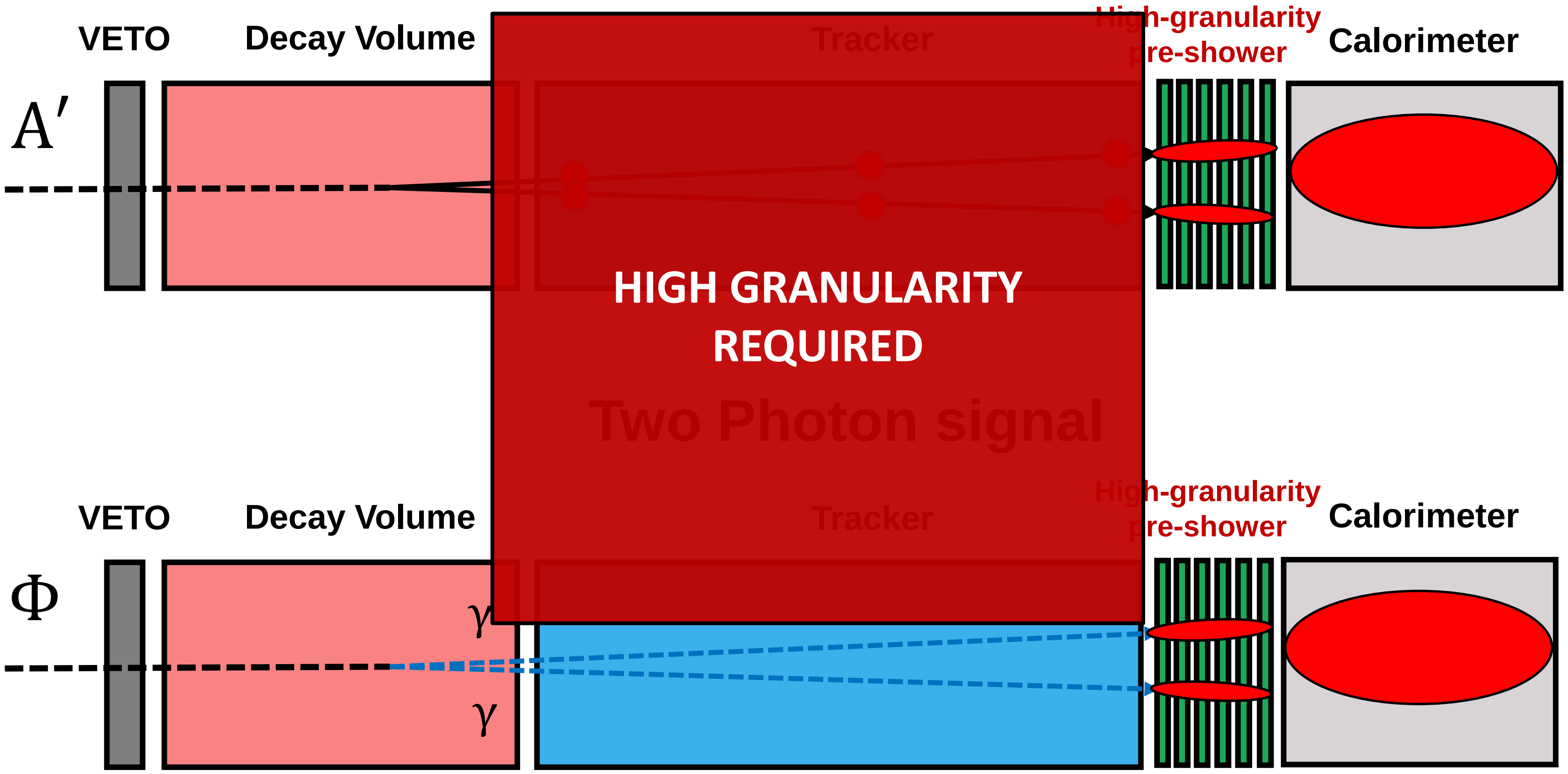
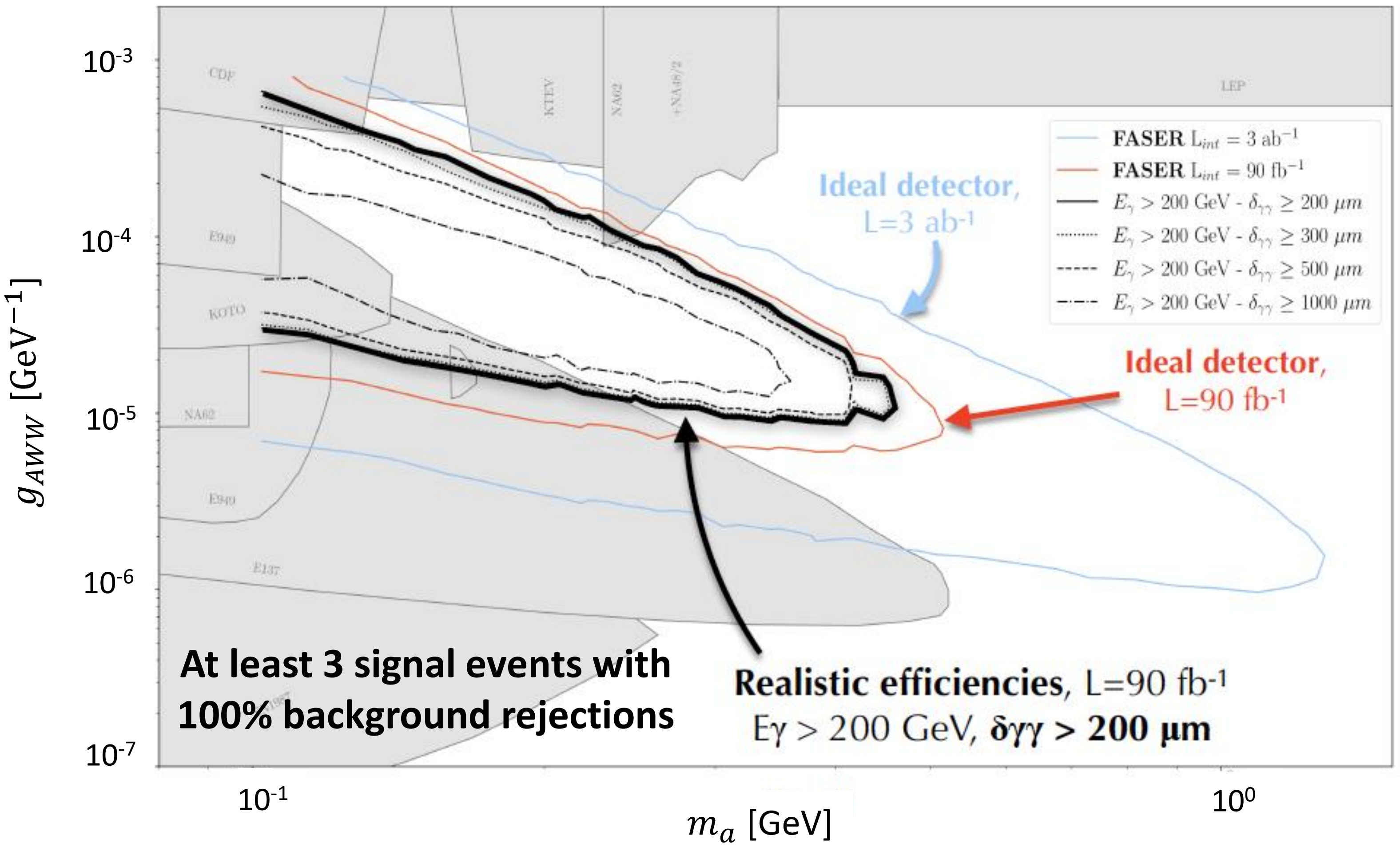
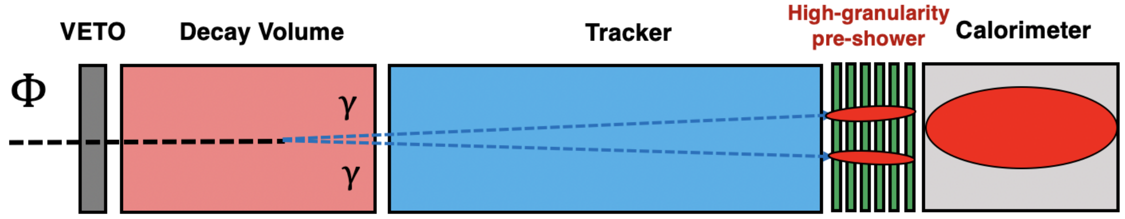


Physics with FASER

- FASER can probe **Axion-Like-Particles** (ALPs) model
- ALPs produced via the aWW coupling
- ALPs **decay into a photon-pair** within FASER volume



Two Photon signal



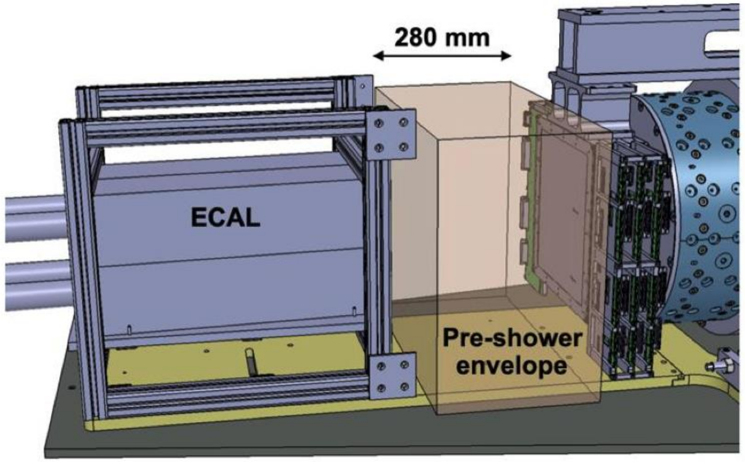
H. Abreu et al. "The FASER W-Si High Precision Preshower Technical Proposal" CERN-LHCC-2022-006 ; LHCC-P-023 https://cds.cern.ch/record/2803084

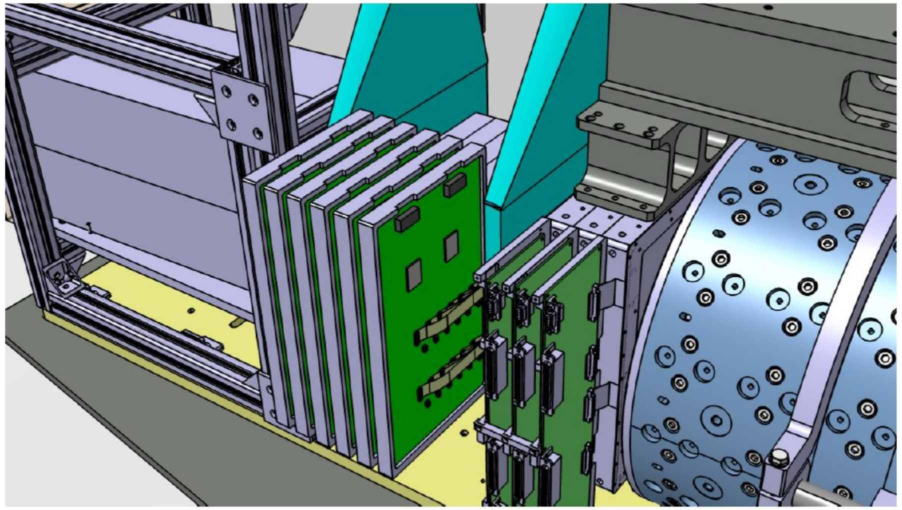
Preshower Detector Upgrade

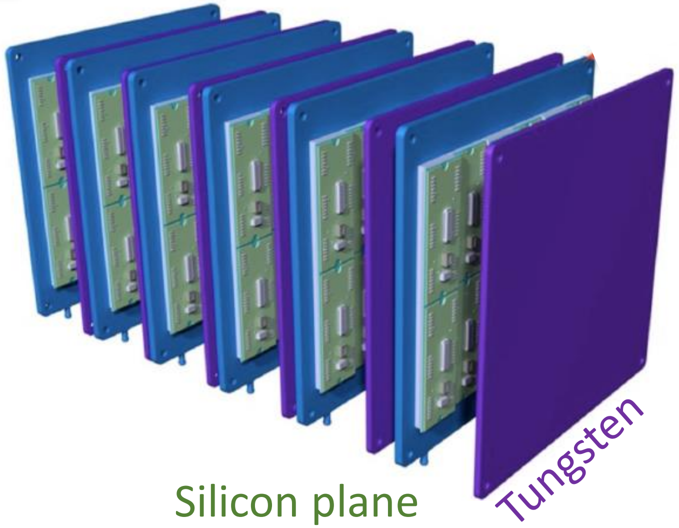
H. Abreu et al. "The FASER W-Si High Precision Preshower Technical Proposal" CERN-LHCC-2022-006 ; LHCC-P-023 https://cds.cern.ch/record/2803084

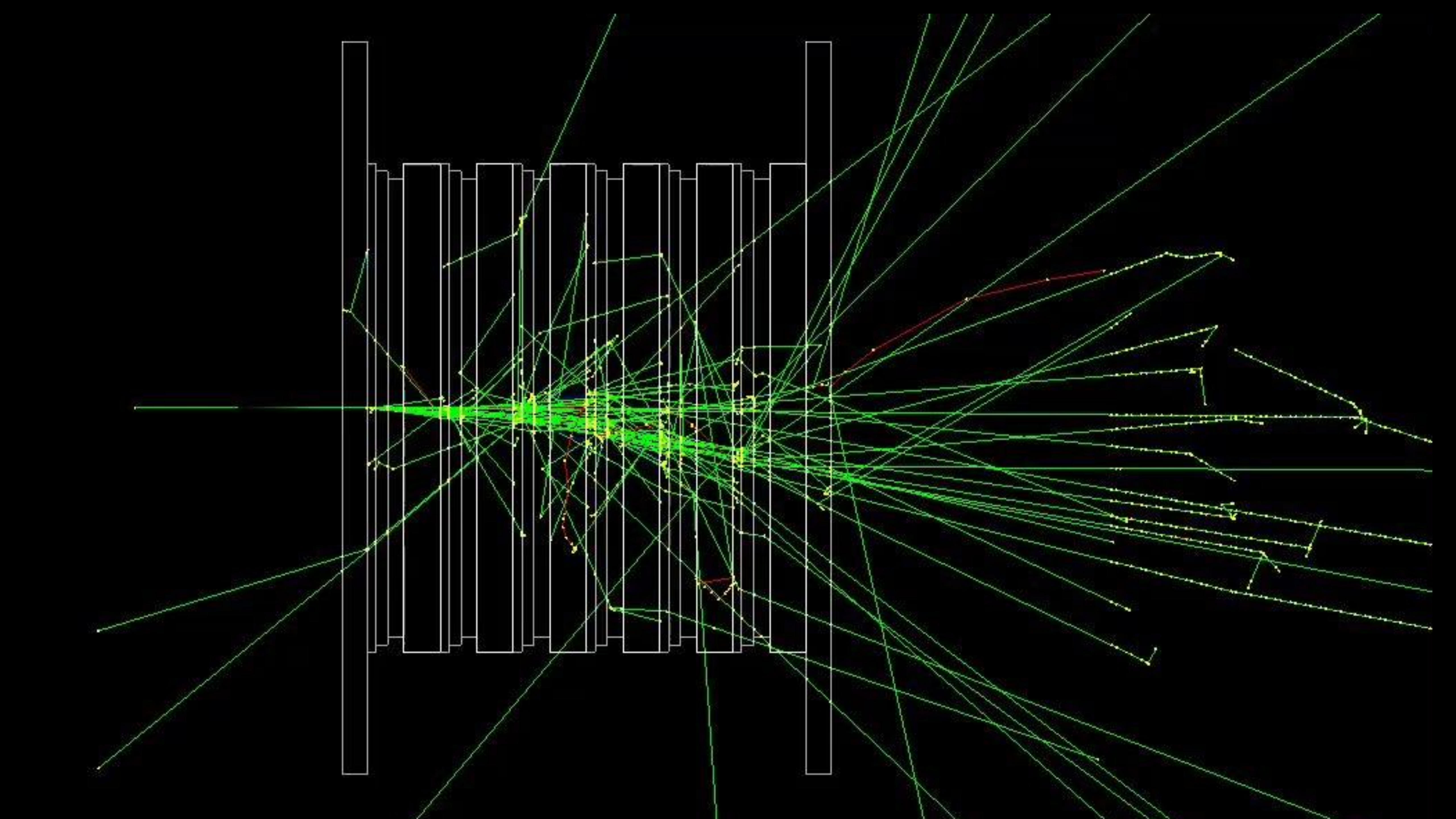
- 6 detector planes
- Each detector plane: **1 X0 of tungsten** + plane of **monolithic Si-pixel sensors**

Independent measurement of two very collimated photons at TeV energy scale

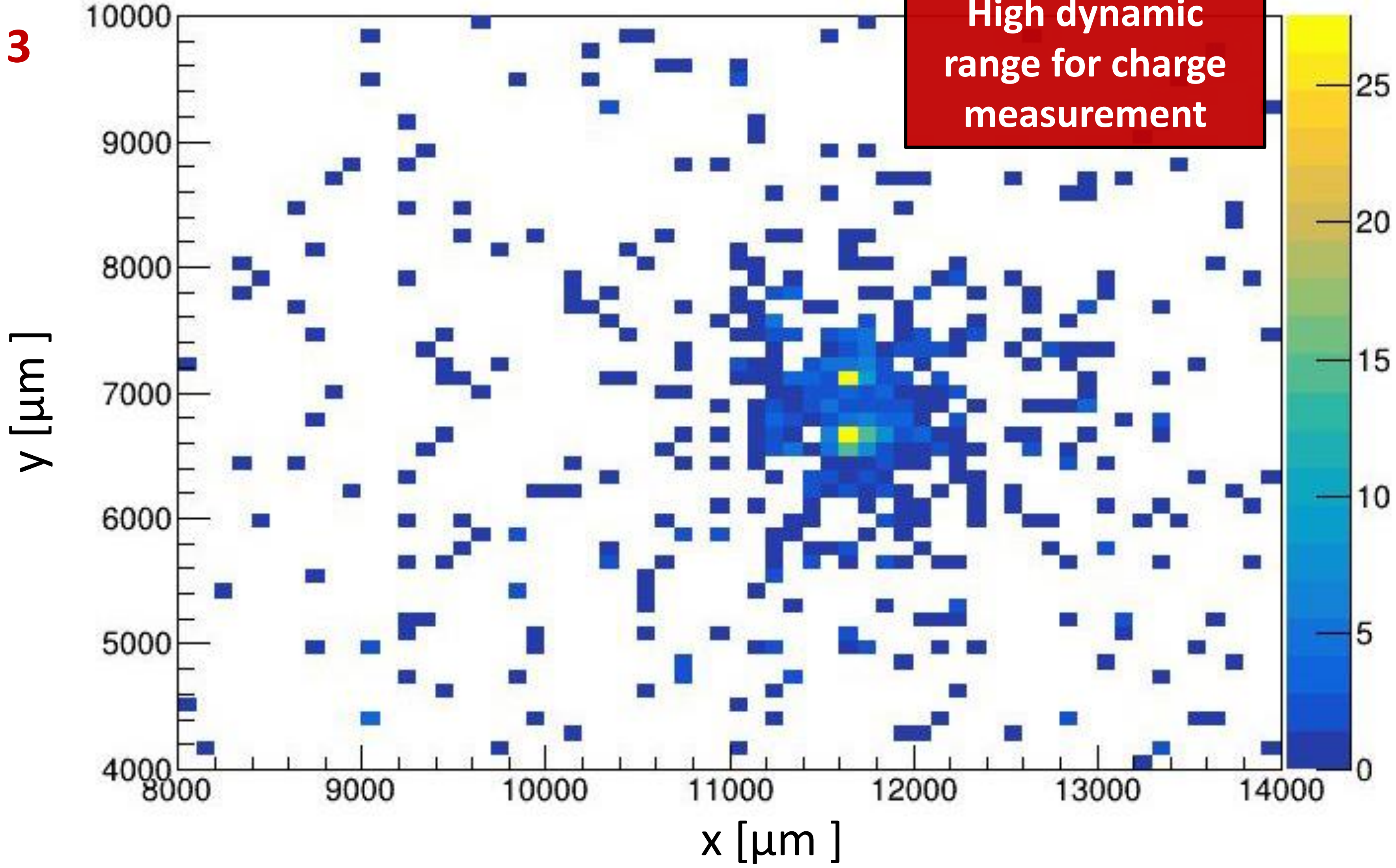








PLANE 3



High dynamic range for charge measurement

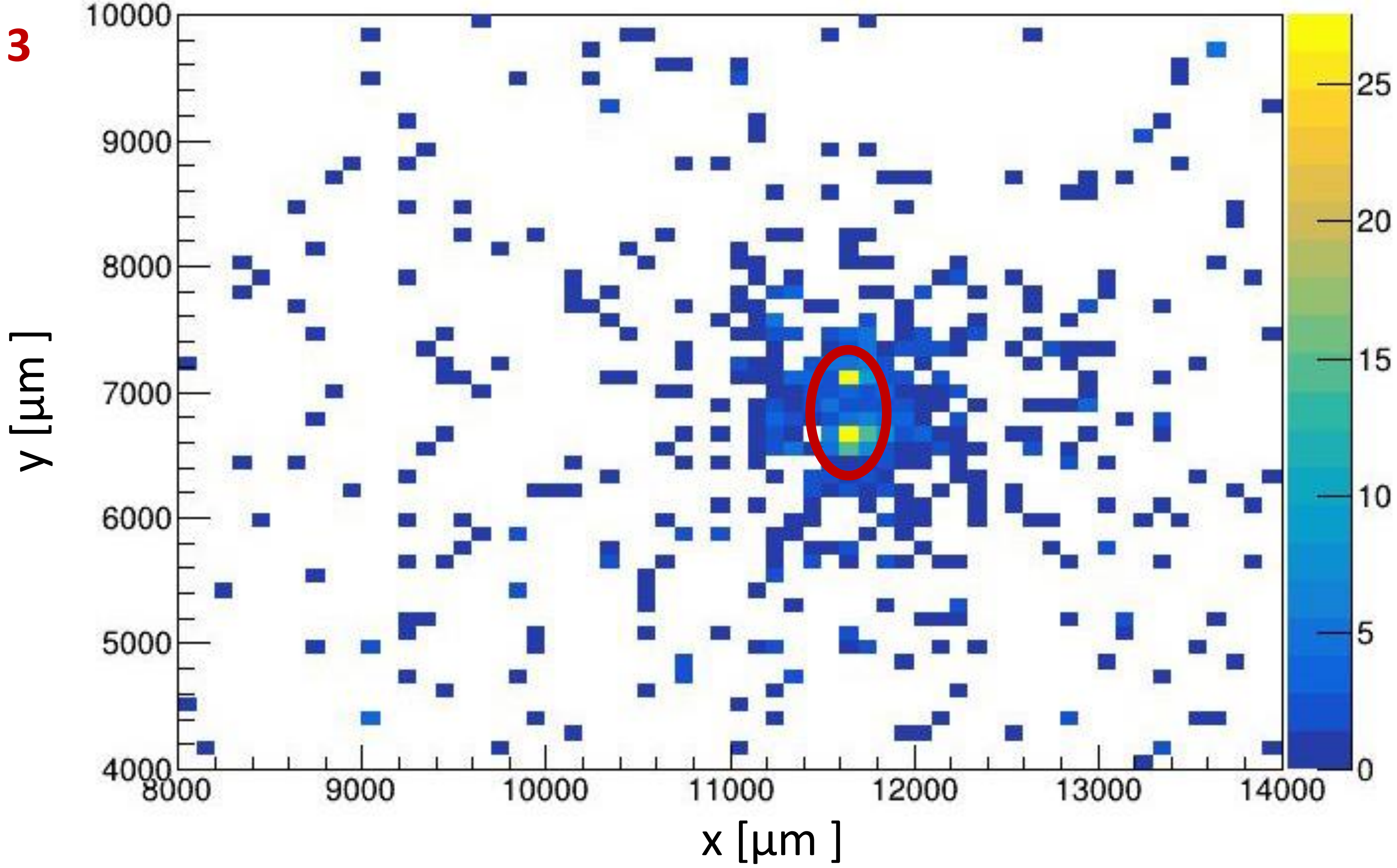
- **Why 6 planes?**
- **Why pixelated sensors?**

$E_{\gamma 1}$= 1 TeV
$E_{\gamma 2}$= 1 TeV

$d(\gamma 1, \gamma 2) = 500\ \mu m$

Events simulated using Allpixsquared 100 µm pixel pitch

PLANE 3



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$E_{\gamma 1}$ = 1 TeV

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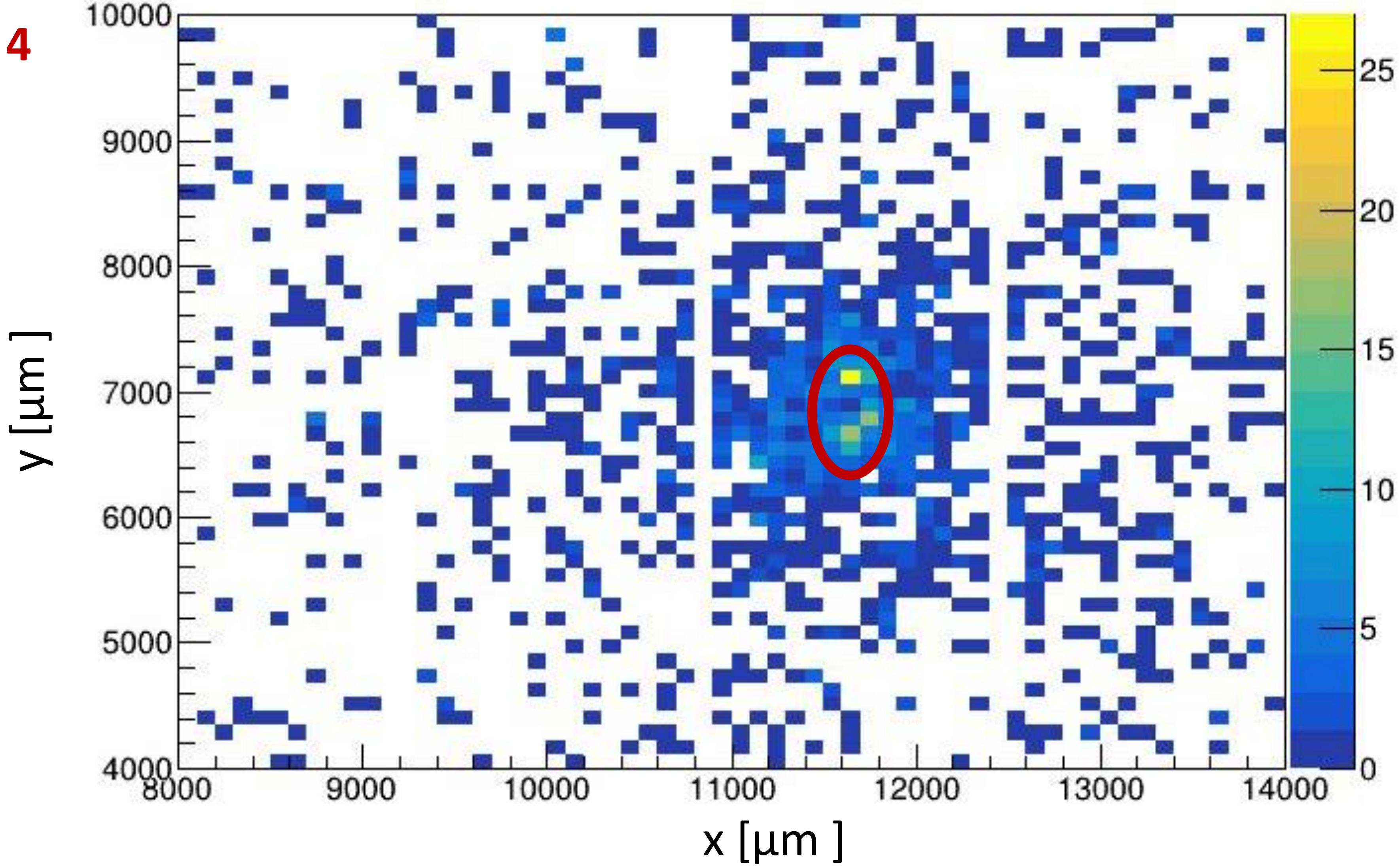
d($\gamma 1, \gamma 2) = 500$ µm

Events simulated using Allpixsquared 100 µm pixel pitch

PLANE 4



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$E_{\gamma1}$= 1 TeV
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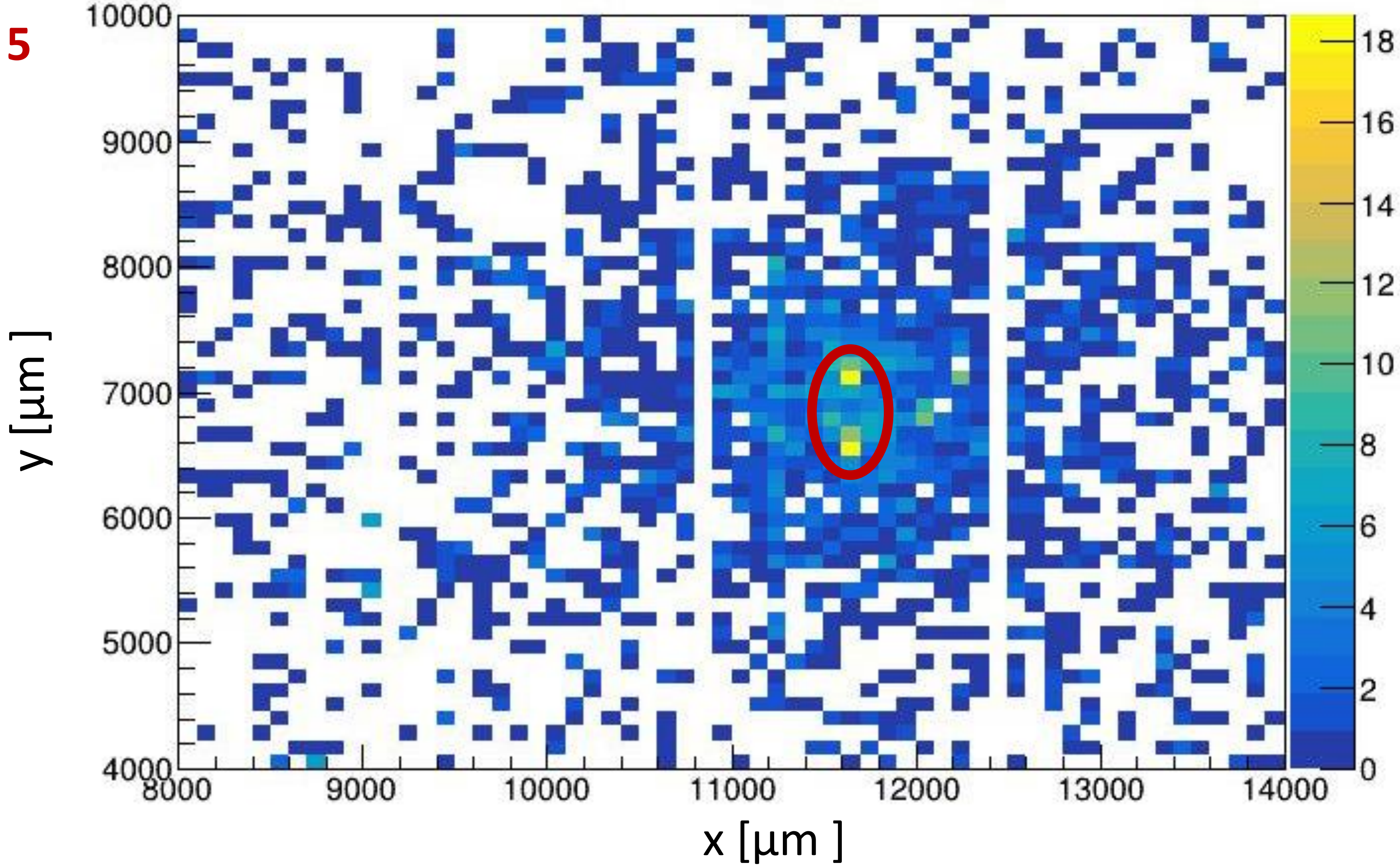
$d(\gamma1, \gamma2) = 500$ µm

Events simulated using Allpixsquared 100 µm pixel pitch

PLANE 5



- Why 6 planes?
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$E_{\gamma 1}$= 1 TeV

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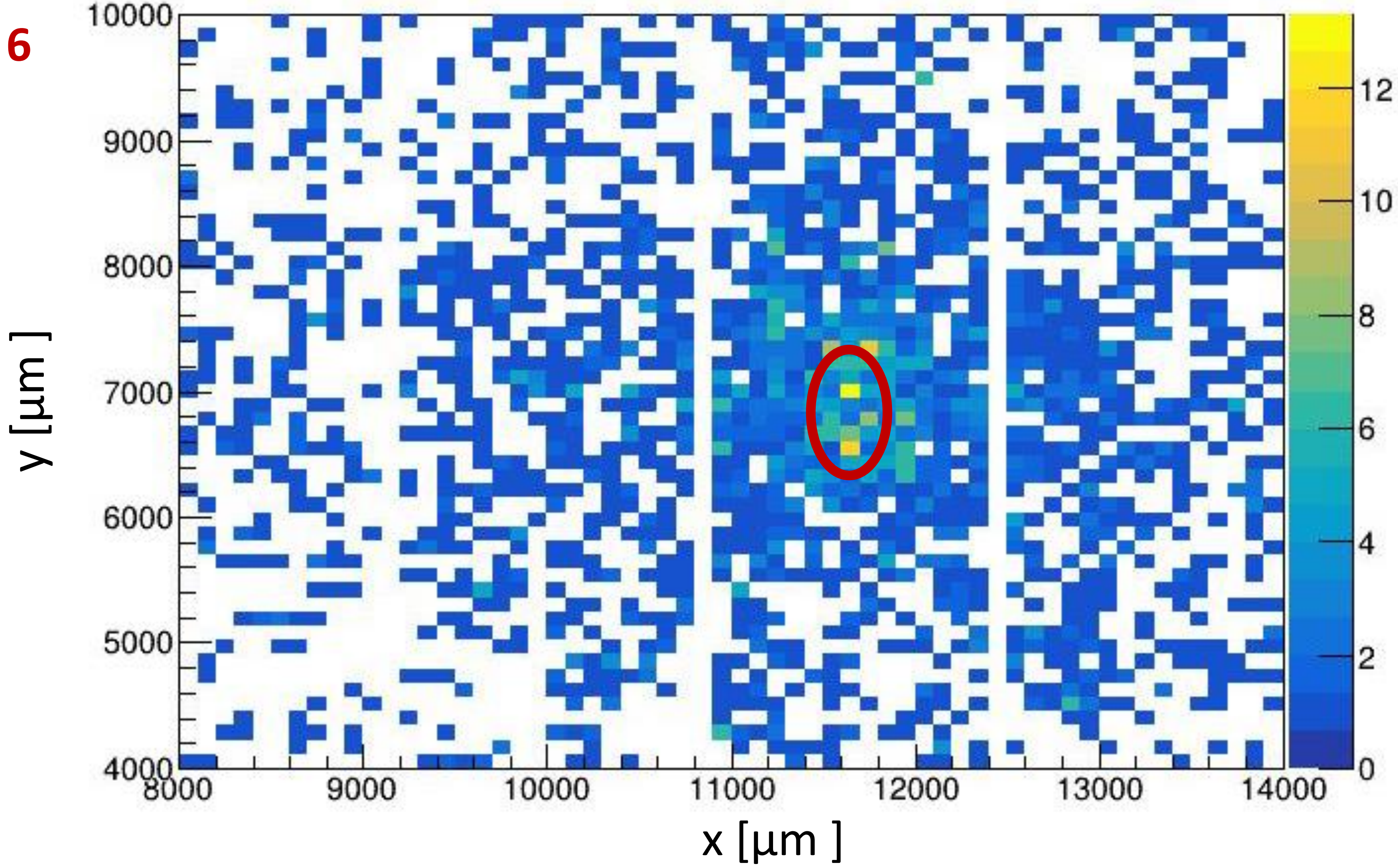
d($\gamma 1, \gamma 2$) = 500 µm

Events simulated using Allpixsquared
100 µm pixel pitch

PLANE 6



- **Why 6 planes?**
- **Why pixelated sensors?**

$E_{\gamma 1}$= 1 TeV
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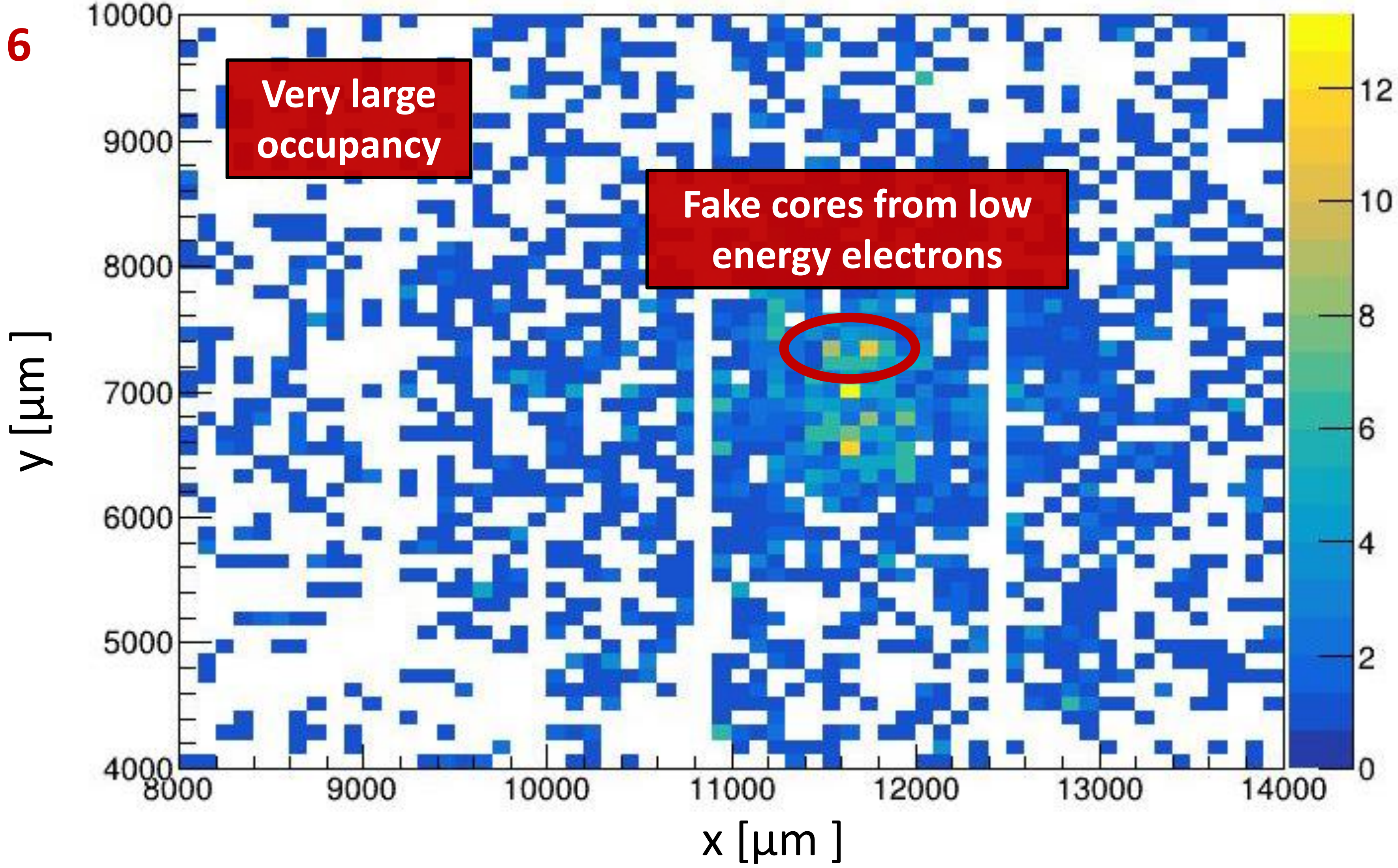
Events simulated using Allpixsquared 100 µm pixel pitch

PLANE 6



- Why 6 planes?
- Why pixelated sensors?

$E_{\gamma 1}$= 1 TeV

$E_{\gamma 2}$= 1 TeV

$d(\gamma 1, \gamma 2) = 500\ \mu m$

Events simulated using Allpixsquared
100 µm pixel pitch

Monolithic ASIC Specifications

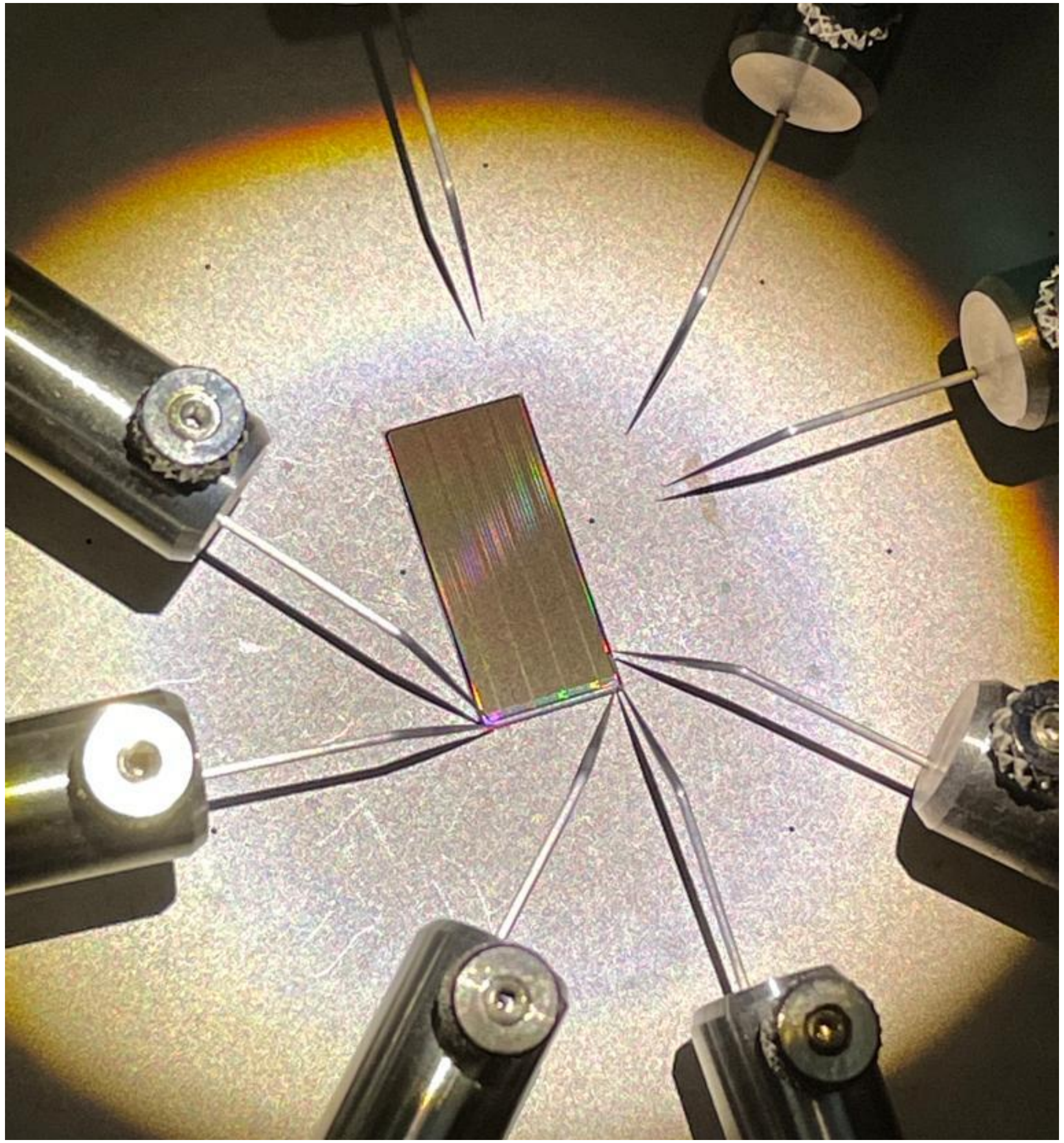
Main specifications	
Pixel Size	65 µm side (hexagonal) ~ 100 µm pitch
Pixel dynamic range	0.5 ÷ 65 fC
Cluster size	O(1000) pixels
Readout time	< 200 µs
Time resolution	< 300 ps
Power consumption	< 150 mW/cm^2

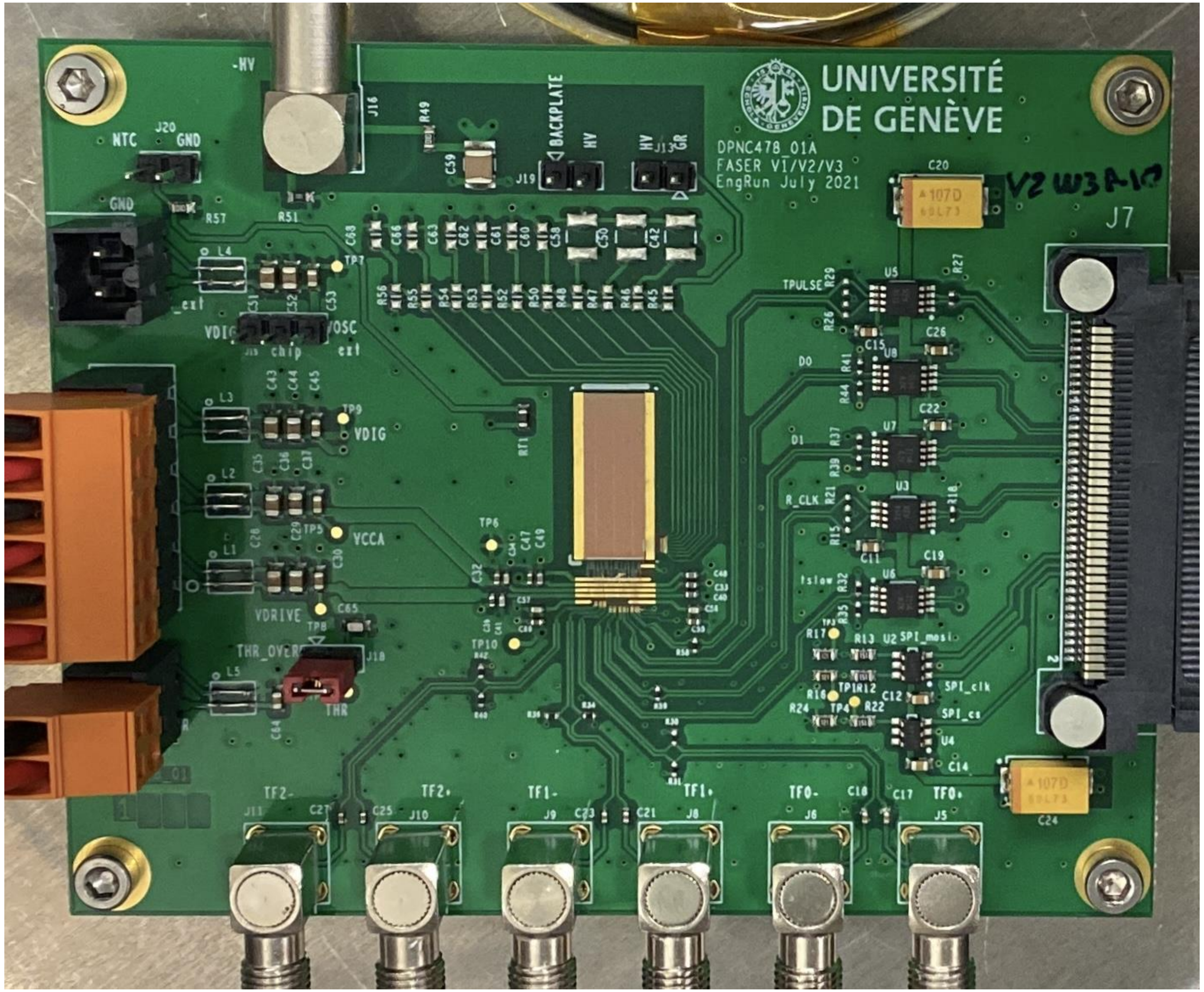
Selected technology: SG13G2, by IHP microelectronics.

ASIC design: University of Geneva, with support from KIT and CERN

- Monolithic ASIC in **130nm SiGe BiCMOS**
- Design tailored for new FASER preshower
- Pixel size: **hexagonal pixels with 65 µm side** (~ 100 µm pitch)
- Operates as an **ultra-fast imaging chip** (ultra-fast readout)

In between an imaging chip and a HEP detector



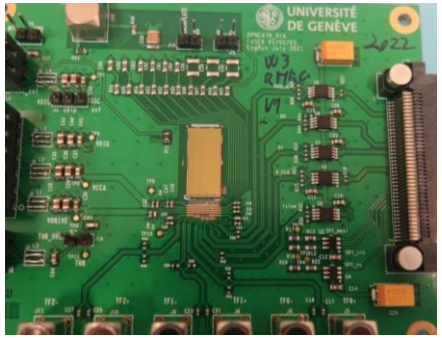


UNIVERSITÉ
DE GENÈVE
DPNC478_01A
FASER V1/V2/V3
EngRun July 2021
V2 W3A-10
J7
-HV
NTC
GND
VDIG
VCCA
VDRIVE
THR_OVER
THR
TF2-
TF2+
TF1-
TF1+
TF0-
TF0+
SPI_clk
SPI_cs
BACKPLATE

On-going Studies

Lab Test on the Pre-production Chip

- Chip response
- Readout
- Effects seen in simulation



Background Studies

- Muons
- Neutrinos' DIS

→ Variables to discriminate signal from background (angle of emission etc.)

PRESHOWER UPGRADE

Design of the New Chip

- Based on lab studies and tests
- To be submitted in May 2023

Event Reconstruction

- Improving recontruction algorithm
- Introducing Machine Learning

Summary and Conclusions

- New FASER preshower detector will **enable discrimination of photons** from LLPs decays

- Monolithic ASIC to distinguish clusters from **two ultra-collimated high-energy electromagnetic showers**
  - **Hexagonal pixels** with 65 μm side (≈ 100 μm pitch)
  - **High dynamic range (from 0.5 fC to 65 fC)**
  - **Ultra-fast readout**

- New pre-shower installed in ‘23/’24 winter break to **take data during LHC Run3**

Thank you !

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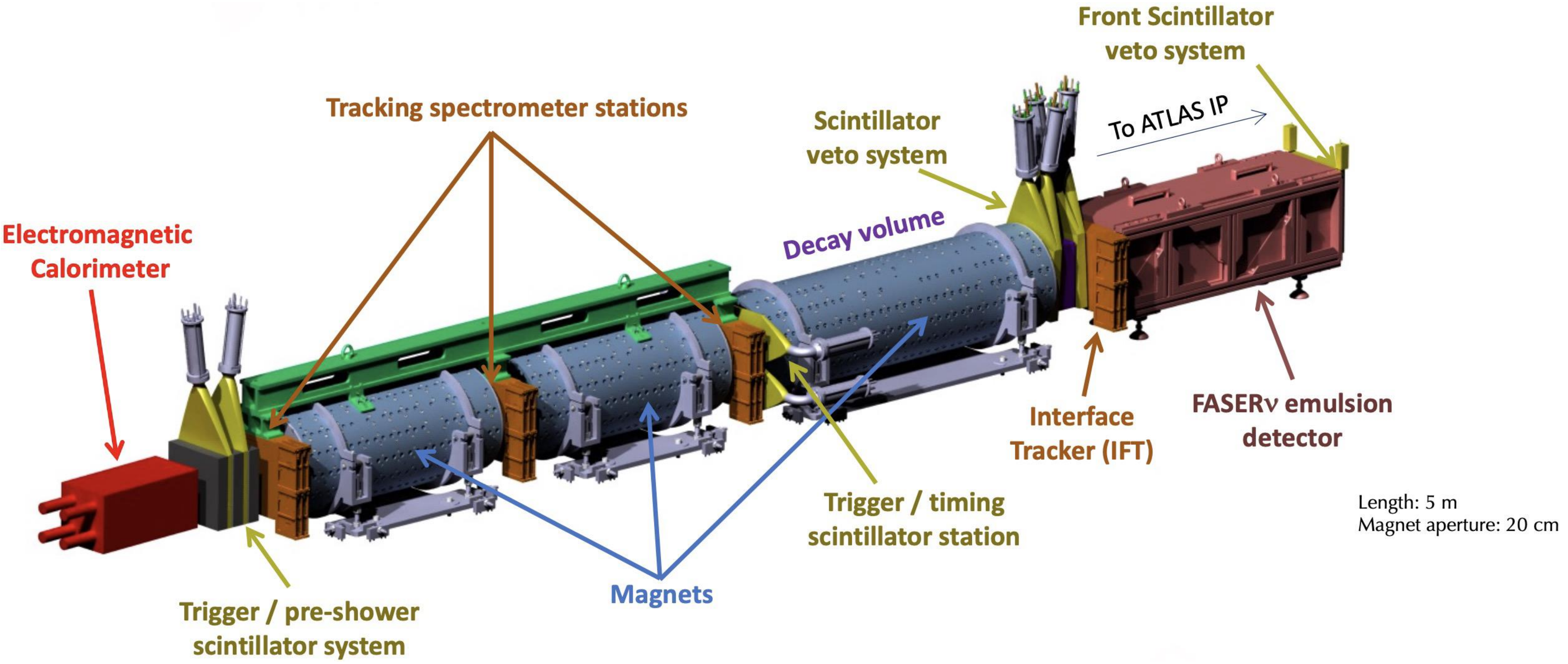
And if you want to know more:

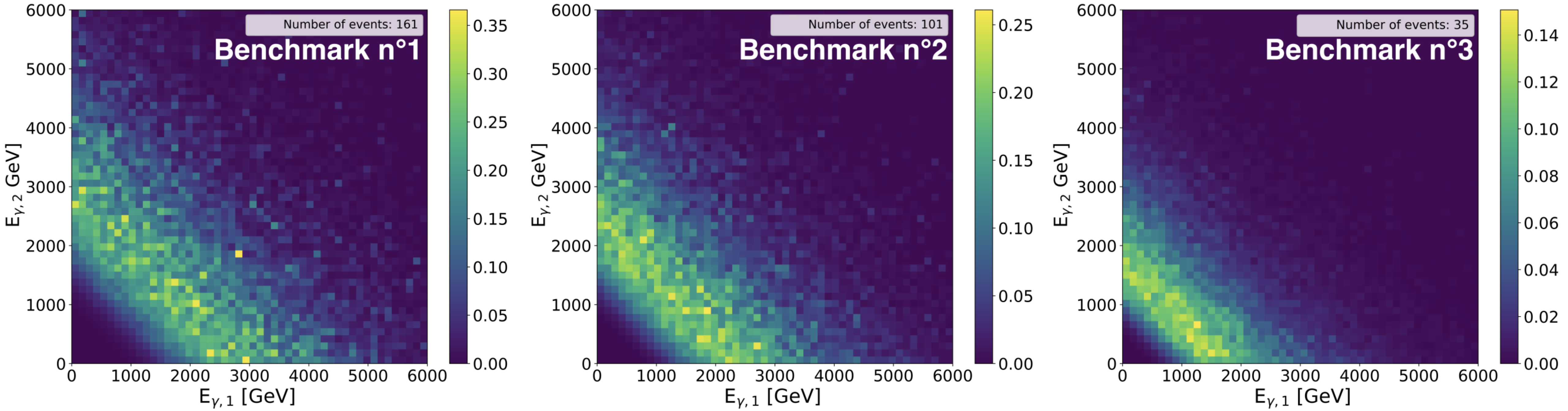
H. Abreu et al. "The FASER W-Si High Precision Preshower Technical Proposal"
CERN-LHCC-2022-006 ; LHCC-P-023
https://cds.cern.ch/record/2803084

BACKUP SLIDES

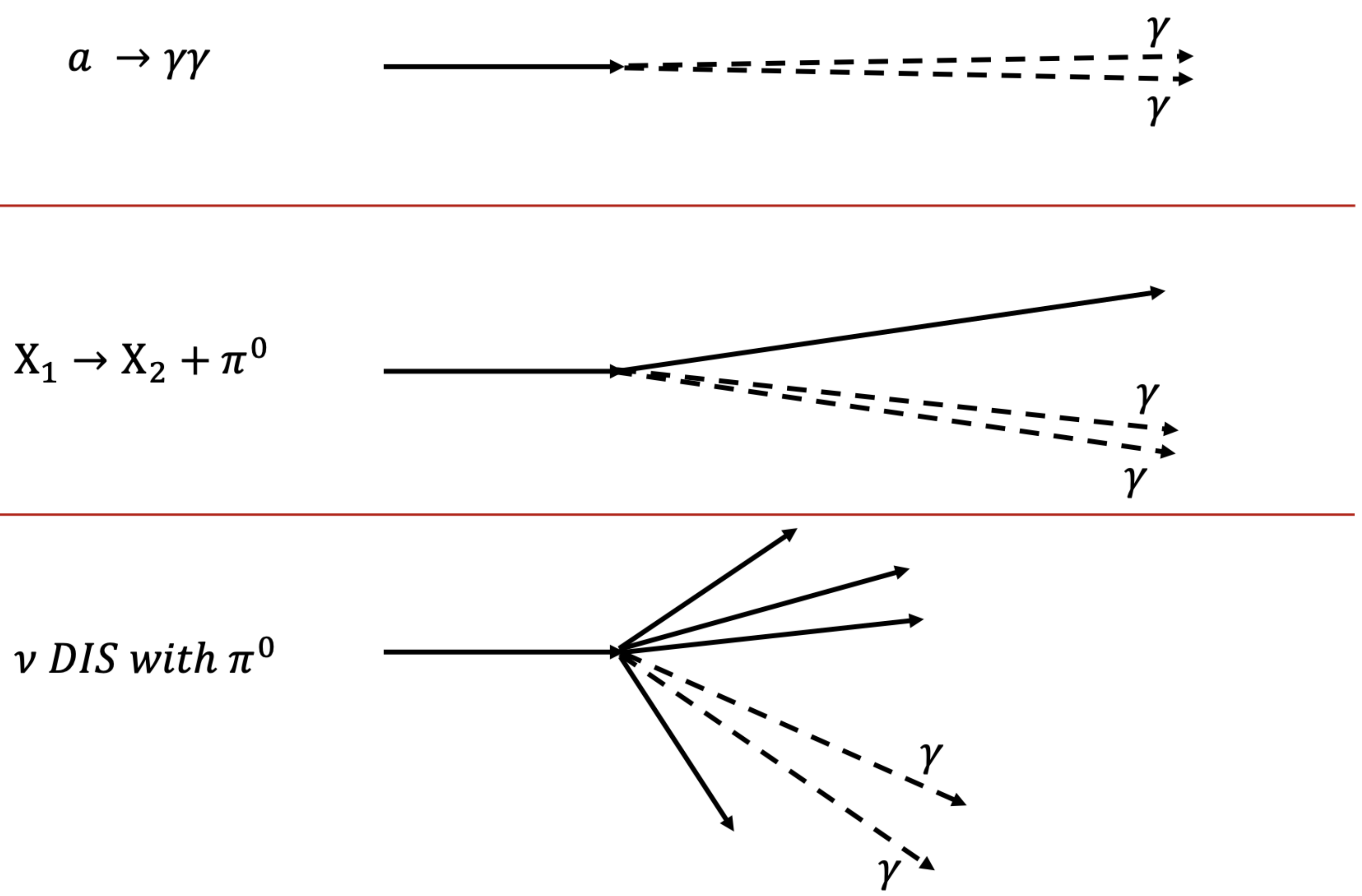
The FASER Experiment



Di-photon Signal Energy Distributions



New physics signature



- Few mrad angular resolution
- Low occupancy
- Photon discrimination
- Combined information with tracking stations

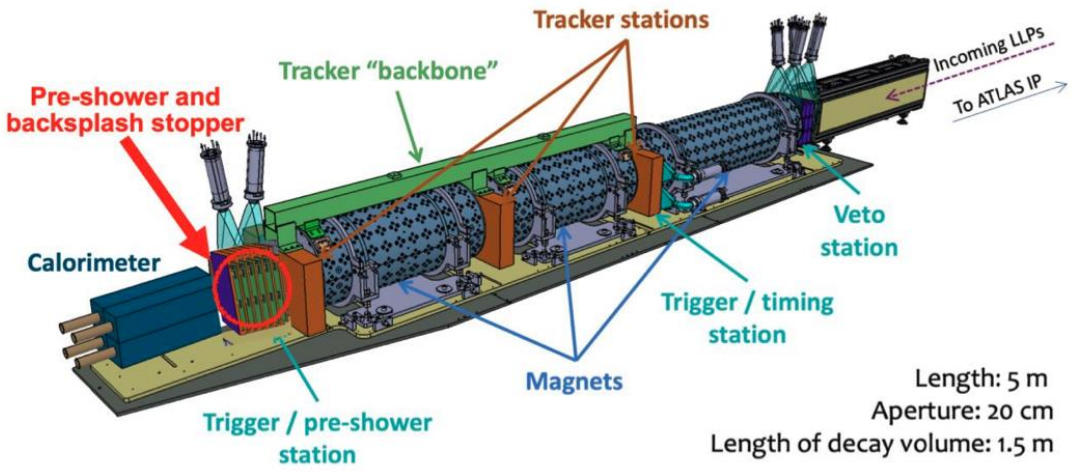
Physics reasons for the new pre-shower

- Enables measurement:
  - Axion-Like Particles (ALP) produced via aWW coupling.
  - LLP with neutral pions in the final state.
  - Neutrino background suppression.

- Reinforces measurement:
  - Dark photon and other LLPs decaying into charged fermions.
  - LLP with charged and neutral pions in the final state.

The FASER Pre-shower Detector Upgrade

- MAIN CHALLENGE: ***Resolve separate photon signatures*** before coarser calorimeter ⇨ preshower needed



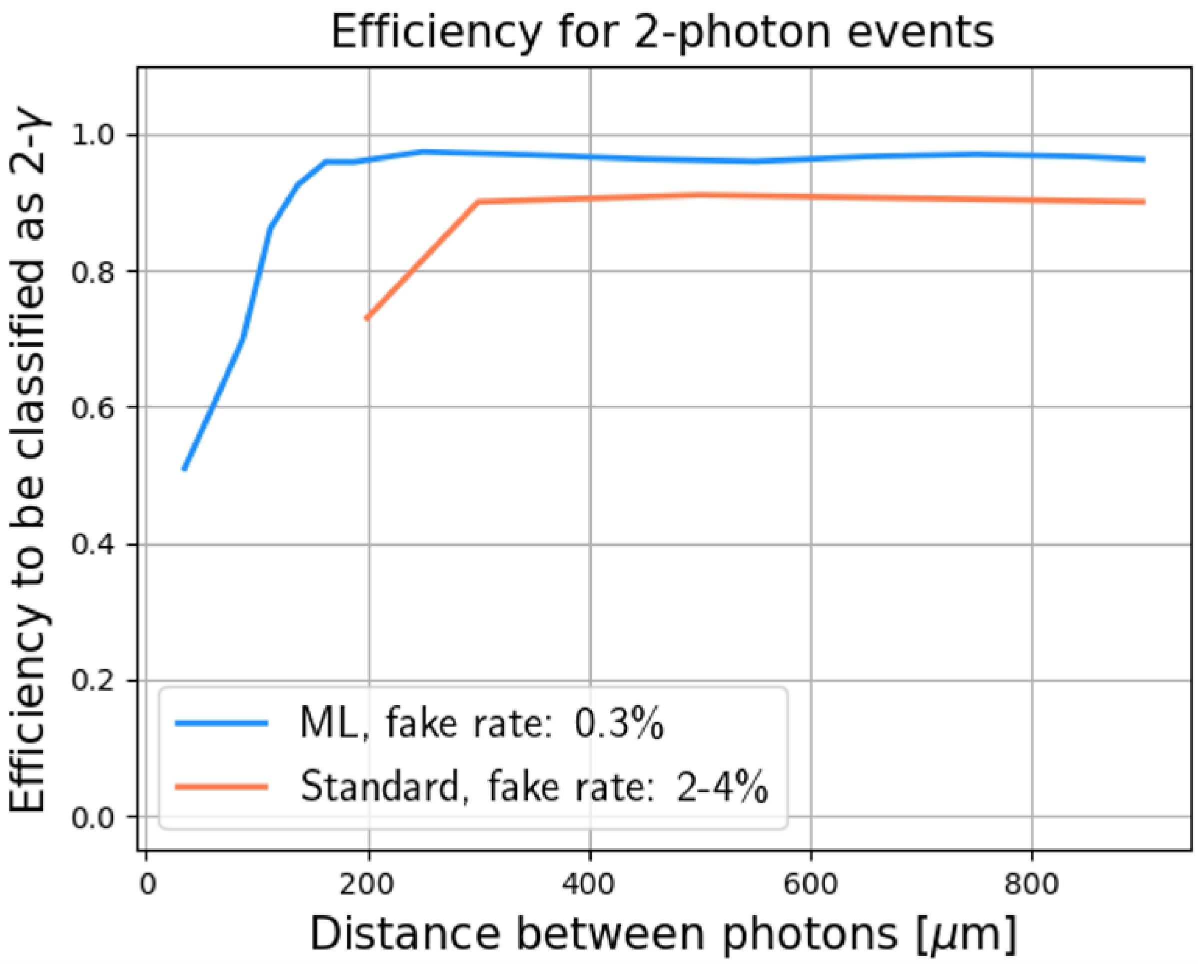
- **<u>Current preshower</u>**:

  2 layers of tungsten (1X0) + scintillating detectors
  ⇨ no XY granularity

- Main goal of the upgraded preshower detector:
  - **High granularity/high dynamic range** for charge measurements
  - Pre-shower based on monolithic silicon pixel sensors
  - Discriminate **TeV scale electromagnetic showers**
  - Targeting data-taking in 2024/2025, during LHC Run3 and during HL-LHC

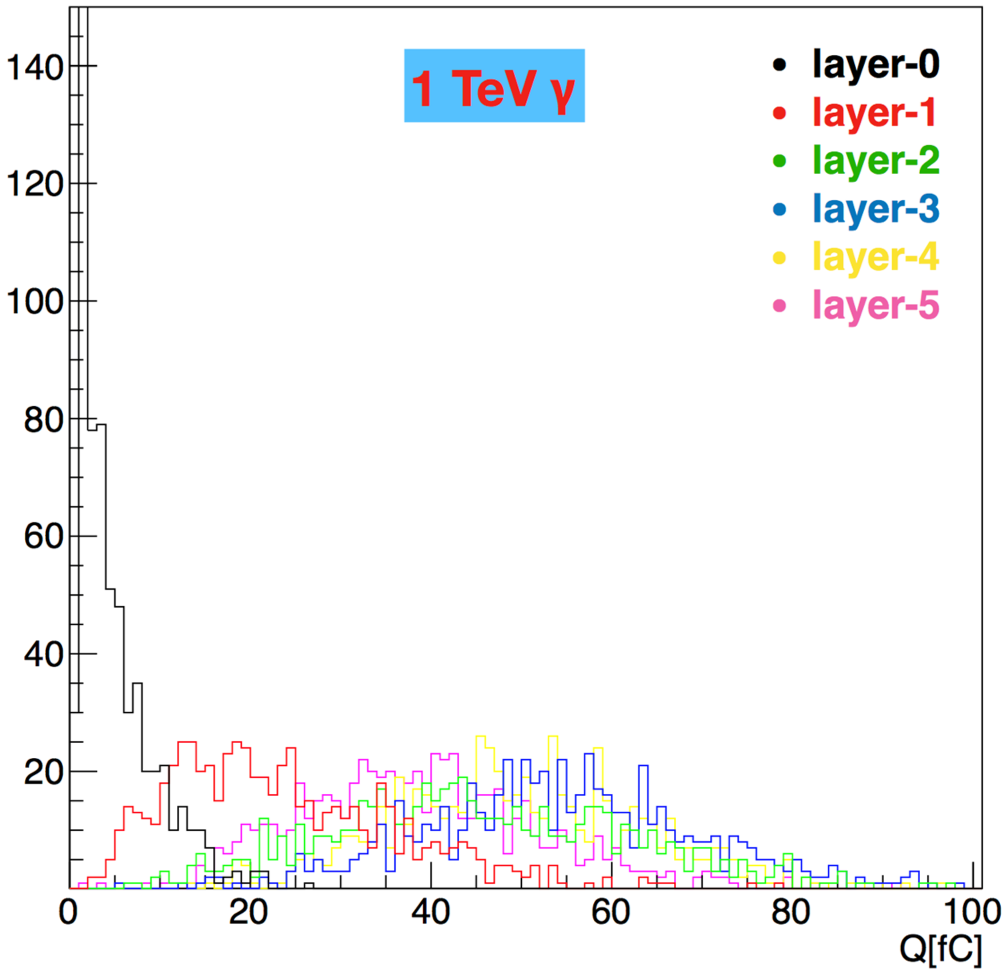
Di-Photon Reconstruction Efficiencies

$E_{\gamma 1}$= 1 TeV
$E_{\gamma 2}$= 1 TeV



Electromagnetic Shower Development

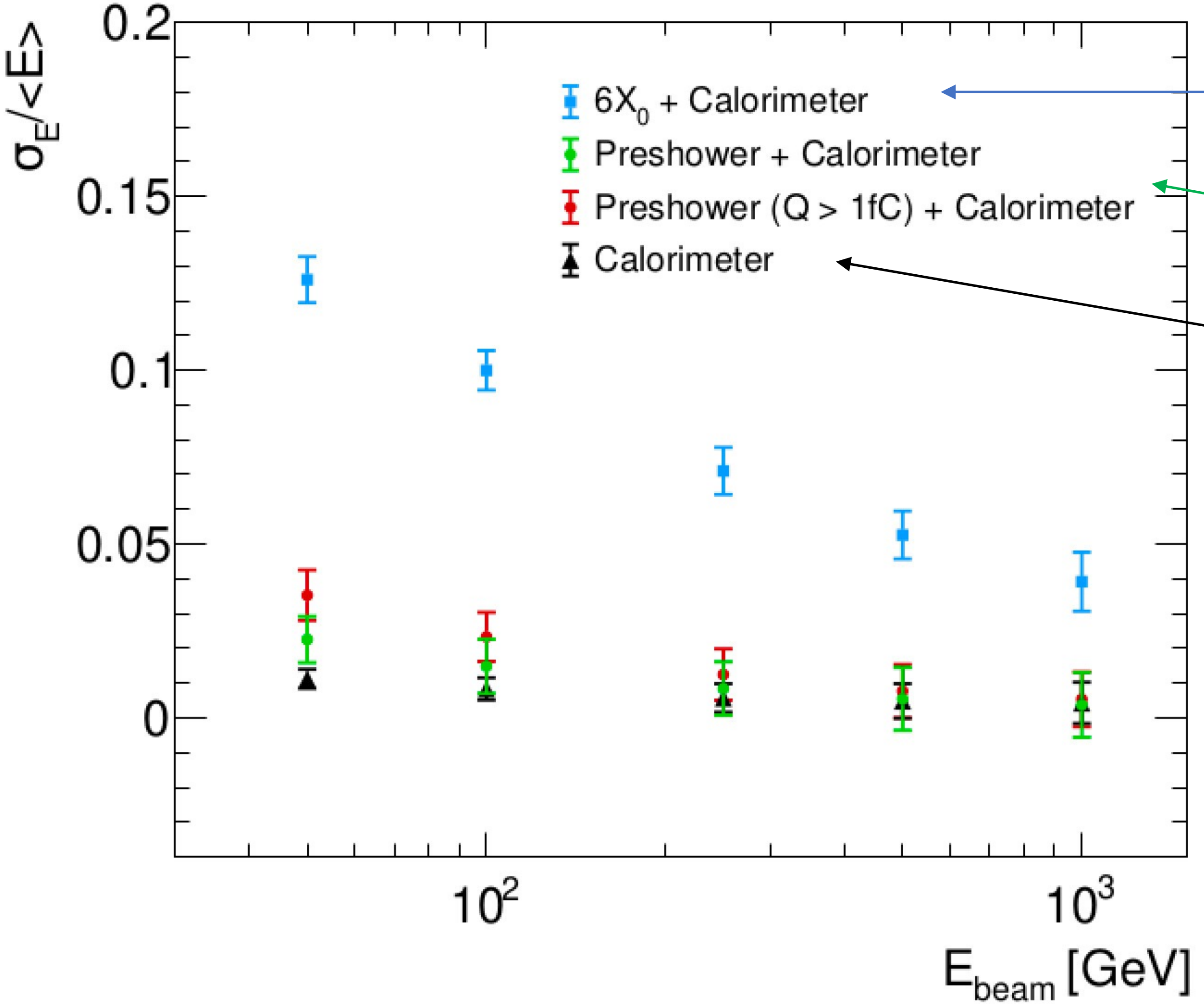
Total charge deposited at the peak of the electromagnetic shower



1 photon at $E = 1\text{TeV}$ converting in the first layer

- The charge deposited increases while traversing more tungsten
- After 4 layer (= 4X0) the amount of charge deposited decreases —> the EM shower begins to die

Energy resolution



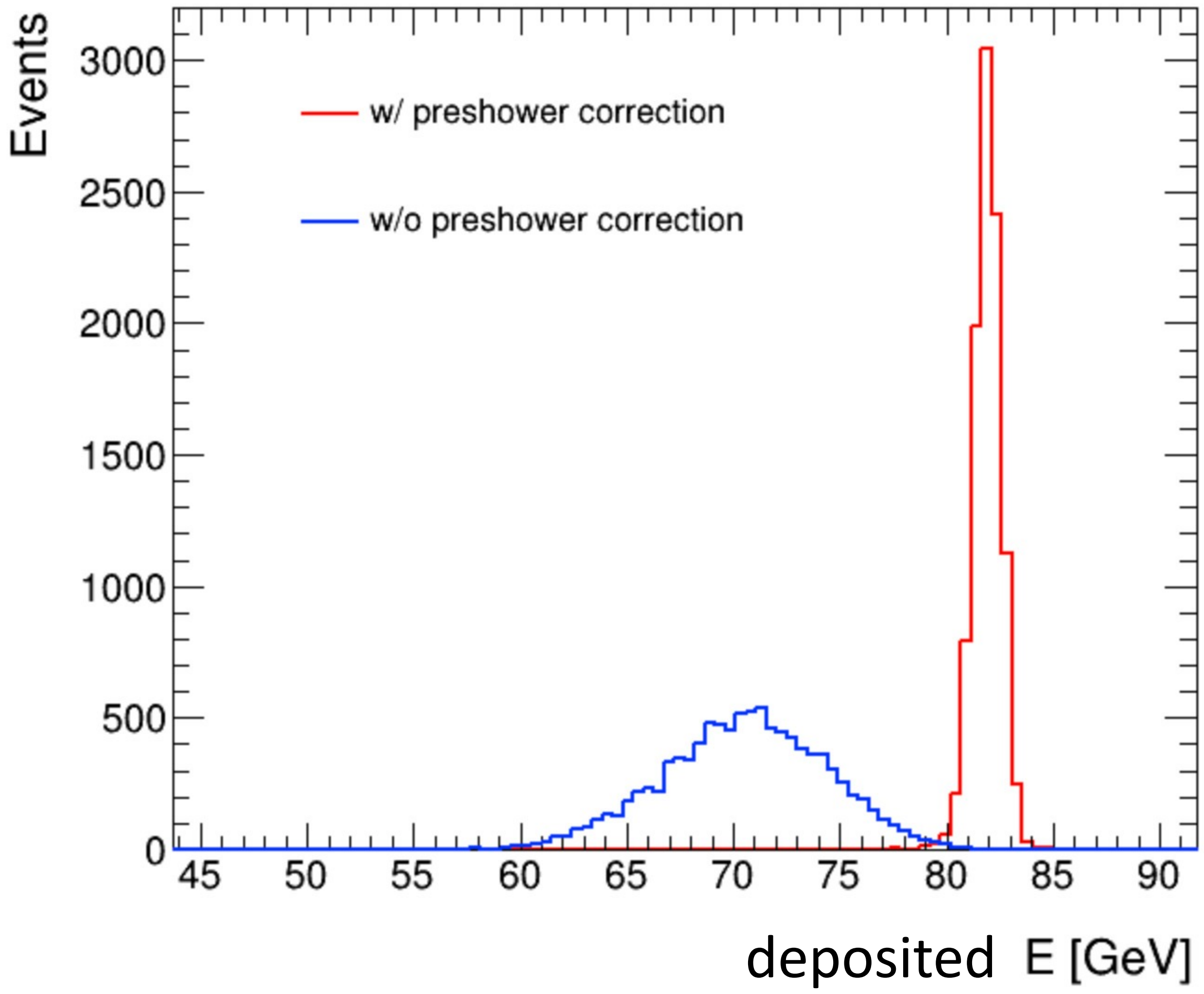
Only looking at the calorimeter (not using the preshower information)

Correcting with the Preshower energy

Calorimeter only

Energy resolution

For 500 GeV photons



The FASER Small Prototype Chip

F. Martinelli et al.
2021 *J. Inst.* **16** P12038
https://doi.org/10.1088/1748-0221/16/12/P12038

Purpose

study **different level of INTEGRATION OF THE FRONT-END** electronics inside the sensitive area of the pixels

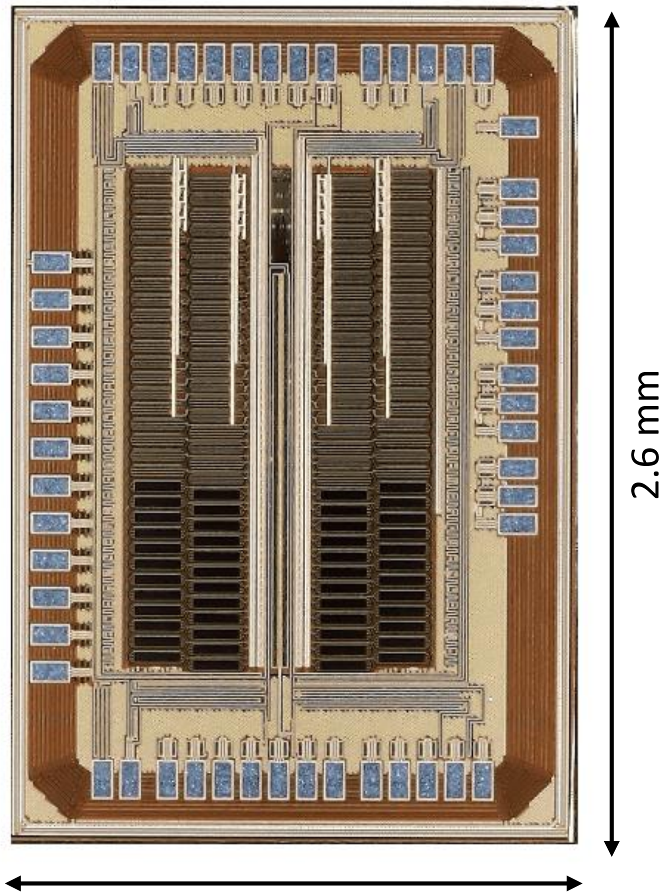
Final aim

identify the BEST FRONT-END CONFIGURATION for the pre-production chip of the FASER Pre-shower (submitted in June 2021)

200 µm x 50 µm PIXELS
shape to reduce the electric field at the edge of the sensitive areas

Tested in 2021

2 superpixels
16x4 pixels each



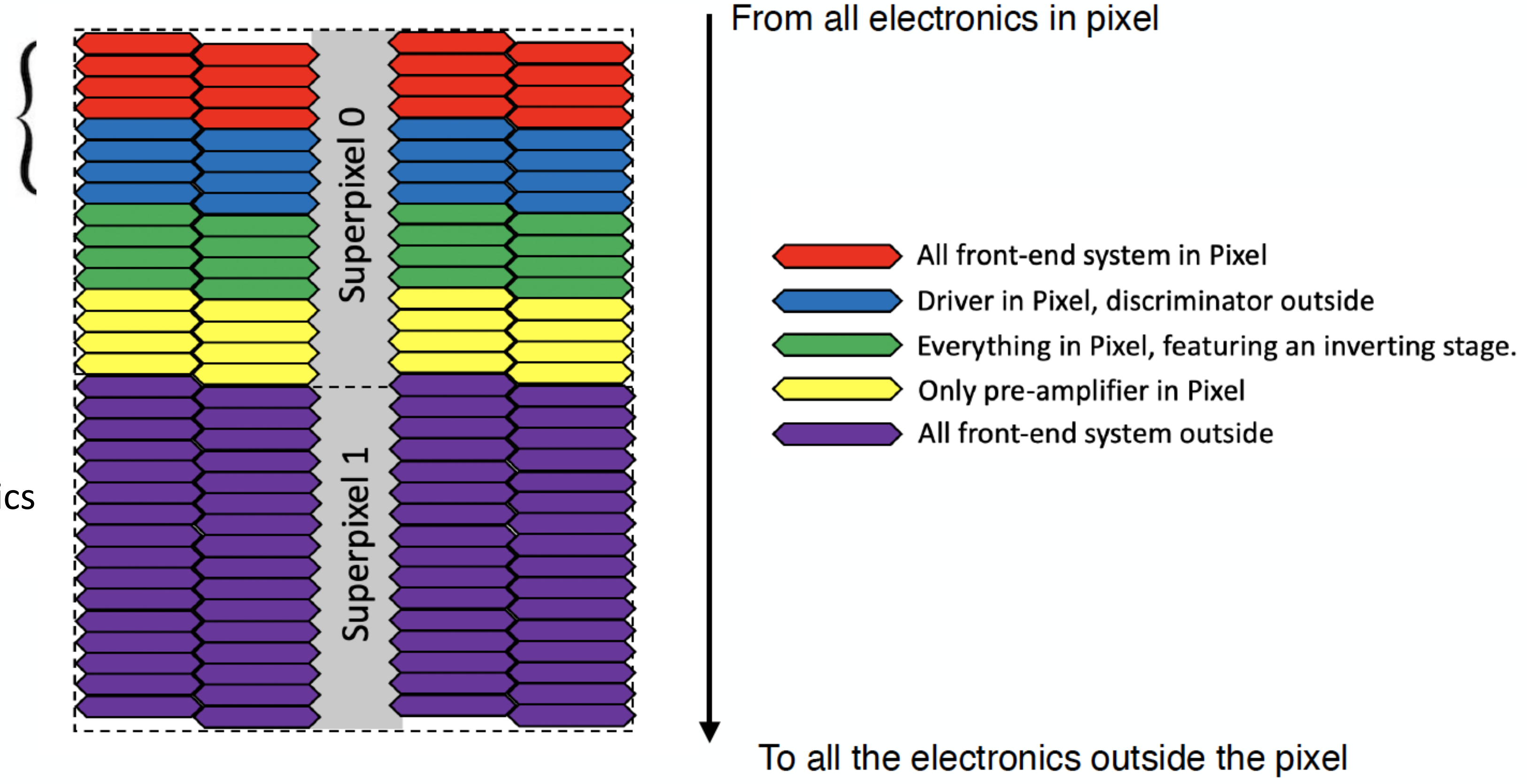
Small Prototype: Front-end Configurations

F. Martinelli et al.
2021 *J. Inst.* **16** P12038
https://doi.org/10.1088/1748-0221/16/12/P12038

5 Different front-end configurations

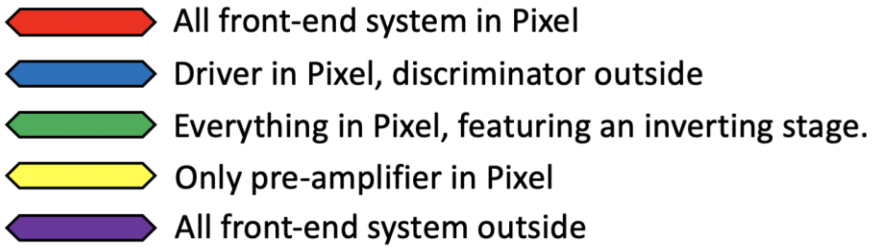
Configurations we would like to include

Backup configurations to still study electronics elements for the pre-production chip

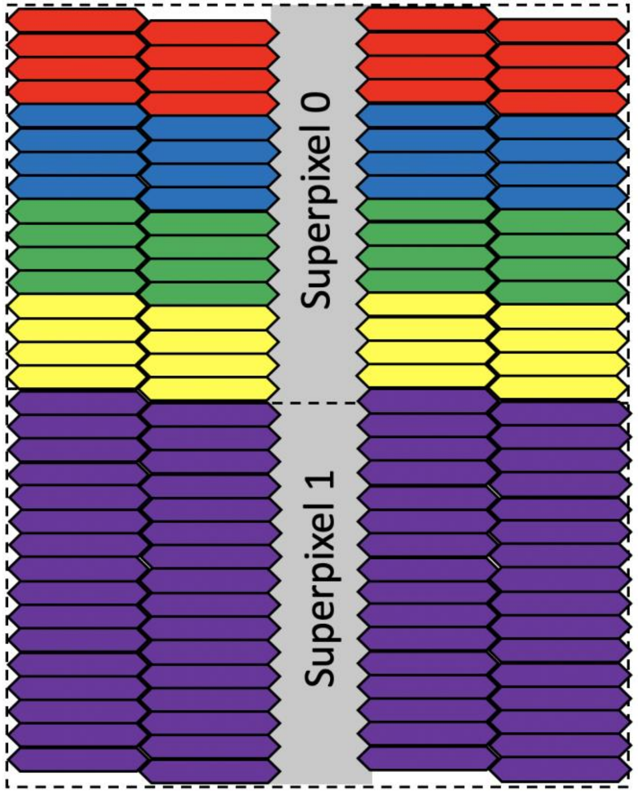


Small Prototype: Results and Comments

F. Martinelli et al.
2021 *J. Inst.* **16** P12038
https://doi.org/10.1088/1748-0221/16/12/P12038



Configuration	σ_v [mV]	G_c [mV/fC]	ENC [e⁻]	$\sigma_{V_{th}}$ [mV]
All f.e. outside pixel	4.2 ± 0.2	159 ± 1.0	165 ± 9	32.3
Only pre-amp. in pixel	2.5 ± 0.1	96.8 ± 0.5	161 ± 9	26.9
All f.e. in pixel, inv. stage	6.9 ± 0.5	179 ± 1.0	241 ± 19	30.8
Pre-amp. and driver in pixel	3.8 ± 0.2	133.7 ± 0.6	178 ± 9	23.4
All f.e. in pixel	5.4 ± 0.4	148 ± 1.0	228 ± 20	27.1



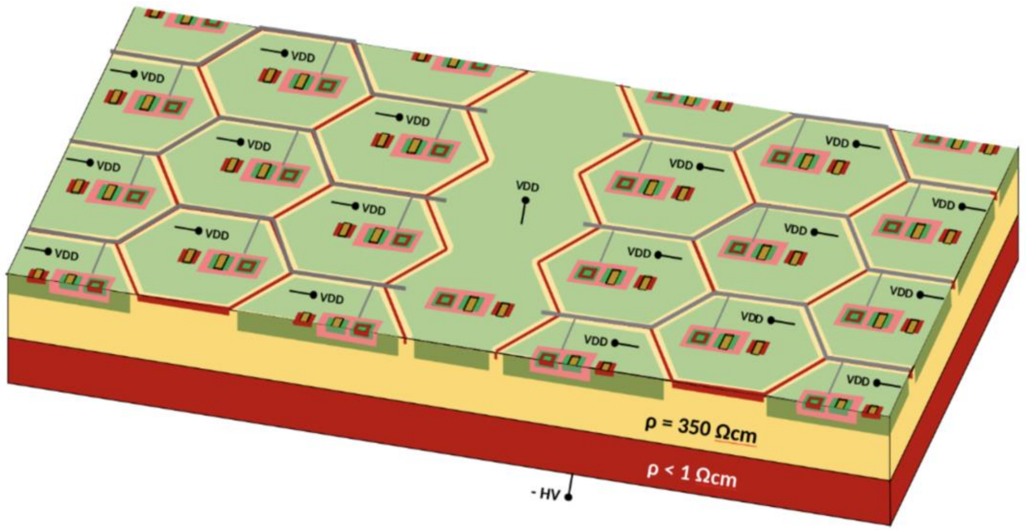
- The **last two configurations** represent a good compromise between comptacness and performance
- Configurations integrated in the pre-production chip

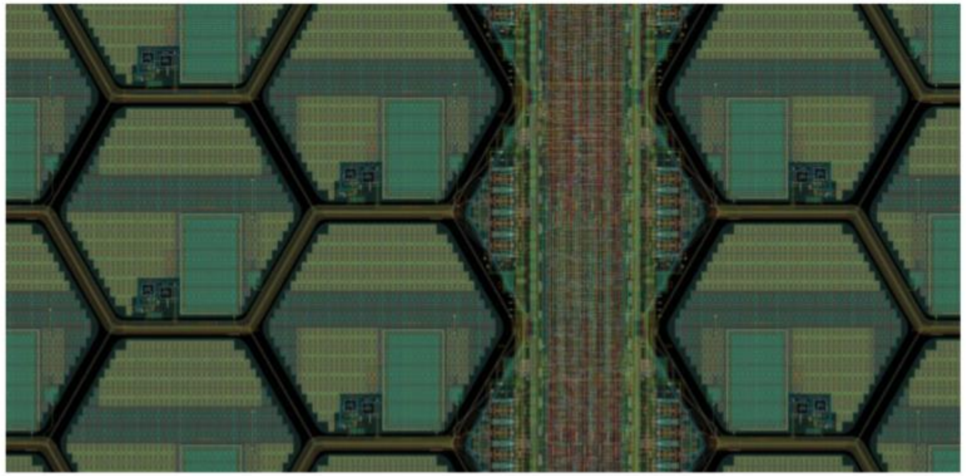
Sensor Cross Section

- Low resistivity heavily p-doped substrate as a support
- Negative high voltage applied to the substrate

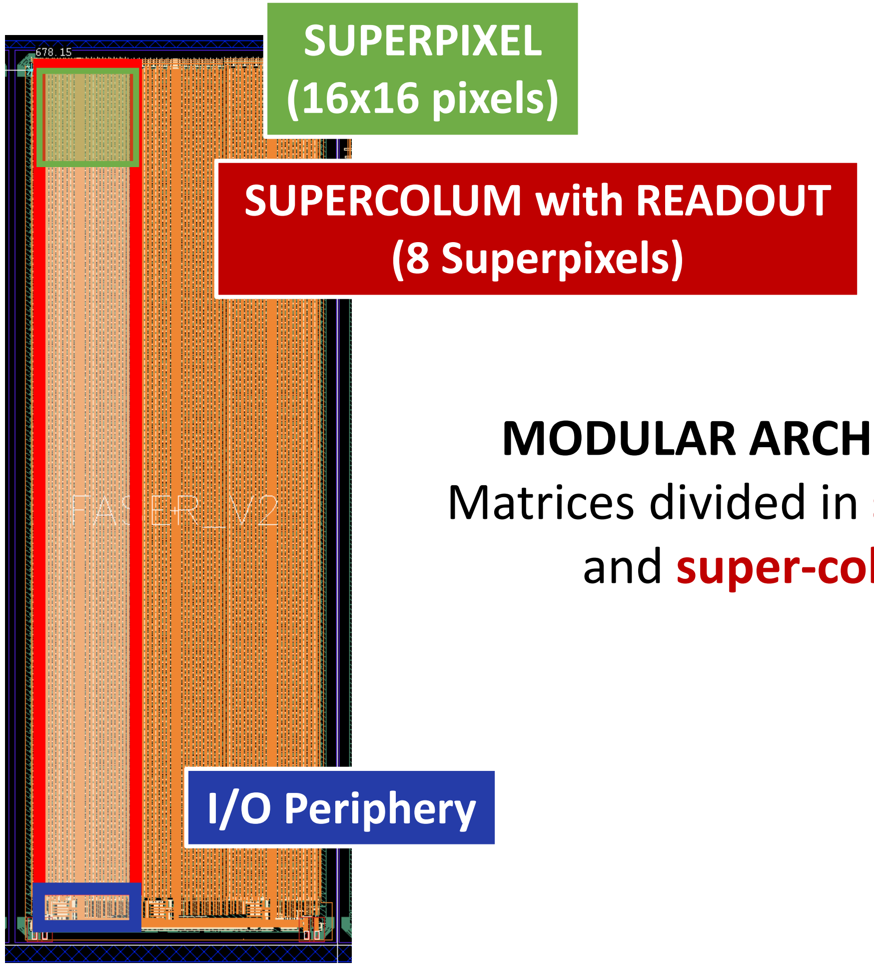
- Triple – well design
- **Analog electronics inside the pixel**
- **Digital electronics outside the pixel**
- Electronics inside the guard ring isolated from substrate using a deep n-well
- Digital electronics in a separate well
- Positive low voltage applied to pixels and electronics deep n-wells

- ≈ 6% dead area in the pixel matrix

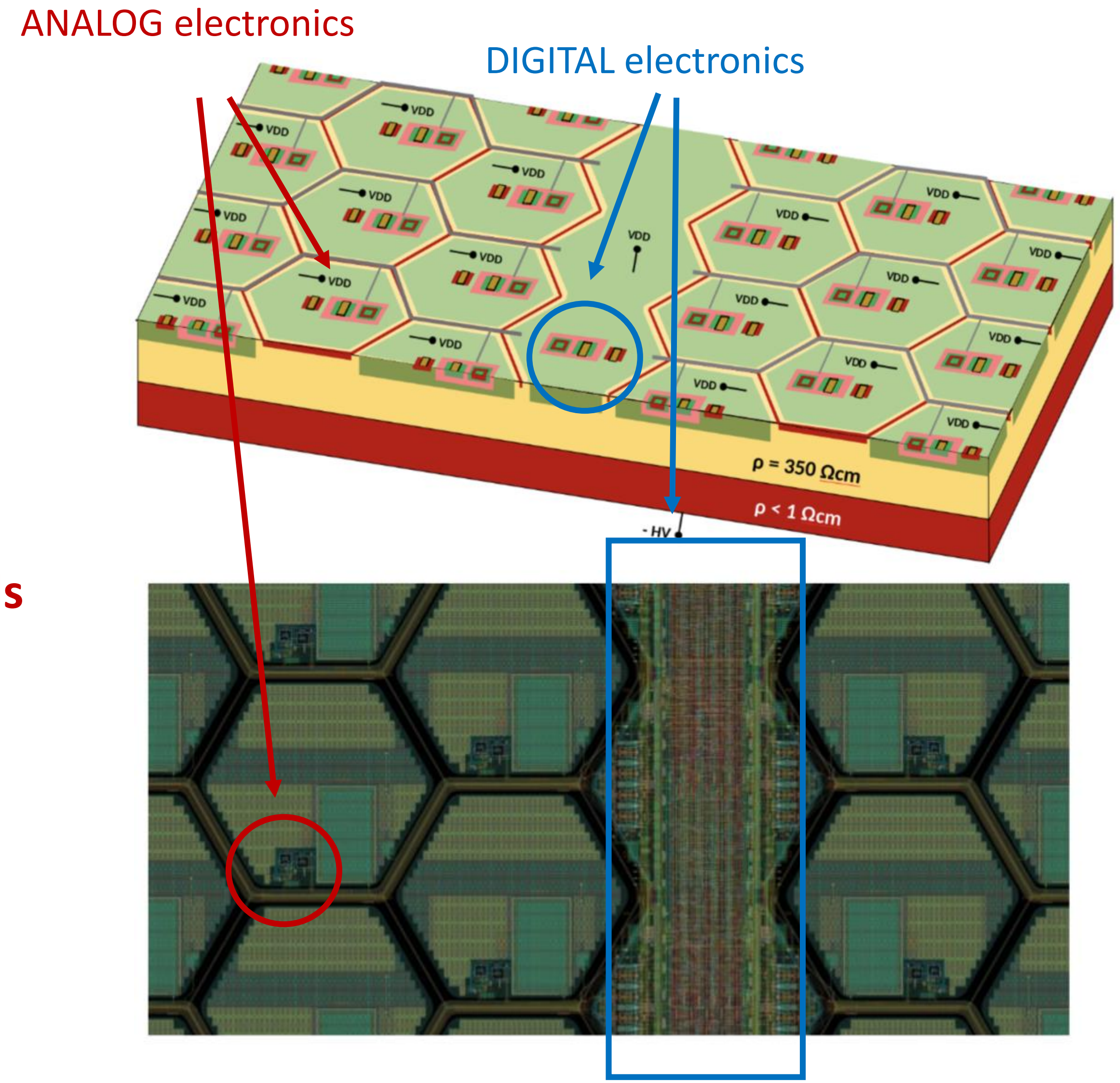




The Chip Architecture

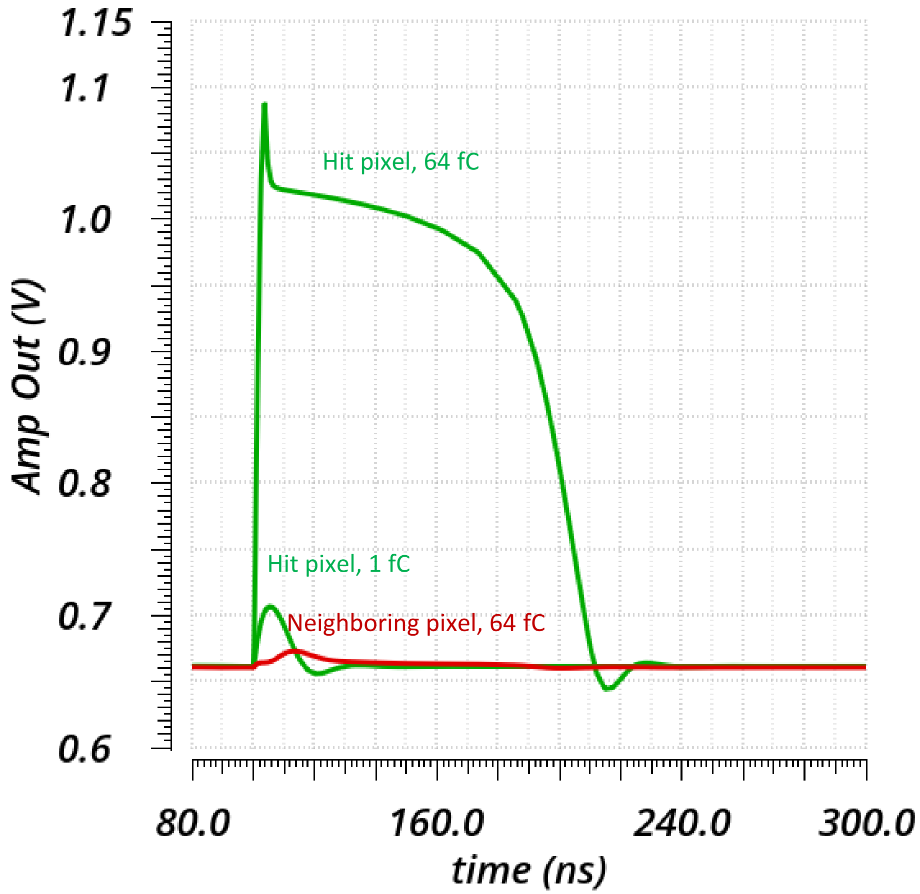


MODULAR ARCHITECTURE
Matrices divided in **super-pixels** and **super-columns**



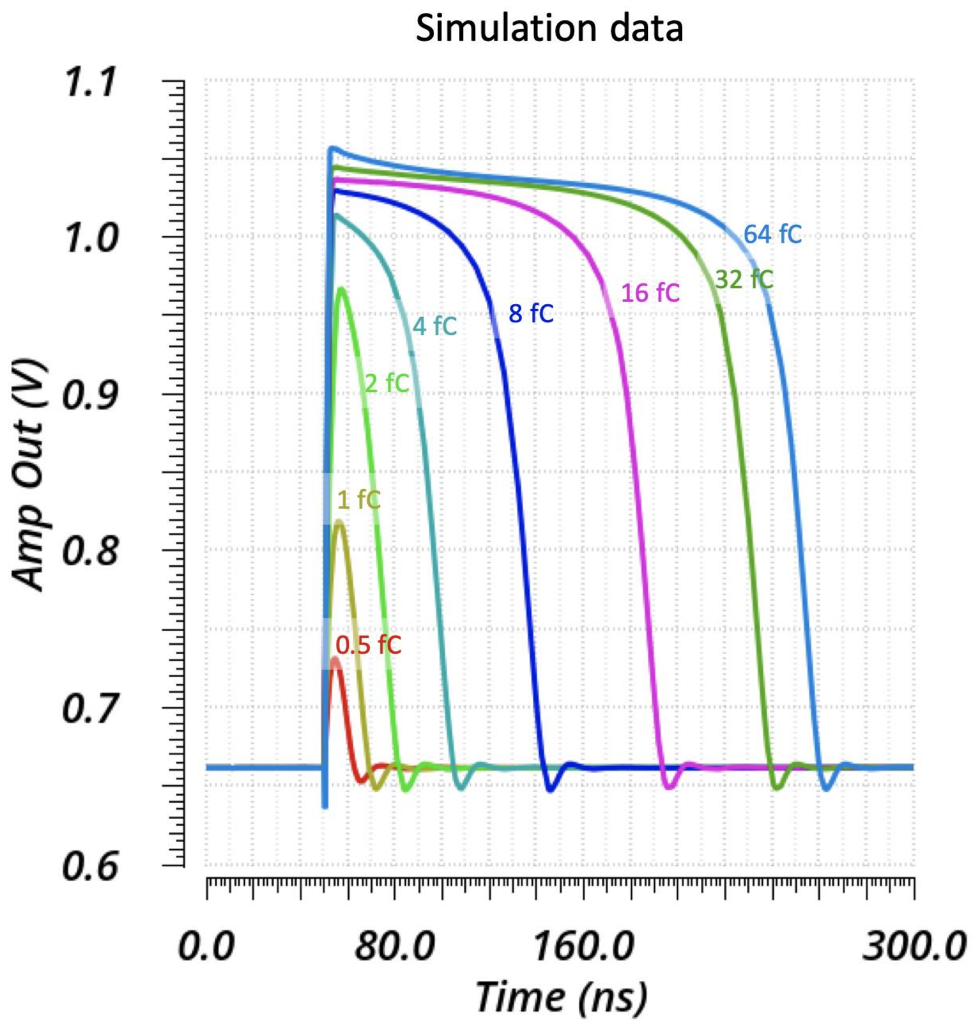
Signal Routing and Crosstalk Suppression

- Signal routed in a **shielded bus** to **minimize crosstalk between neighboring pixels**
- Big signal produced by a 64 fC charge (in green)
- Signal induced in the neighbouring pixel (in red)
  - **Crosstalk is supressed but not eliminated**
  - The signal produced by a 1 fC charge is small but still bigger than the induced signal
  - Threshold set accordingly to 0.5 – 1 fC

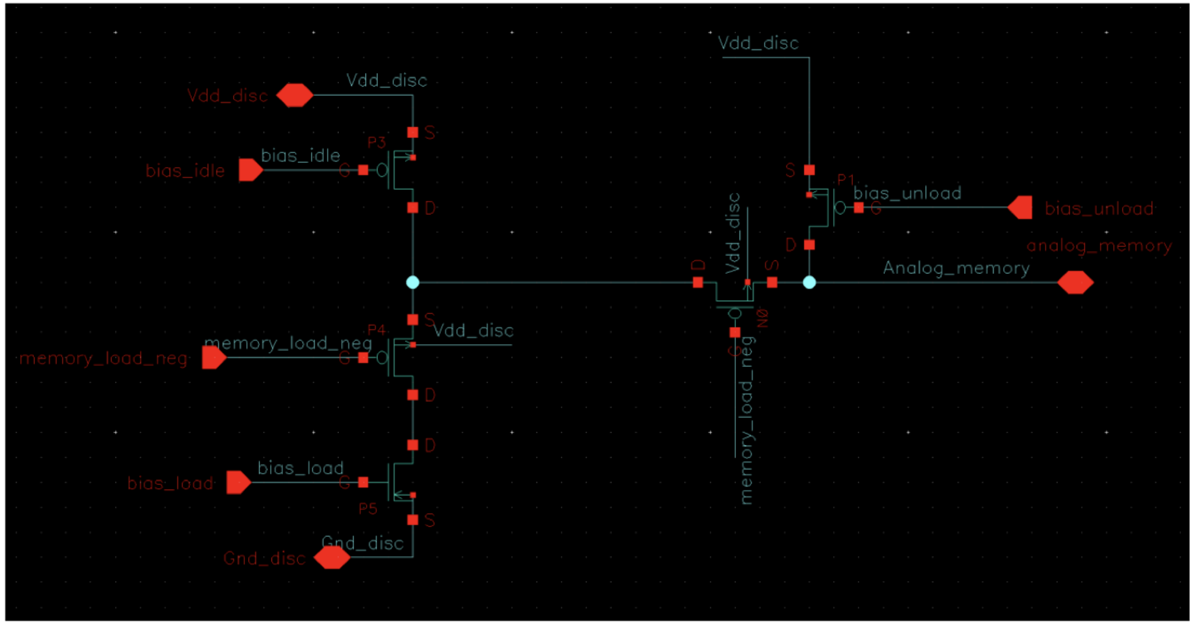


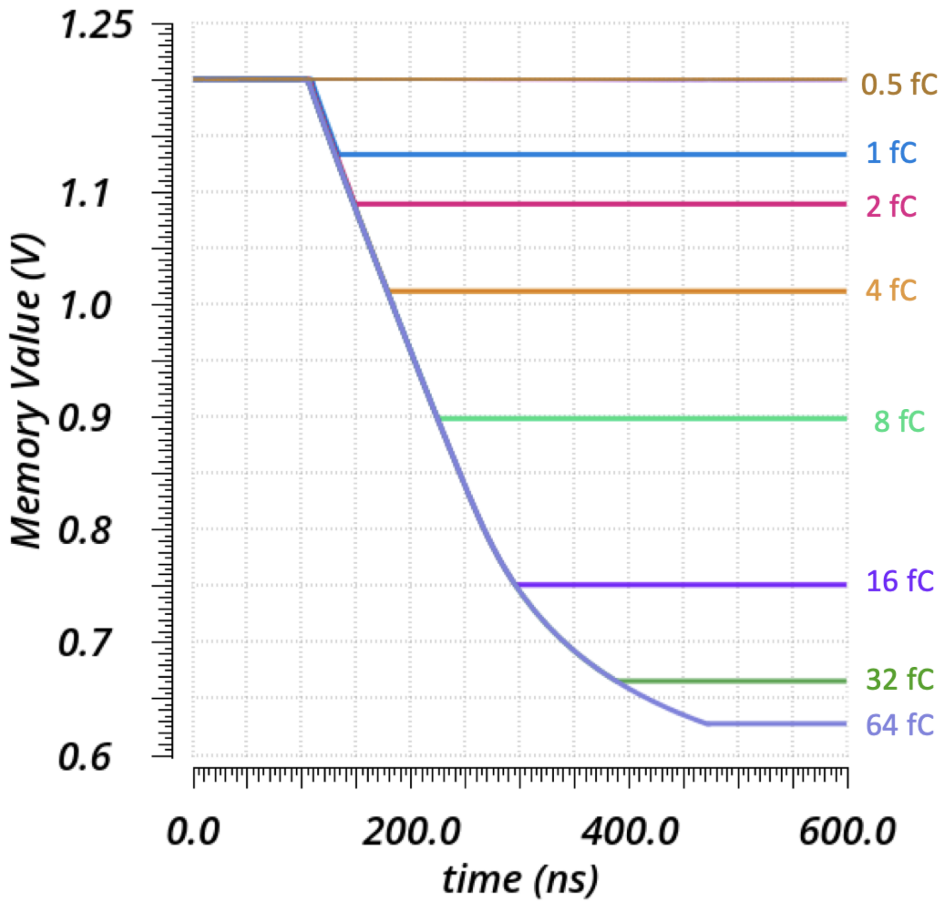
Amplification Stage

- Since we want to measure high charges we convert the charge information to Time Over Threshold
- **For different charges, if the charge increases also the TOT increases but not linearly (almost logarithmic relation)**
- **Saturation at 64 fC (intrinsic saturation of the pixel)**



Memory Control and Analog Memories





- Current leakage even if the switch is opened. It takes 200 µs to degradate the memory value of 30 mV (= 1 bin of our ADC).

After 200 µs we still measure something but we are less precise