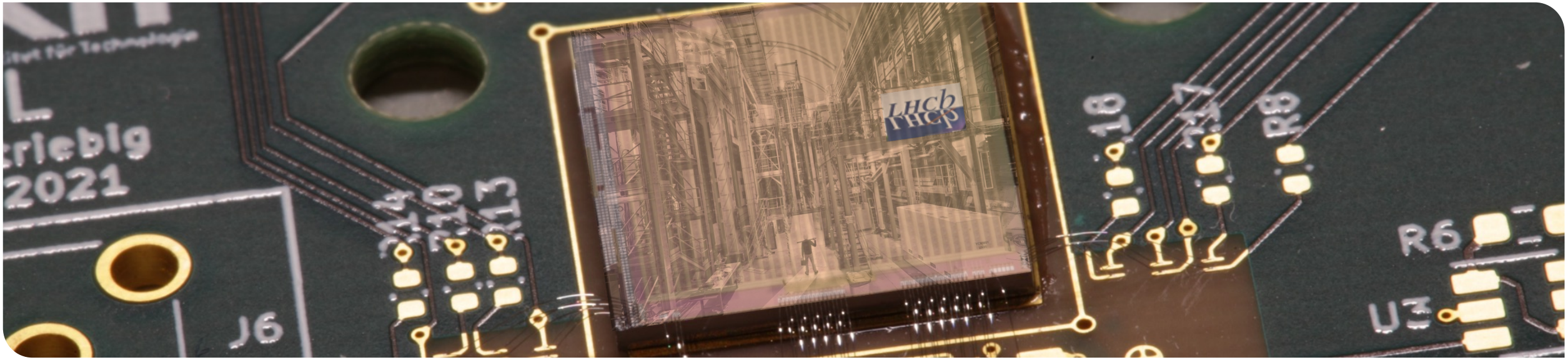
Karlsruhe Institute of Technology

KIT ASIC and Detector Laboratory

MightyPix: A HV-CMOS Pixel Chip for LHCb's Mighty Tracker

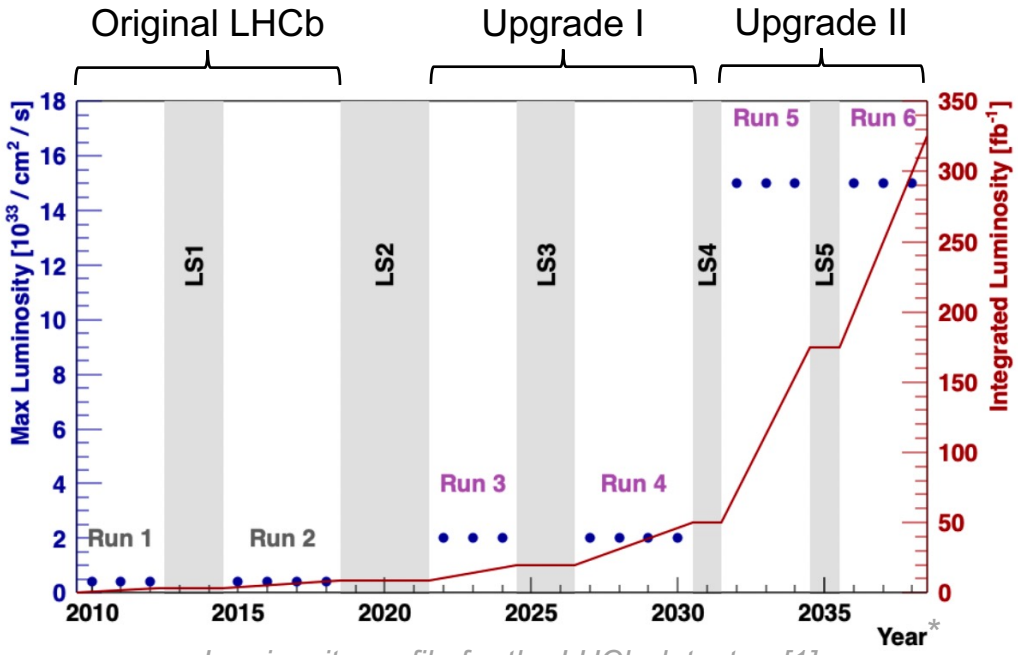
Sigrid Scherl

sigrid.scherl@kit.edu



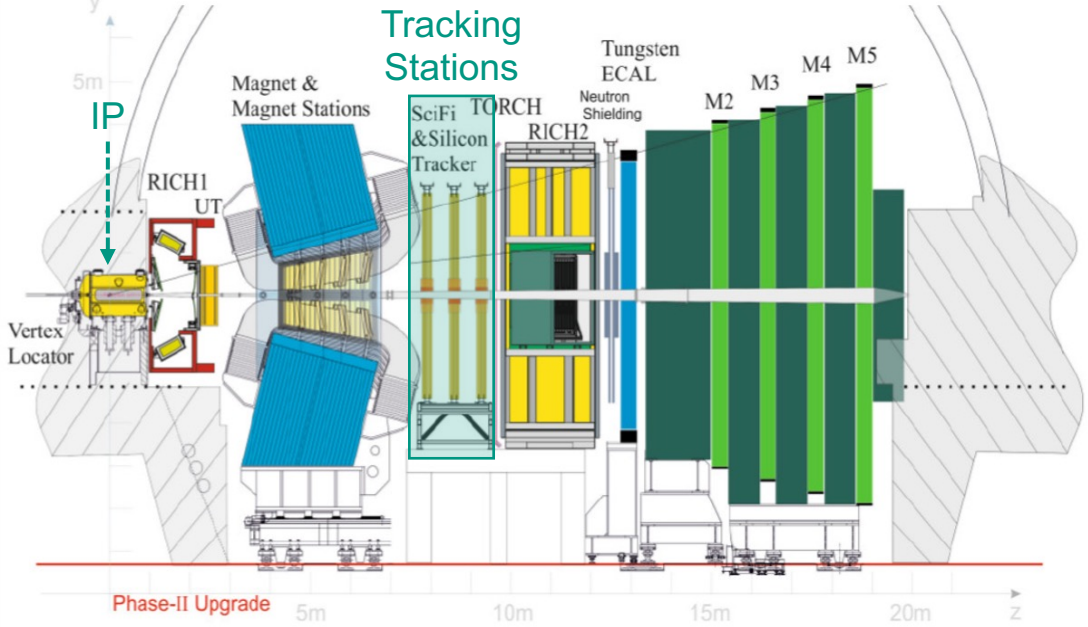
LHCb Upgrade towards HL-LHC

- Upgrade II: $\mathcal{L}_{\max} = 1.5 \times 10^{34} \mathrm{cm}^{-2}\mathrm{s}^{-1}$
- Increased readout speed of 40 MHz BX rate
- New software-only trigger



Luminosity profile for the LHCb detector. [1]
** Pushed back a bit now*

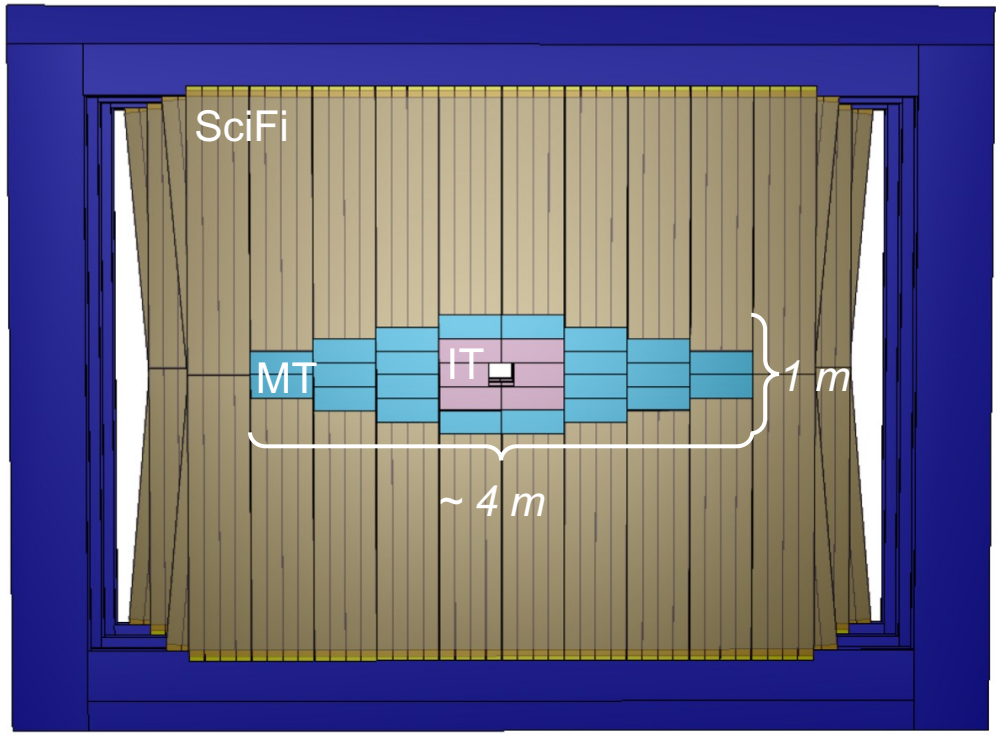
- New tracking stations
- Proposed hybrid tracker **Mighty Tracker**
- Composed of *SciFi Tracker*, *Inner* and *Middle Tracker*



Schematic side view of the Upgrade II LHCb detector. [1]

Mighty Tracker

- **SciFi Tracker**: Scintillating fibres with SiPM readout
- **Inner Tracker** and **Middle Tracker**
  - Silicon sensors meet requirements of radiation hardness and granularity
  - Baseline technology: HV-CMOS pixel chip **MightyPix**
  - In total over 46000 silicon sensors to cover area of 18 m^2 (six layers with 3 m^2 each)



Schematic of one layer of the Mighty Tracker. [1]

Schedule from January 2022. [2]

Installation of SciFi

Replacements for SciFi, installation of Inner Tracker

Installation of Middle Tracker

MightyPix

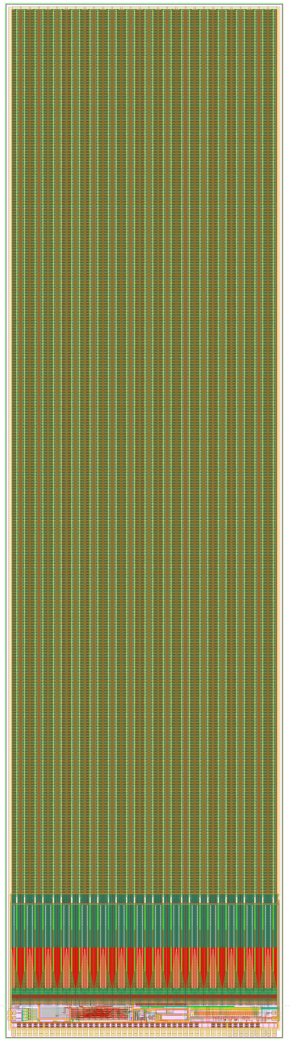
- Based on knowledge from ATLASPix[1] and MuPix[2]
- Final design parameters and requirements:
  - Good granularity
  - Good time resolution
  - Lower power consumption
  - Radiation hard
  - Cooled to under 0°C
- First prototype: **MightyPix1**

Parameter	Required Value
Chip size	$\sim 2\ \mathrm{cm} \times 2\ \mathrm{cm}$ *(Limited by reticle size)*
Pixel size	$\sim 150\ \mu\mathrm{m} \times 50\ \mu\mathrm{m}$
Time resolution	$< 3\ \mathrm{ns}$ *(Hit assigned to right BX)*
Power consumption	$< 0.15\ \mathrm{W/cm^2}$
NIEL[3]	$6 \times 10^{14}\ 1\ \mathrm{MeV}\ \mathrm{n_{eq}/cm^2}$ *(Includes safety factor of 2)*
Cooling	$< 0°\mathrm{C}$ *(Test beam studies)*

[1] *HV-CMOS pixel chip originally developed for CERN's ATLAS experiment*
[2] *HV-CMOS pixel chip for the Mu3e experiment at PSI*
[3] *Non Ionising Energy Loss*

MightyPix1: Overview

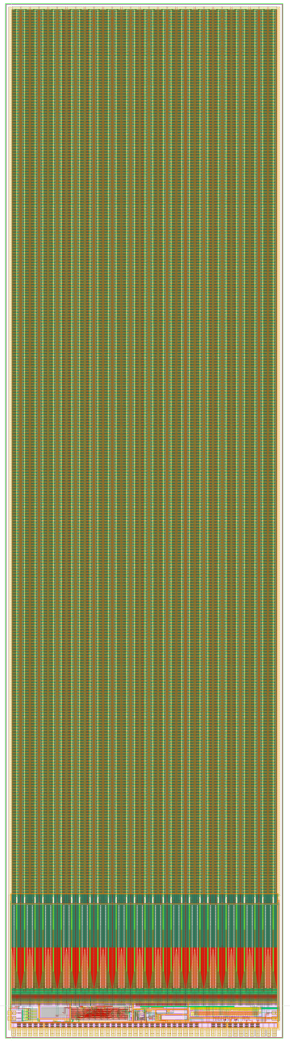
- **Implemented** in TSI 180 nm process
- **Submitted** in May 2022, came back in December
- **Chip size:** ~ 2 cm × 0.5 cm → full column length, ¼ width
- **Pixel matrix:** 29 columns, 320 rows
- **Pixel:** 165 µm × 55 µm with CMOS amplifier and CMOS comparator



The first prototype: MightyPix1

MightyPix1: Overview

- **Data format:** 2 × 32 bit words per hit
- **Data output rate:** 1.28 Gbit/s going to lpGBT
- **Digital interfaces:** Timing and Fast Control (TFC), Slow Control (I2C), configuration shift register (SR) interface
- **External clocks:** 40 MHz and 640 MHz coming from lpGBT
- **Internal clocks:** CML and CMOS PLL with 40 MHz reference clock
- **Bias voltages:** Integrated 10 bit voltage DACs, can be supplied externally

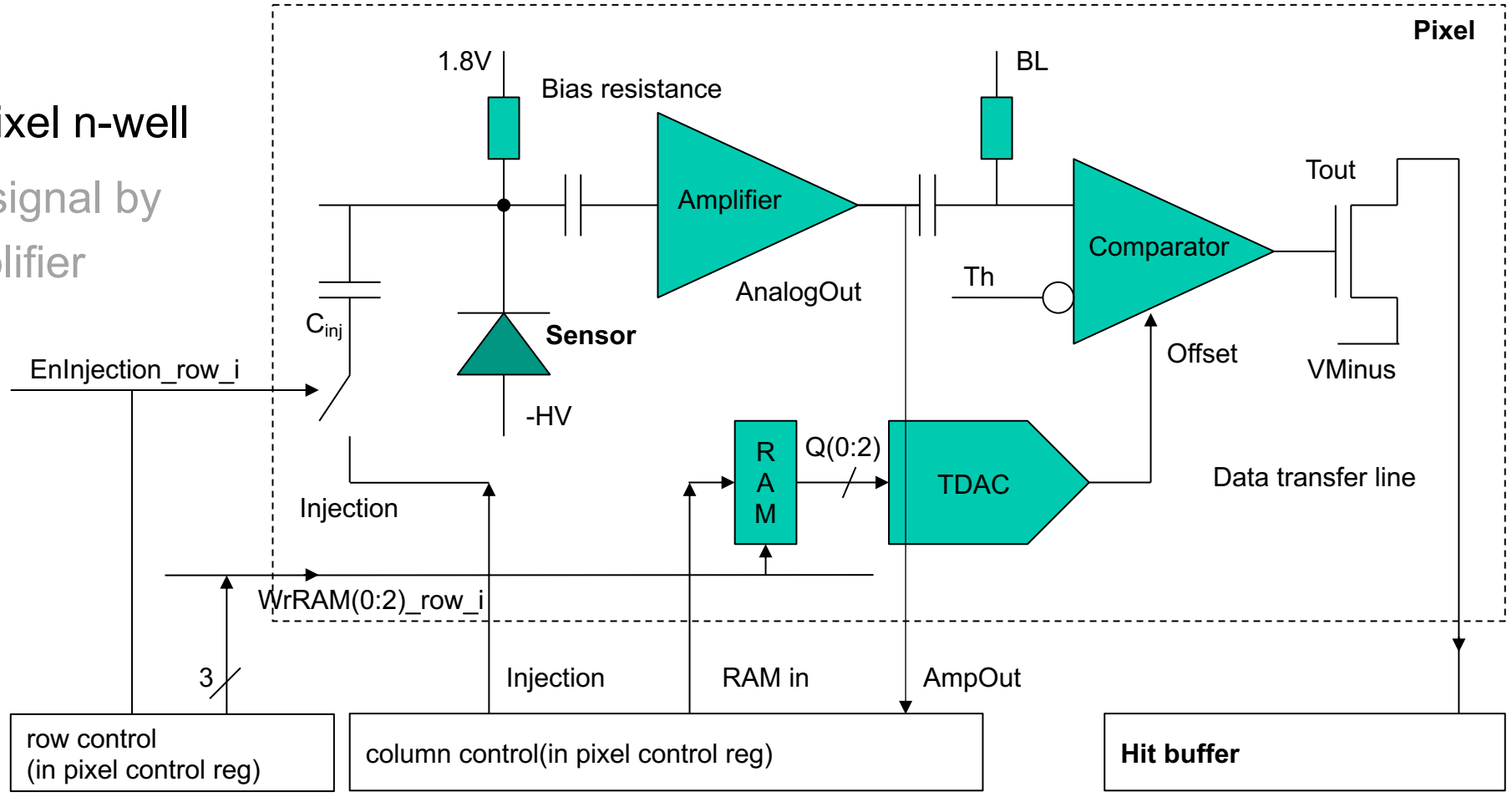


The first prototype: MightyPix1

MightyPix1: Analogue Part

Working principle:

1. Charge collected by pixel n-well
2. Converted to voltage signal by Charge Sensitive Amplifier
3. Analog voltage pulse shaped and converted to digital signal by comparator
4. Hit information stored in hit buffer

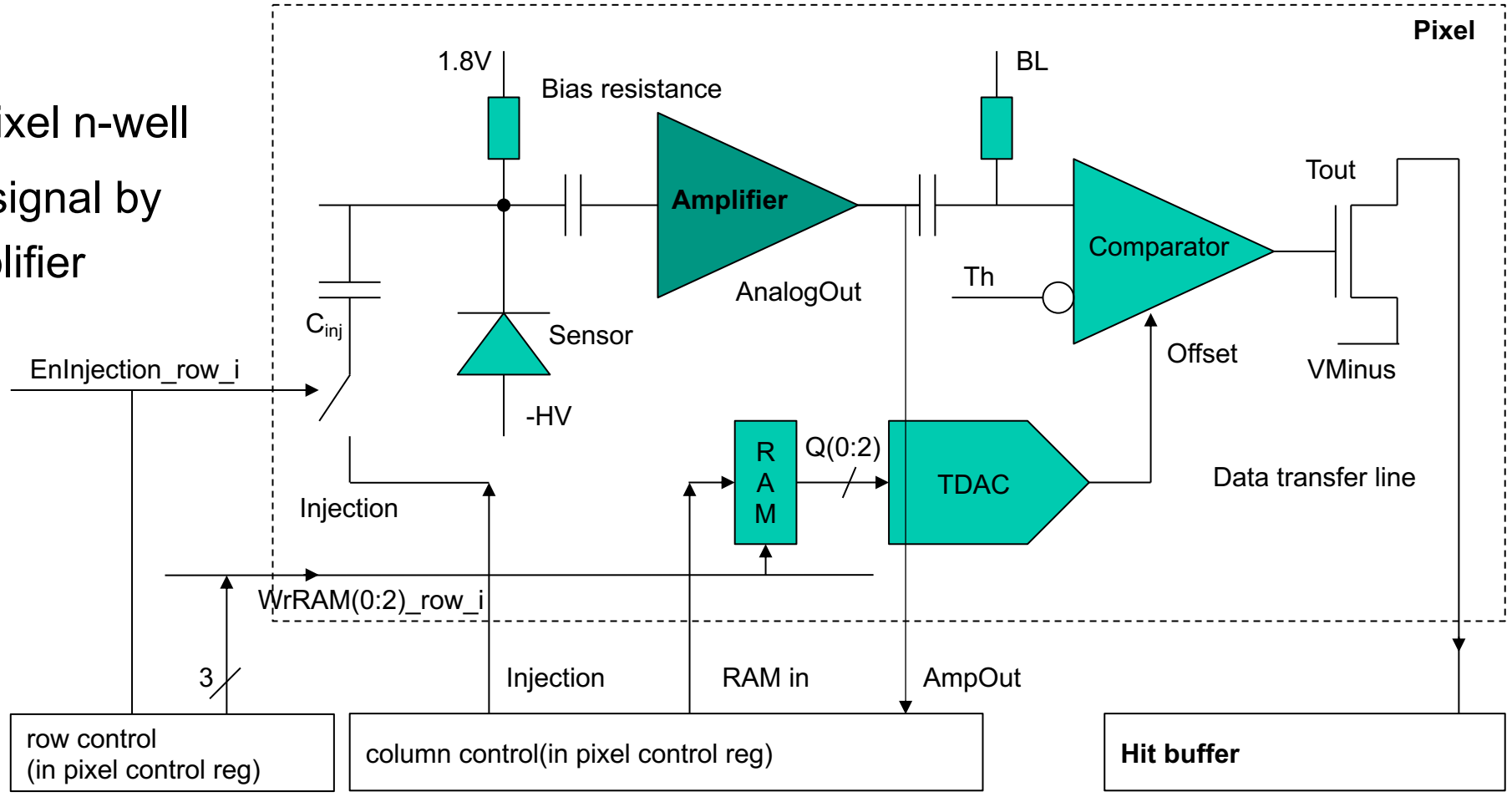


Source: Ivan Perić

MightyPix1: Analogue Part

Working principle:

1. Charge collected by pixel n-well
2. Converted to voltage signal by Charge Sensitive Amplifier
3. Analog voltage pulse shaped and converted to digital signal by comparator
4. Hit information stored in hit buffer

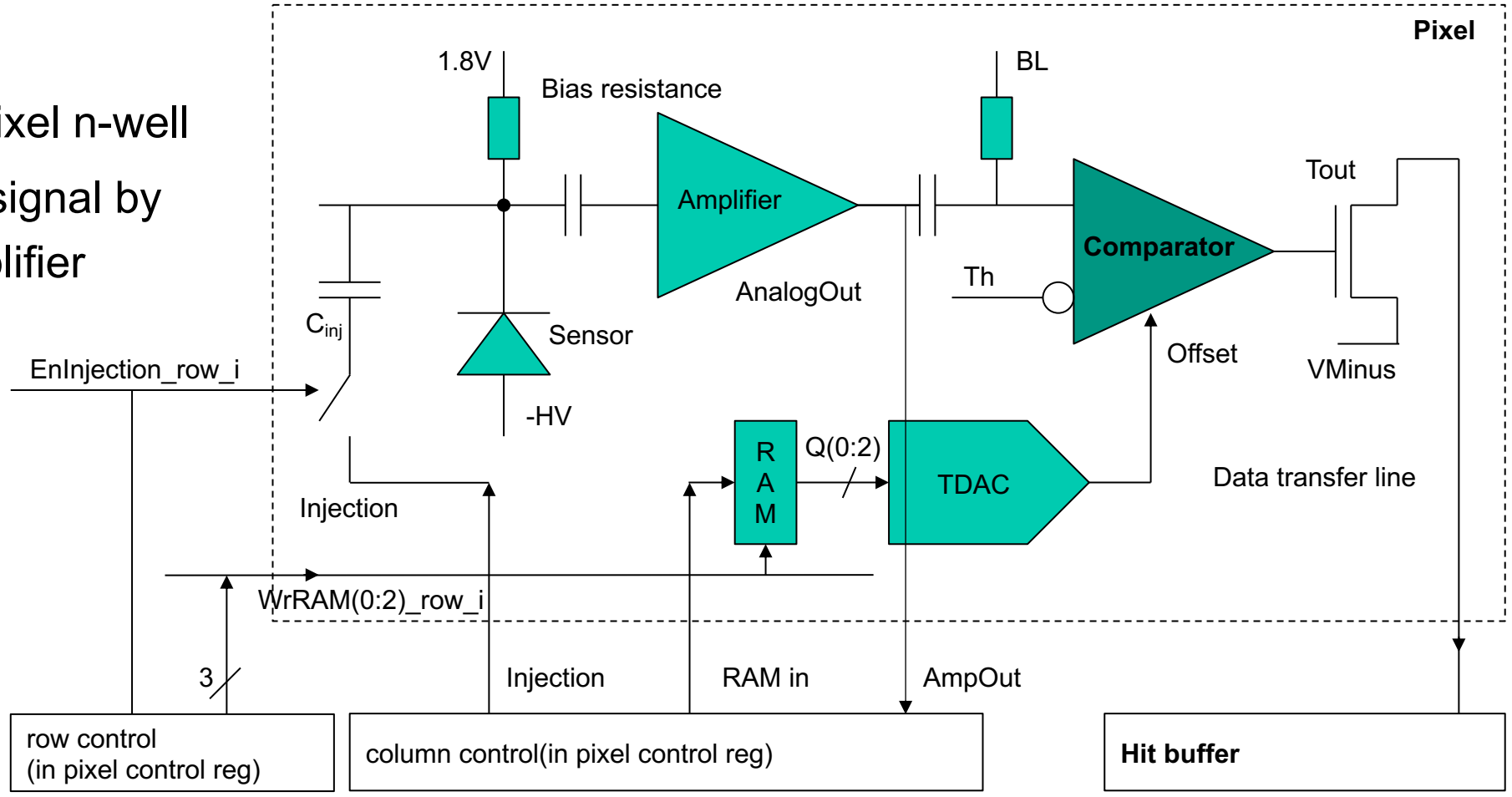


Source: Ivan Perić

MightyPix1: Analogue Part

Working principle:

1. Charge collected by pixel n-well
2. Converted to voltage signal by Charge Sensitive Amplifier
3. Analog voltage pulse shaped and converted to digital signal by comparator
4. Hit information stored in hit buffer

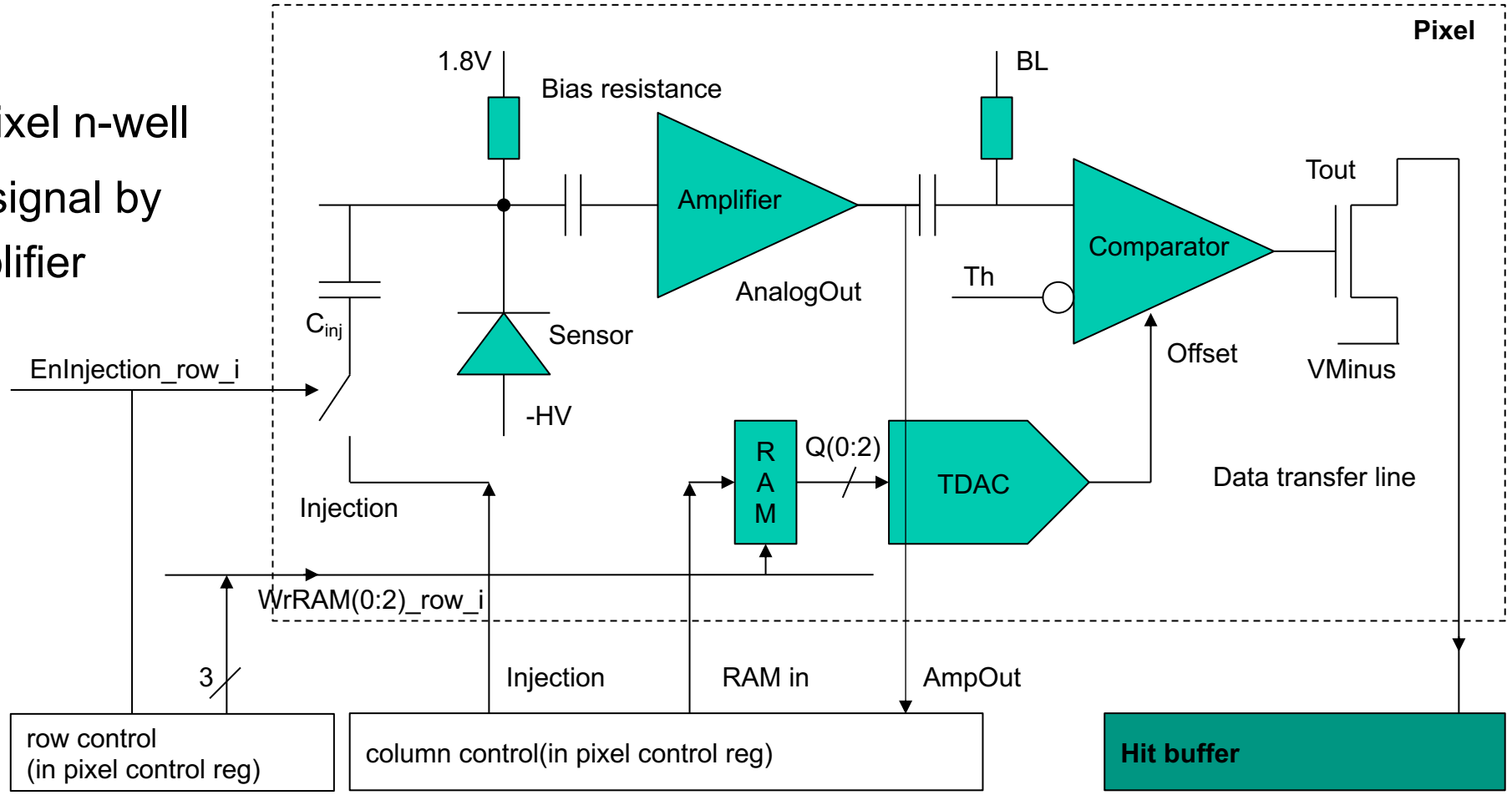


Source: Ivan Perić

MightyPix1: Analogue Part

Working principle:

1. Charge collected by pixel n-well
2. Converted to voltage signal by Charge Sensitive Amplifier
3. Analog voltage pulse shaped and converted to digital signal by comparator
4. Hit information stored in hit buffer



Source: Ivan Perić

MightyPix1: Efficiency Simulation

- *Can MightyPix handle the particle hit rate at LHCb?*
- When a pixel is hit by a particle, it cannot detect another hit until first one is read out

- Quantify performance through

$$\text{efficiency} = \frac{\text{detected events}}{\text{total events}}$$

- Expected rate in hottest region of Mighty Tracker: 1.7 hits per event[1] and chip[2] with additional 5% of clusters with two pixels
- Have MC simulated data based on old SciFi geometry
- Use model of MightyPix1 pixel matrix to check efficiency

[1] Within 25 ns window
[2] With size of 2 cm × 2 cm

MightyPix1: Efficiency Simulation

- Check how many hits are detected correctly for expected rate

Expected rate: 1.7 hits per 25 ns and 2 cm x 2 cm chip

Readout Speed	40 MHz
Rate	*Expected*
Simulated Hits	1166
Missing Hits	9
Efficiency	*99.23%*

MightyPix1: Efficiency Simulation

- How about for twice the expected amount of incoming particles?

Expected rate: 1.7 hits per 25 ns and 2 cm x 2 cm chip

Twice expected rate: 3.4 hits per 25 ns and 2 cm x 2 cm chip

Readout Speed	40 MHz	
Rate	*Expected*	*2 x exp.*
Simulated Hits	1166	2322
Missing Hits	9	105
Efficiency	*99.23%*	*95.48%*

MightyPix1: Efficiency Simulation

- Analysis shows that missing particle hits fall into readout time of previous hit
  → Increase readout speed

Expected rate: 1.7 hits per 25 ns and 2 cm x 2 cm chip

Twice expected rate: 3.4 hits per 25 ns and 2 cm x 2 cm chip

Readout Speed	**40 MHz**		**160 MHz**	
Rate	*Expected*	*2 x exp.*	*Expected*	*2 x exp.*
Simulated Hits	1166	2322	1166	2322
Missing Hits	9	105	7	16
Efficiency	*99.23%*	*95.48%*	*99.40%*	*99.31%*

MightyPix1: Efficiency Simulation

- **Results:**
  - MightyPix can handle expected particle hit rate → efficiency over 99% in hottest region
  - Missing particle hits fall into readout time of previous hit
  - Could handle higher rate if readout speed is increased

Readout Speed	40 MHz		160 MHz	
Rate	*Expected*	*2 x exp.*	*Expected*	*2 x exp.*
Simulated Hits	1166	2322	1166	2322
Missing Hits	9	105	7	16
Efficiency	*99.23%*	*95.48%*	*99.40%*	*99.31%*

Summary

- Proposed new tracker for LHCb: **Mighty Tracker**
  → to be instrumented with 18 m^2 of silicon sensors
- First prototype **MightyPix1**
  - Submitted in May 2022, wafers are currently being diced
  - Compatible with LHCb readout
  - Able to handle highest expected hit rates
- What's next?
  - Measure MightyPix1
  - Design MightyPix2

References

[1] CERN/LHCC 2021-012
(*https://cds.cern.ch/record/2776420*)

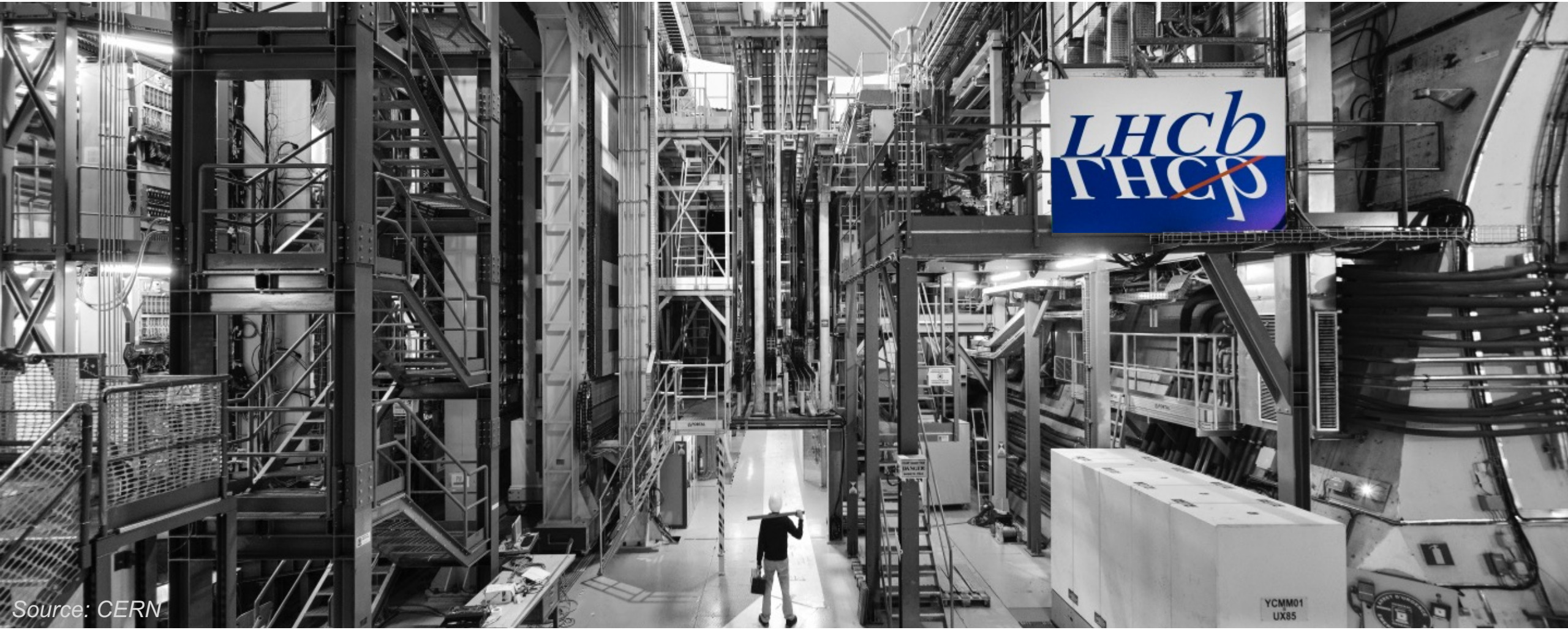
[2] https://lhc-commissioning.web.cern.ch/schedule/LHC-long-term.htm
(*Accessed 23/9/2022*)

[3] CERN-LHCb-PUB-2022-003
(*https://cds.cern.ch/record/2800986?ln=en, publication pending*)

[4] H. Augustin et al. *The MuPix sensor for the Mu3e experiment.* Nucl. Instrum. Meth. A, 979:164441, 2020.

[5] https://commons.wikimedia.org/wiki/File:Normal_Distribution_Sigma.svg

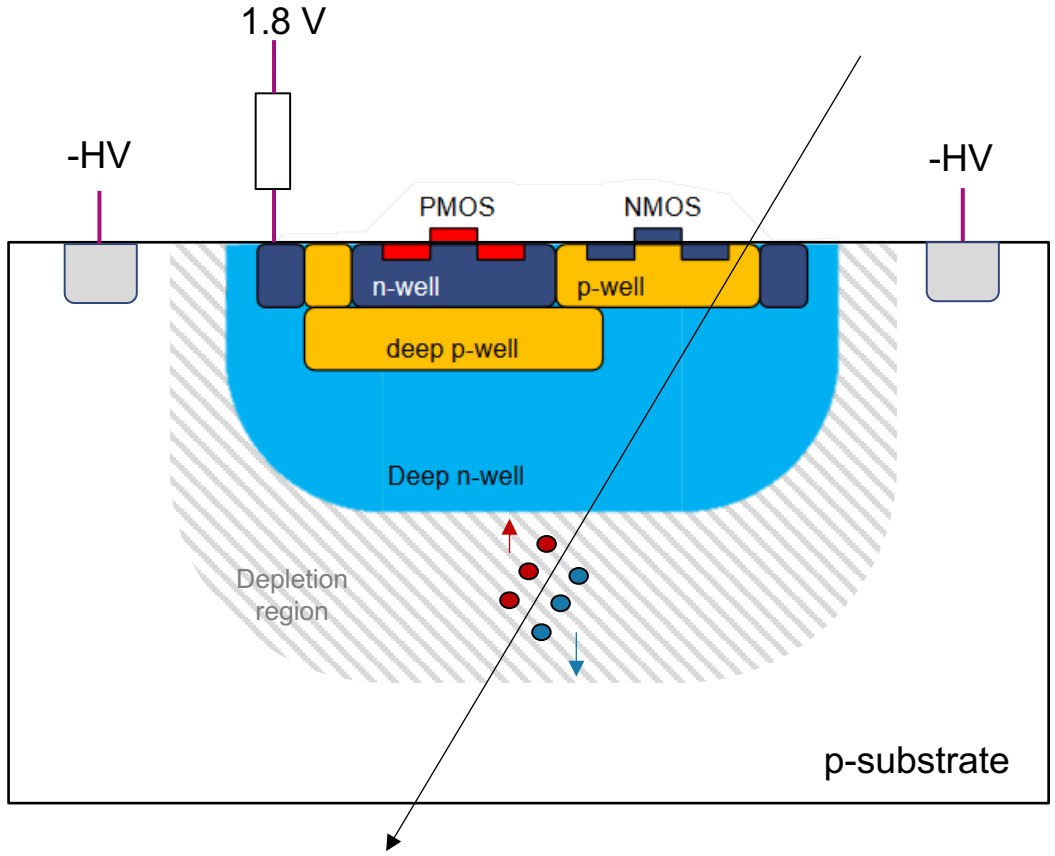
Backup



Source: CERN

HV-CMOS

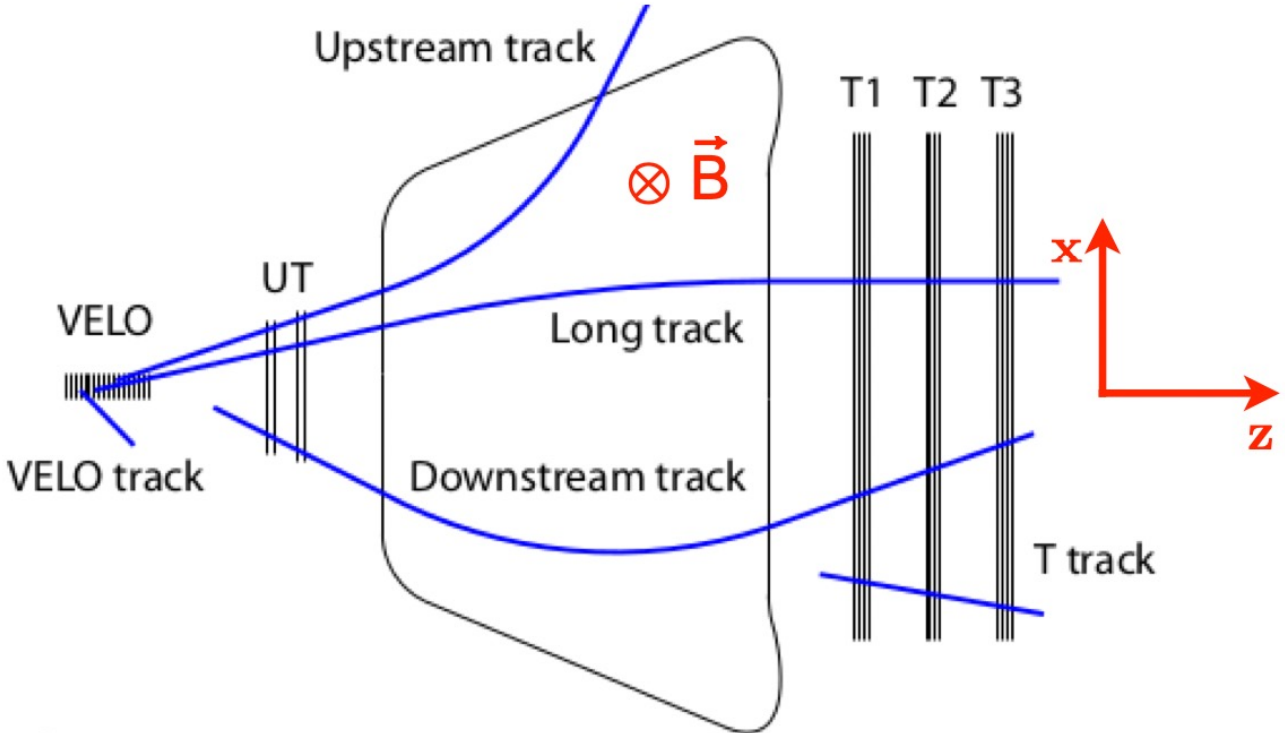
- Sensing element and readout circuit on same chip
- n-well/p-substrate diode acts as sensor
- Readout electronics isolated from high voltage by deep n-well
- High reverse bias creates thick depletion region between deep n-well and p-substrate
- Photons and ionising particles create electron/hole pairs, collected via drift



Working principle of HV-CMOS sensors.

Purpose of the Mighty Tracker

- Tracking stations T1 – T3 downstream of the magnet
- Crucial to provide info on particle momenta with VELO and Upstream Tracker (UT)



Source: Fred Blanc, FCC Workshop, 12/11/2020

MightyPix1: TFC Signals

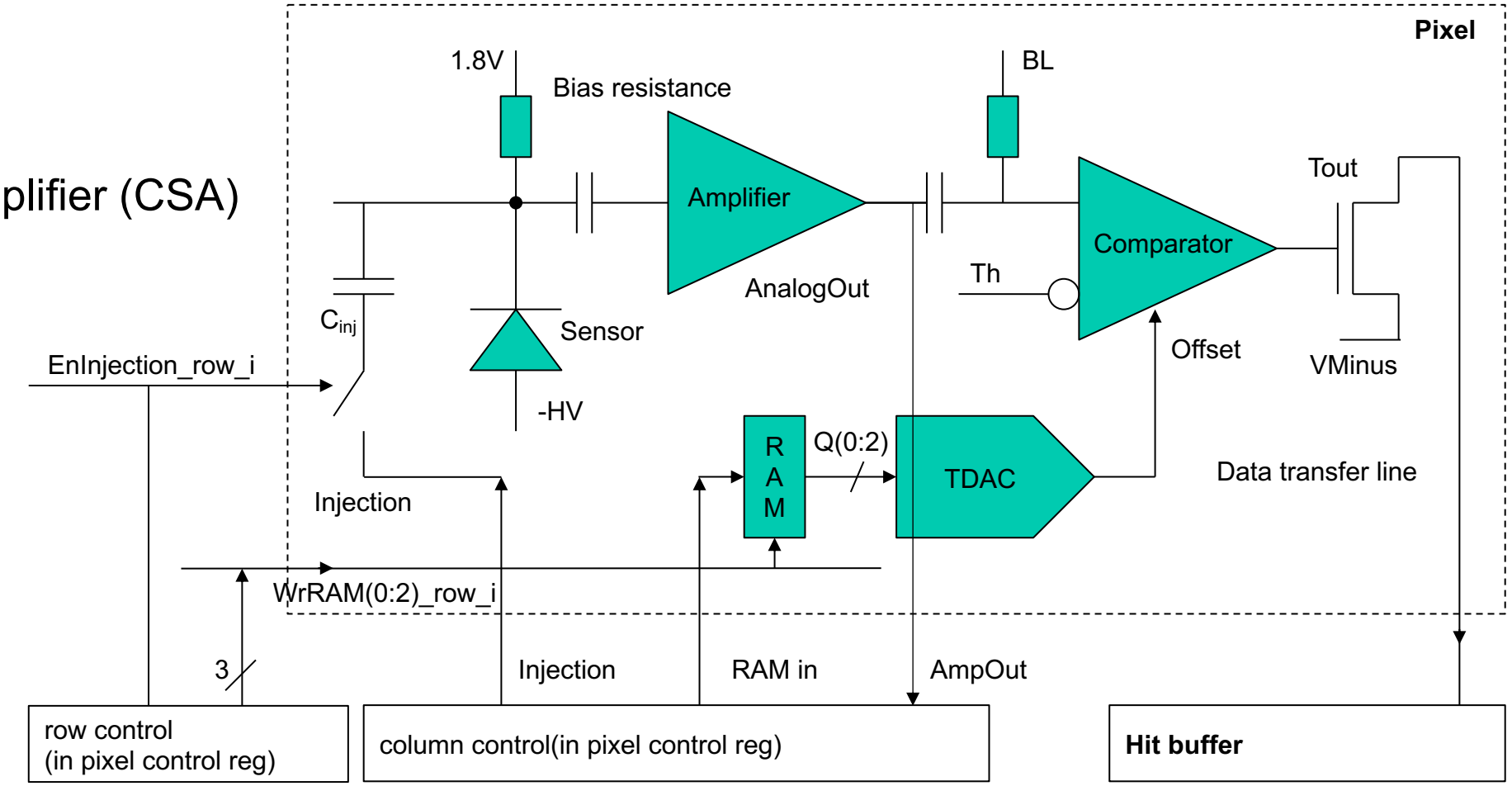
- LHCb sends Timing and Fast Control (TFC) signals to all FE modules

- **BXReset:** Reset internal BXcounter to synchronise chips to same BX
- **Snapshot:** Capture number of received TFC commands *(partially implem.)*
- **FEReset:** Reset all modules except for TFC receiver, BXcounter and chip configuration registers
- **Cal:** Could be used to control an on-chip injection circuit *(not yet implem.)*
- **Sync:** Chip outputs sync pattern, configurable via configuration register

MightyPix1: Analogue Part

Pixel contains:

- Sensor diode
- Charge Sensitive Amplifier (CSA)
- Comparator
- Threshold tune DAC
- RAM for tune bits



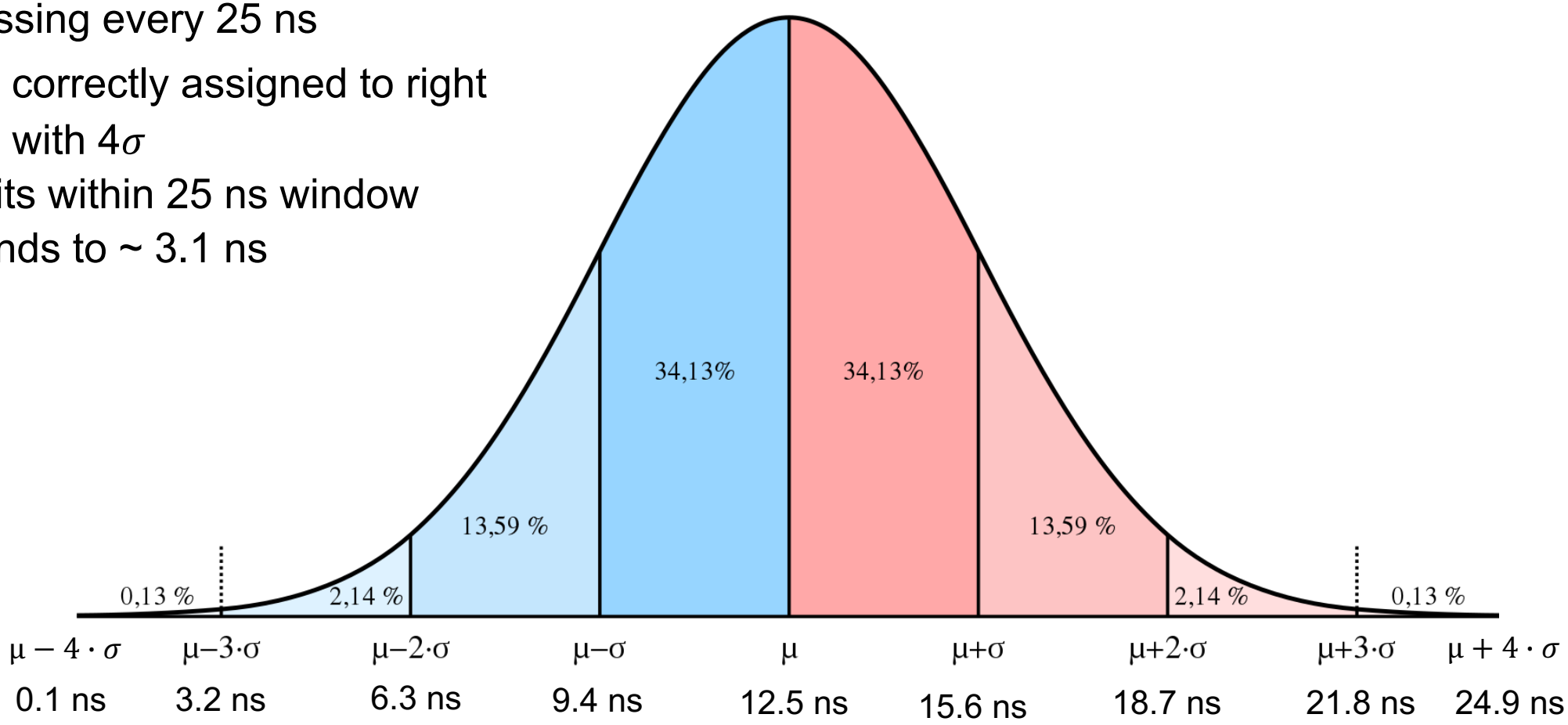
Source: Ivan Perić

MightyPix1: Digital Readout

- Readout Control Unit (RCU) FSM
- Working principle:
  - Data busses discharged
  - Data loaded from highest active hit buffer to EoC buffer, go on to next one
  - Read data from EoC
  - For every hit 2 × 32 bit data words
  - Parallel scrambler analogue to VELOPix
  - Data sent into serializer tree

Why do we need a time resolution of < 3 ns?

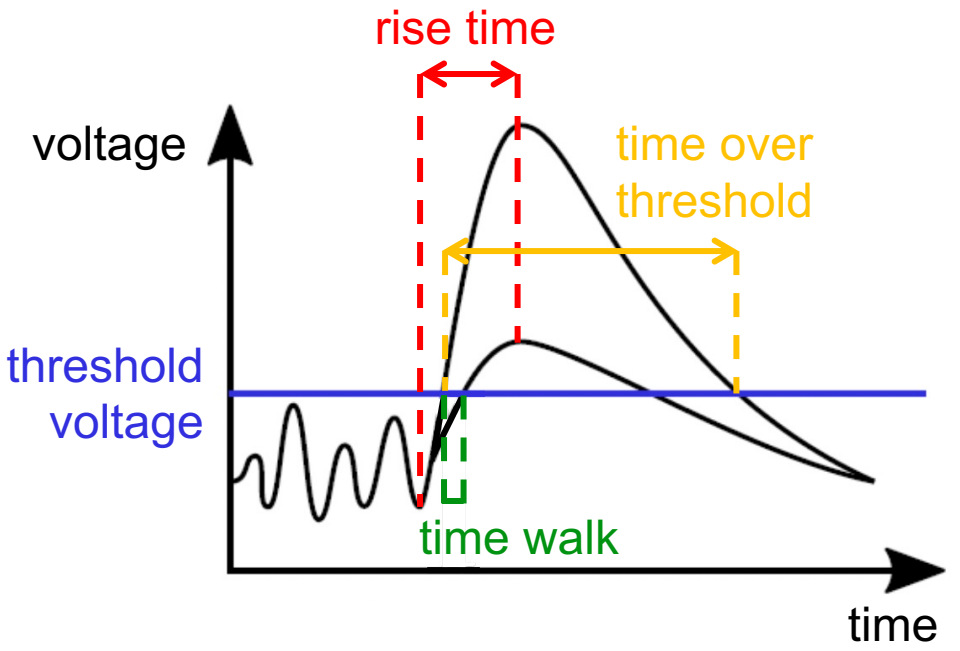
- One bunch crossing every 25 ns
- Hits need to be correctly assigned to right bunch crossing with 4σ
  → 99.99% of hits within 25 ns window
  → 1σ corresponds to ~ 3.1 ns



Normal distribution. [5]

MightyPix1: Time Walk and ToT

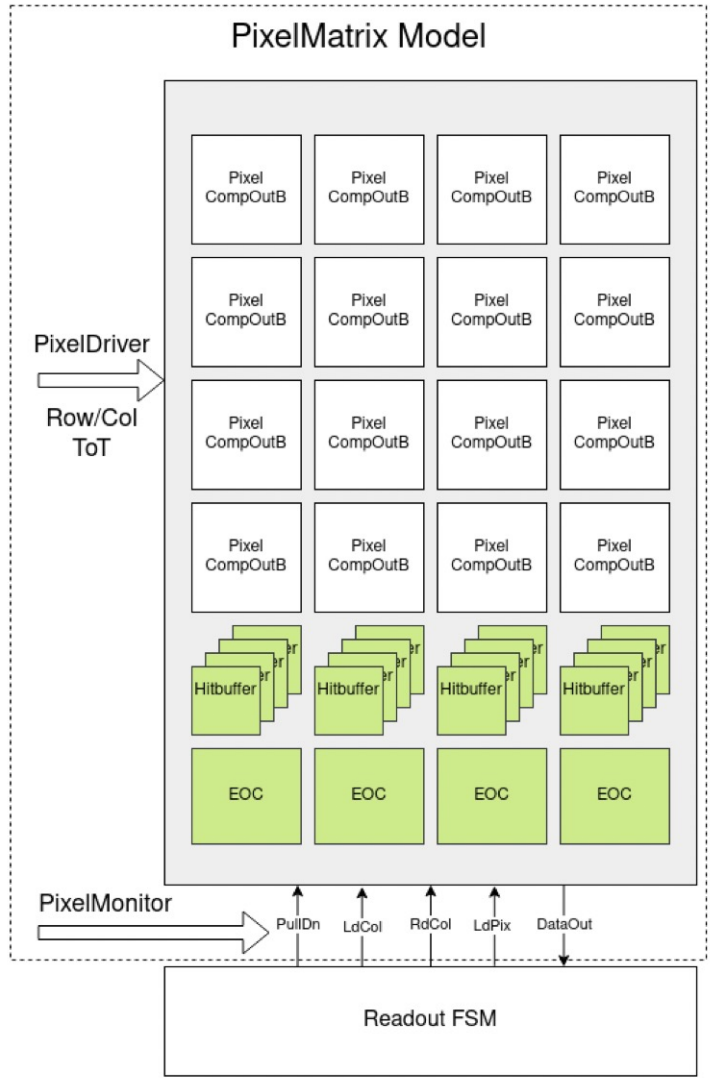
- **Time walk:**
  - Rise time same for all signals
  - Difference in time at which threshold is crossed is called time walk
  - Time walk ~ 2.5 ns for signals of 2500 e^- and 25000 e^-
- **Time over Threshold:**
  - 1.5 µs to 2 µs
  - Simulations show impact of resulting dead time negligible (*See slides on Efficiency Simulation)*



Schematic description of time walk, rise time, and time over threshold. Adapted from [4].

MightyPix1: Efficiency Simulation

- Data: Simulated physics data from the University of Zurich LHCb group *[3]*
- Model: Parametrizable model of pixel matrix (RCU, hit buffer structure, EoC)
- Comparison of input data with data seen at RCU
- *Why do hits go missing?*
  - Each pixel has one hit buffer
  - Columns scanned left to right and hit info loaded to EoC for each hit buffer
  - If readout takes too long and next hit already occurs before readout it will be missed



Source: Nicolas Striebig

MightyPix1: Efficiency Simulation

Readout Speed	40 MHz				160 MHz	
Clusters	*No*	*No*	*Yes*	*Yes*	*No*	*No*
Rate	*Expected[1]*	*Twice exp. [2]*	*Expected[1]*	*Twice exp. [2]*	*Expected[1]*	*Twice exp. [2]*
Simulated Hits	1166	2322	1223	2437	1166	2322
Missing Hits	9	105	9	122	7	16
Efficiency	*99.23%*	*95.48%*	*99.26%*	*94.91%*	*99.40%*	*99.31%*

[1]Expected particle hit rate: 1.7 hits per 25 ns and 2 cm x 2 cm chip
[2]Twice the particle expected hit rate: 3.4 hits per 25 ns and 2 cm x 2 cm chip