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Vertical Integration System Testing of the CMS HGCAL Electronics

In preparation for the High-Luminosity era of the LHC, the CMS experiment will replace the existing calorimeter endcaps with a novel device - the High Granularity Calorimeter (HGCAL). The device will have around six million readout channels. Given the scale of the endcap upgrade project, the electronics system is highly specialised and has significant complexity involving multiple layers of data transfer, so testing must be carefully planned. The strategy has been to split the efforts between vertical (start-to-end) and horizontal (parallelisation) test systems wherever possible. An important milestone for the former has been the development and operation of test systems to prototype one vertical slice of the future endcap electronics system.

As for the final detector, the test systems consist of front-end (on-detector) electronics hardware with prototype custom ASICs and a back-end (off-detector) ATCA board (Serenity) running custom firmware and software. In addition, in both its front-end and back-end segments, the test system readout is split into two parts for the readout of coarse granularity data (for the trigger system) and high granularity data (for full event readout). The trigger back-end is responsible for using the coarse data to decide if the corresponding event should be read out in high definition. The DAQ back-end is also responsible for distributing a precise timing reference to both the front-end systems and also for their control and configuration.

The main goals of the tests have been to verify various kinds of data exchange between the front-end and the back-end electronics, specifically the timing distribution, slow and fast control, acquisition of coarse and high-definition data, etc., across all the relevant interfaces. The success in all these activities will allow the project to move towards horizontal system scaling. Everything listed, except the readout of the high-definition data (where the relevant prototype data concentrator ASIC is not yet fabricated), has already been achieved.

Specifically, the clock reference brought from the back-end can be reliably recovered in the front-end ASICs such that the two parts are fully synchronised. Regarding slow control, it is possible to read from and write to any register of any ASIC existing in the front-end. Considering fast control, the back-end can send a variety of fast commands with evidence of them being properly received by the front-end ASICs. The front-end readout (ROC) ASICs can be configured to send user-defined trigger data. These data can then be transmitted through a sequence of several additional front-end ASICs, complete their journey via the fibre-optic channel to the back-end and be unpacked by the back-end firmware where they precisely match what the readout ASICs were configured to originally send out.

This presentation will illustrate the architecture of the electronics systems, explain how the prototypes are related to a vertical slice of the future endcap electronics system, and summarise the central objectives that have been achieved to date. In addition, it will give an outlook into future test system activities.

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