Today’s talk:

- FASER detector rationale
- Upgrade of preshower
  - monolithic silicon pixel ASIC
- Upgrade of calorimeter readout scheme
- FASER(ν)2 at Forward Physics Facility (FPF)

Check these out too!

- Noshin: first dark photon search results
- Tobias: neutrinos in the forward region
- Rosham: new physics searches at FPF
The ForwArd Search ExpeRiment at the LHC

Search for light, weakly interacting (LLP) new particles stemming from rare meson decays ($\pi$, $\eta$, $K$, $D$ ...) in very forward ATLAS region ($\theta \sim \mu$rad)

Today’s talk:

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- Upgrade of preshower
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The FASER Experiment

≈ 7 m length, 20 cm aperture (magnets)

- Tracking spectrometer stations
- Electromagnetic Calorimeter
- Trigger / pre-shower scintillator system
- Magnets
- Decay volume
- Interface Tracker (IFT)
- Trigger / timing scintillator station
- Front Scintillator veto system
- To ATLAS IP
- FASERv emulsion detector
The FASER Experiment

\[ \sim 7 \text{ m length, 20 cm aperture (magnets)} \]

2 tungsten layers (2 \( X_0 \)) + 2 graphite layers + 2 scintillators

Electromagnetic Calorimeter

Tracking spectrometer stations

Scintillator veto system

Interface Tracker (IFT)

Decay volume

Front Scintillator veto system

To ATLAS IP

Trigger / pre-shower scintillator system

Magnets
Current Detection Capabilities: Two Fermions

Signal: decays into 2 fermions (0.1-5 TeV)

Signal: decays into 2 photons (0.1-5 TeV)

no X-Y granularity: unable to resolve diphoton events!
**Desired Detection Capabilities:** Two Fermions / Photons

Signal: decays into 2 fermions (0.1-5 TeV)

- **A'**
  - **VETO**
  - **Decay Volume**
  - **Tracker**
  - **Calorimeter**

Signal: decays into 2 photons (0.1-5 TeV)

- **Φ**
  - **VETO**
  - **Decay Volume**
  - **Tracker**
  - **Calorimeter**

- **Upgraded pre-shower**
- **Calorimeter**

**Desired Detection Capabilities:**
- Two Fermions / Photons
- fine X-Y granularity, high dynamic range

**Notes:**
- Decays into 2 fermions (0.1-5 TeV)
- Decays into 2 photons (0.1-5 TeV)

**Stefano Zambito | Université de Genève**
Upgraded preshower detector

- 6 detector planes + 2 scintillators
- each plane: 1 $X_0$ tungsten + monolithic Si pixel sensors
- project approved by CERN: CERN-LHCC-2022-006
- targeting installation in 2024, during LHC Run 3
6 planes in total (silicon detector + W plate)

6 ASICS per module, 208x128 pixels each

12 modules per plane, on cooling plate
Simulating two photons:
\[ E_\gamma = 1 \, \text{TeV}, \quad \Delta R_\gamma = 0.5 \, \text{mm} \]
Simulating two photons:

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Simulating two photons: 

\( E_\gamma = 1 \text{ TeV}, \Delta R_\gamma = 0.5 \text{ mm} \)
Stefano Zambito | *Université de Genève*

**Simulating two photons:**

\[ E_{\gamma} = 1 \text{ TeV}, \Delta R_{\gamma} = 0.5 \text{ mm} \]

Layer 6

- Simulation implemented in ALLPIX2
  - Realistic hexagonal pixel matrix
  - Charge measurement simulation (MC events from Cadence IC)
    - Including channel-to-channel variations and ADC resolution
  - Example: two photons of \( E = 1 \text{ TeV}, 500 \mu\text{m} \) separation
Monolithic active pixel sensor
130 nm SiGe BiCMOS technology (IHP SG13G2)

- High-resistivity (220 $\Omega \cdot \text{cm}$) substrate, about 130 $\mu\text{m}$ thickness
- Hexagonal pixels integrated as triple wells; 80 fF pixel capacitance
- High dynamic range for charge measurement (0.5÷65 fC); fast readout of many channels

Main specifications

<table>
<thead>
<tr>
<th>Specification</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Pixel Size</td>
<td>65 $\mu\text{m}$ side (hexagonal)</td>
</tr>
<tr>
<td>Pixel dynamic range</td>
<td>0.5 ÷ 65 fC</td>
</tr>
<tr>
<td>Cluster size</td>
<td>O(1000) pixels</td>
</tr>
<tr>
<td>Readout time</td>
<td>&lt; 200 $\mu\text{s}$</td>
</tr>
<tr>
<td>Power consumption</td>
<td>&lt; 150 mW/cm$^2$</td>
</tr>
<tr>
<td>Time resolution</td>
<td>&lt; 300 ps</td>
</tr>
</tbody>
</table>
September 2022: CERN SPS Test Beam (20-150 GeV e⁻)

UniGe FEi4 Telescope: tracking & trigger

Calorimeter modules

DUT

e⁻

calorimeter modules
September 2022: CERN SPS Test Beam (20-150 GeV $e^-$)

Testbeam setup in Geant4

- Telescope planes
- Tungsten + DUTs (6.6 $X_0$)
- 3 calorimeter modules (25 $X_0$)

Studying resolution of the calorimeter

UniGe FEi4 Telescope: tracking & trigger

Experimental Setup: DUT Planes

- ASIC
- W: 7*1.1 mm
- 3 DUT planes equipped with v2 chips, each a $X_0$ of tungsten: 6.6 $X_0$ in total (+ telescope)

10 cm
5 cm
September 2022: CERN SPS Test Beam (20-150 GeV e⁻)

- DUT: 3 sensors + 6.6 $X_0$ W
- Calorimeter module
- UniGe FEi4 Telescope: tracking & trigger
- 20 GeV e⁻
September 2022: CERN SPS Test Beam (20-150 GeV e⁻)

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Calorimeter module

DUT: 3 sensors + 6.6 $X_0$ W

- 20 GeV e⁻

Testbeam setup in Geant4

Telescope planes (~$X_0$)

Tungsten + DUTs (6.6 $X_0$)

3 calorimeter modules (25$X_0$)

Studying resolution of the calorimeter

UniGe FEi4 Telescope: tracking & trigger

● Early analysis showed data/mc discrepancies
● Simulations were pointing to missing material upstream in simulation (NA61, magnets, pipes,..) → degraded resolution
● Material upstream simulation with G4Beamline provided by authors of [1]


Special thanks to Ali Eren Simsek and Nikolaos Charitonidis
September 2022: CERN SPS Test Beam (20-150 GeV $e^-$)

Studying resolution of the calorimeter

UniGe FEi4 Telescope: tracking & trigger

DUT: 3 sensors + 6.6 $X_0$ W

Calorimeter module

20 GeV $e^-$

Graph showing simulation of various configurations:
- 6$X_0$ + Calorimeter
- Preshower + Calorimeter
- Preshower ($Q > 1$ fC) + Calorimeter
- Calorimeter

Comparison with and without preshower measurement

$\sigma_E / \langle E \rangle$ vs $E_{beam}$ [GeV]
Diphoton Signature: Sensitivity

Impact of upgrader preshower evaluated for benchmark dark photon (a) model

$\mathcal{L} \sim g_{WW} a W \bar{W}$ coupling to SU(2)$_L$

- abundant LHC production thanks to coupling with W
- $a$ exclusively decays to $\gamma\gamma$

![Graph showing diphoton signature sensitivity](image)
Plan to upgrade the calorimeter readout scheme to improve range and energy scale

- Currently relying on single PMT, and optical filter to reduce light output by factor 10

  - Calibrations: MIP data (high PMT gain) extrapolated to low gain with LED-determined gain ratio

- Upgrade: use two separate PMTs to cover low E (high gain) and high E (low gain) at same time

Upgrade: same PMT type, but operated at medium gain

- High energy range PMT: 3-3000 GeV
- Low energy range PMT: 0.1-300 GeV

⇒ 3-300 GeV overlap region for cross-calibrations
FASER 2 upgrade proposed in the context of a broader Forward Physics Facility (FPF)

- 65 m long and 9 m wide cavern, 617-682 m west of ATLAS IP, on beam collision axis
- Besides FASER2 and FASERv2, may host several other experiments: FORMOSA, AdvSND, FLArE, ...

The Forward Physics Facility (FPF) is a proposal to build a new underground cavern at the Large Hadron Collider (LHC) to host a suite of far-forward experiments during the High-Luminosity LHC era.
FASER2 detector: wider, and longer

- $\pi^0$ angular acceptance increasing from 0.6% to 10%
- Improved sensitivity to large LLP masses and longer lifetimes
- Larger volume requires revised instrumentation strategy:
  - need 4 Tm bending power: superconducting magnets
  - much bigger tracker: silicon (mostly) replaced by SciFi
FASEv2: 20-ton emulsion-based v detector

- 3300 AgBr layers interleaved with tungsten plates
- veto + two tracker planes to interface with FASER2
- μ charge, and global event reconstruction
- for HL-LHC, expect: O(10^6) ν_μ, O(10^5) ν_e, O(10^4) ν_τ
Empowering FASER’s capabilities with several upgrades...

▶️ **New preshower will enable multi-γ tagging and greatly increase dark photon searches’ reach**
   - Detector layout and mechanics design converged; pre-production ASIC extensively tested
   - Final chip design just submitted to foundry: targeting preshower installation in 2024

▶️ **Calorimeter readout scheme upgrade: extended range and improved energy scale**

▶️ **Further upgrades proposed in the context of a broader Forward Physics Facility**
   - Wider and longer FASER2 detector to tackle larger LLP masses and longer lifetimes
   - Bigger and more complex FASERv2 system to expand neutrino physics program
Empowering FASER’s capabilities with several upgrades...

- New preshower will enable multi-$\gamma$ tagging and greatly increase dark photon searches’ reach
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- Calorimeter readout scheme upgrade: extended range and improved energy scale

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  - Bigger and more complex FASERv2 system to expand neutrino physics program

... Many years of exciting physics ahead of us!
Spares
Pre-production ASIC Prototype: Tests

Reticle: 2.4 x 1.5 cm²
53 reticles per wafer
Thickness 300 μm

Wafers received in Jun 2022, tested in laboratory
- I-V characteristics measured at probe station
- Charge response scrutinised with $^{109}$Cd and IR laser
- Stress-tests for digital electronics and readout

CHIP Schematic
CHIP @ probe station
Monolithic Pixel ASIC: Chip Structure

Chip organized in 13 “super-columns”, each with:

- active region, subdivided into 8 “super-pixels” of 16x16 pixel each
- digital column (40 μm) in the middle: sharing of digital electronics

Digital periphery on the bottom, and multiple guard-ring structure

Super pixel:
- 16 rows of 8+8 pixels
- analog multiplexer
- 4-bit flash ADC
- 3 fast-OR lines
- local bias circuit
- programming logic to mask pixels

Dead area <5%
Monolithic Pixel ASIC: Pixel Circuitry

Charge measured per-pixel, simultaneously for different super-pixels
Monolithic Pixel ASIC: Pixel Circuitry

Charge measured per-pixel, simultaneously for different super-pixels

hit above threshold generates signal sent to periphery via fast-OR
Charge measured per-pixel, simultaneously for different super-pixels

- hit above threshold generates signal sent to periphery via fast-OR
- charge is stored into pixel’s analog memory
Monolithic Pixel ASIC: Pixel Circuitry

Charge measured per-pixel, simultaneously for different super-pixels

- hit above threshold generates signal sent to periphery via fast-OR
- charge is stored into pixel’s analog memory
- after some delay, readout starts super-column after super-column

![Diagram of Monolithic Pixel ASIC](image-url)
Monolithic Pixel ASIC: Charge Measurement

Analog memories: capacitors inside each pixel charged with constant current during ToT

- when signal returns below threshold, memory is disconnected and left floating until read by flash ADC
- preamplifier designed to produce a signal proportional to the log of input charge

Simulation data

<table>
<thead>
<tr>
<th>Time (ns)</th>
<th>Amp Out (V)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.0</td>
<td>1.1</td>
</tr>
<tr>
<td>80.0</td>
<td>1.0</td>
</tr>
<tr>
<td>160.0</td>
<td>0.9</td>
</tr>
<tr>
<td>300.0</td>
<td>0.8</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Time (ns)</th>
<th>Memory Value (V)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.0</td>
<td>1.25</td>
</tr>
<tr>
<td>200.0</td>
<td>1.1</td>
</tr>
<tr>
<td>400.0</td>
<td>1.0</td>
</tr>
<tr>
<td>600.0</td>
<td>0.9</td>
</tr>
</tbody>
</table>

- Low current leakage: error < 1 LSB (ADC) for readout time <= 200 µs
Pre-production Chip (2022)

Engineering run (IHP Microelectronics)

► In each reticle, three pixel matrices

**FASER_v1 (baseline)**

† 128 x 64 pixels, 4 super-columns
† in-pixel pre-amp and driver
† discriminator outside

**FASER_v2**

† 128 x 48 pixels, 3 super-columns
† in-pixel pre-amp, driver, and discriminator

**FASER_ALT**

† 128 x 48 pixels, 3 super-columns
† no analog memories
† counter for charge measurement

► Several test structures (TDC, etc...)

Reticle: 2.4 x 1.5 cm²
53 reticles per wafer
Thickness 300 μm
Evaluating charge response with infrared laser

▶️ measuring ToT via fast-OR signal on the scope
▶️ varying per-pixel injected charge via laser attenuator
▶️ measurement repeated at different $l_{\text{preamp}}$

Each colored line is a different pixel

$E_{\text{preamp}} = 0.7 \mu m$
Expect improvement of front-end uniformity in production ASIC thanks to bigger transistors

**Cadence Spectre Simulation:**

*front-end mismatch in pre-reduction prototype*

*front-end mismatch in production ASIC*
**Small Prototype Chip (2021)**

**First chip prototype tested in 2021**

- designed to study different levels of integration of front-end electronics
- simultaneous goals: minimize dead area and routing capacitance, maximize stability

From all electronics in pixel

Best expected performance

- All front-end system in Pixel
- Driver in Pixel, discriminator outside
- Everything in Pixel, featuring an inverting stage
- Only pre-amplifier in Pixel
- All front-end system outside

Backup options for further studies

To all electronics outside pixel

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F. Martinelli et al. 2021 J. Inst. 16 P12038
https://doi.org/10.1088/1748-0221/16/12/P12038
Small Prototype Chip (2021)

First chip prototype tested in 2021

- designed to study different levels of integration of front-end electronics
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<table>
<thead>
<tr>
<th>Configuration</th>
<th>$\sigma_v$ [mV]</th>
<th>$G_C$ [mV/fC]</th>
<th>$ENC$ [e$^-$]</th>
<th>$\sigma_{V_{th}}$ [mV]</th>
</tr>
</thead>
<tbody>
<tr>
<td>All f.e. outside pixel</td>
<td>4.2 ± 0.2</td>
<td>159 ± 1.0</td>
<td>165 ± 9</td>
<td>32.3</td>
</tr>
<tr>
<td>Only pre-amp. in pixel</td>
<td>2.5 ± 0.1</td>
<td>96.8 ± 0.5</td>
<td>161 ± 9</td>
<td>26.9</td>
</tr>
<tr>
<td>All f.e. in pixel, inv. stage</td>
<td>6.9 ± 0.5</td>
<td>179 ± 1.0</td>
<td>241 ± 19</td>
<td>30.8</td>
</tr>
<tr>
<td>Pre-amp. and driver in pixel</td>
<td>3.8 ± 0.2</td>
<td>133.7 ± 0.6</td>
<td>178 ± 9</td>
<td>23.4</td>
</tr>
<tr>
<td>All f.e. in pixel</td>
<td>5.4 ± 0.4</td>
<td>148 ± 1.0</td>
<td>228 ± 20</td>
<td>27.1</td>
</tr>
</tbody>
</table>

Last two configurations are good compromise between compactness and performance: adopted for pre-production prototype
When we have a hit into a pixel, a copy of the signal exits IMMEDIATELY the pixel through FASTOR.

Each FASTOR sends a signal to the periphery to start the READOUT.

To be sure we collected the charge entirely, the periphery waits a bit before starting the READOUT.

If in a super-pixel zero FASTOR are active, zero bits are sent to the periphery (optimization).

A super-column is composed of 8 super-pixels (16x16 pixels).

Each super-column contains the entire logic necessary to read its own information (readout).

From FASTOR to periphery that starts READOUT.

Periphery of matrix with three super-columns (from pre-production ASIC).