

Status and Perspectives for ATLAS HL-LHC Upgrade Program

Sebastian Grinstein

ICREA/IFAE-Barcelona



On behalf of the **ATLAS Collaboration**

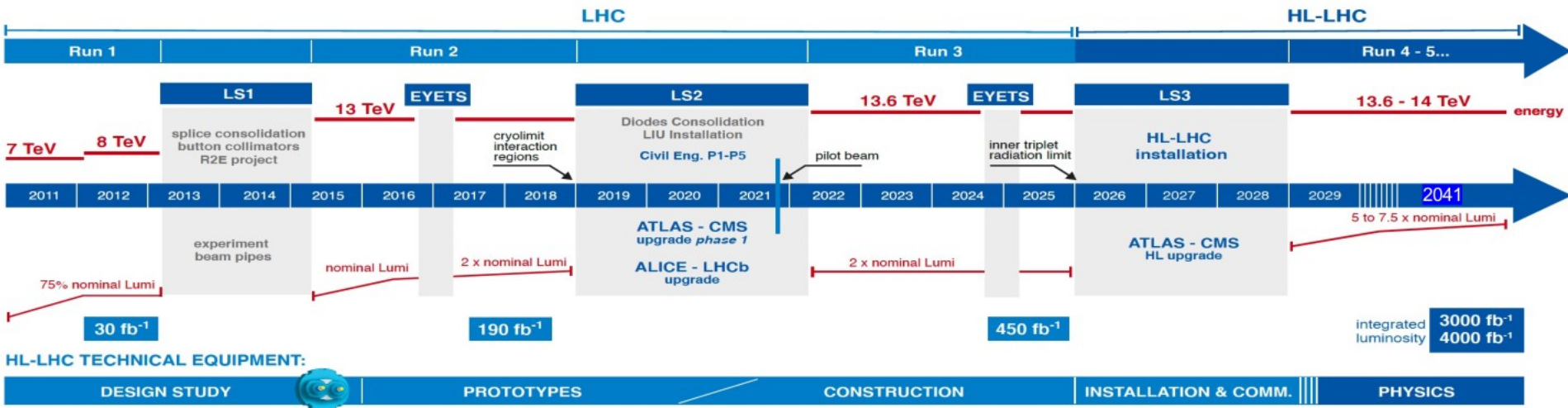


XII International Conference
on New Frontiers in Physics

10-23 July 2023, OAC, Kolymbari, Crete, Greece

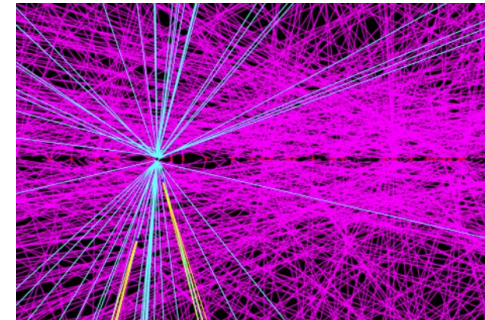


The High Luminosity LHC



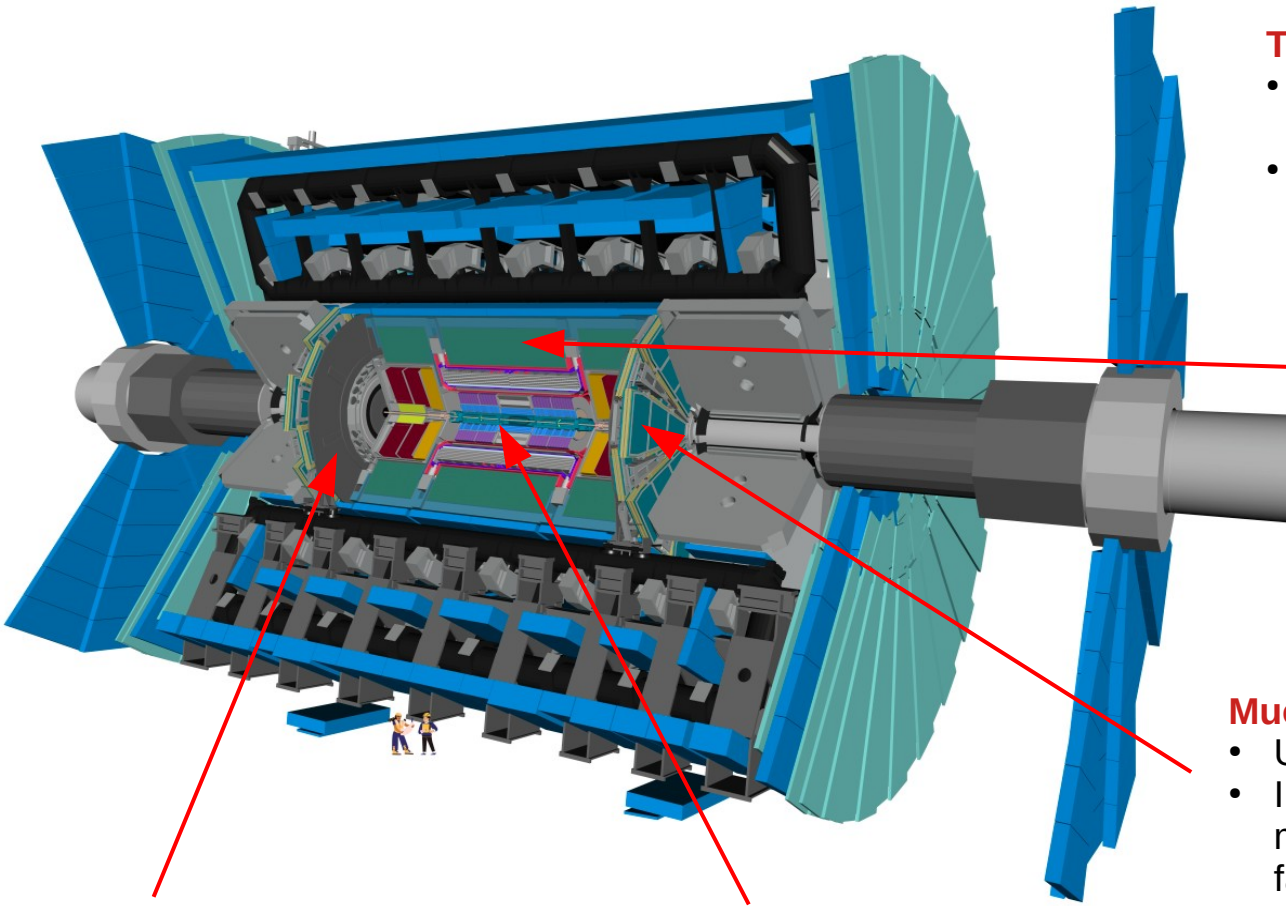
- LHC and its experiments have produced many results (see talks in this and future sessions)
- LHC accelerator periodically upgraded to keep exploring the energy frontier...
- The “HL-LHC” period will start in ~2029 with ~5 times the nominal luminosity
- This will increase the pile up from current $\mu \sim 50$ to $\mu = 200$
- Need to **upgrade ATLAS experiment** to deal with more radiation damage, more “messy” events...

LHC event



HL-LHC simulation

ATLAS Upgrade Overview



Trigger and DAQ Upgrade

- Single level Trigger with 1MHz output (x 10 current)
- Improved system with faster FPGAs

Calorimeter Electronics

- On-detector electronics upgrades of LAr and Tile Calorimeters
- Provide 40 MHz readout for triggering

Muon Detector

- Upgrade of inner barrel chambers
- Improve trigger efficiency and momentum resolution, and reduced fakes

High Granularity Timing Detector

- Precision track timing (30 ps)
- Improve pile-up rejection in the forward region

New Inner Tracker (ITk)

- All silicon with 9 layers up to $|\eta|=4$
- Less material finer segmentation
- Improve vertexing, tracking, b-tagging

See talk of C. Luci on phase-I Upgrades

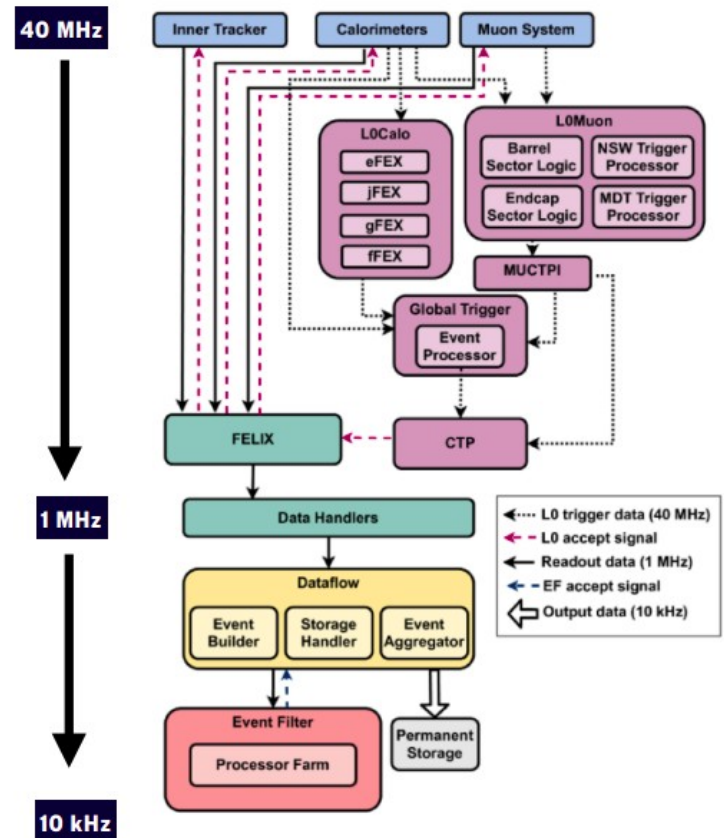
Trigger and DAQ Upgrade

Trigger:

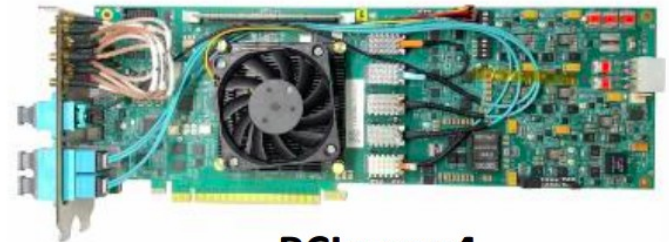
- Trigger data input at 40 MHz
- Level-0: Rate 1 MHz, latency 10 μ s
- Software based Event Filter: Rate 10 kHz
- Exploits full detector granularity and extended tracking range, improves muon trigger efficiency
- For the Event Filter use COTS hardware, either pure software solution, or GPU or FPGA card acceleration (under evaluation).

DAQ:

- Unified backend electronics based on custom PCIe FPGA cards (FELIX) instead of VME-based readout boards



FELIX Prototype Board



PCIe gen4

Calorimeter Electronics

Continuous readout at 40 MHz:
New on-detector and off-detector electronics

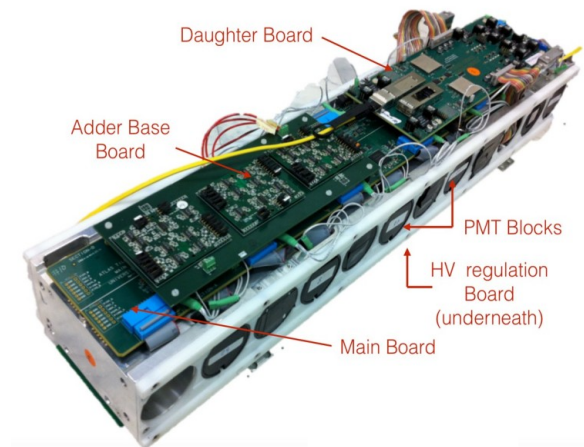
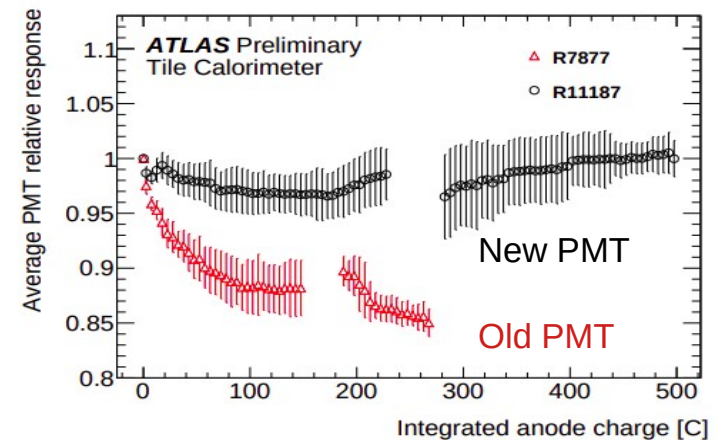
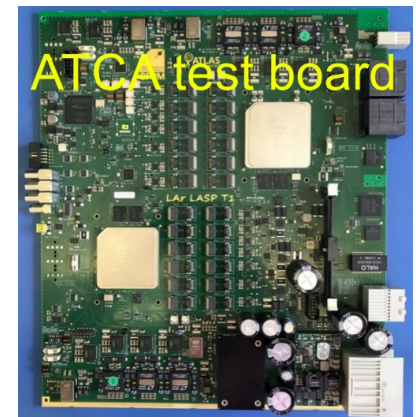
Liquid Argon Calorimeter (LAR)

- Total bandwidth of 345 Tbps
- New high precision front-end electronics with a 16-bit dynamic range and 0.1% linearity
- ATCA boards for waveform feature extraction (E, time)
- New ASICS (ADC, calibration DAC & pulser)

Tile Calorimeter:

- Replacement of the most exposed PMTs (about 10%).
- Replacement of passive PMT HV-dividers by active dividers for better response stability.
- On-detector electronics at advanced stage, production ongoing
- Phase-2 demonstrator installed (July 2019) in ATLAS and is taking data during Run 3

See A. Gavriluk talk in this conference



Muon System

Upgrade readout/trigger electronics

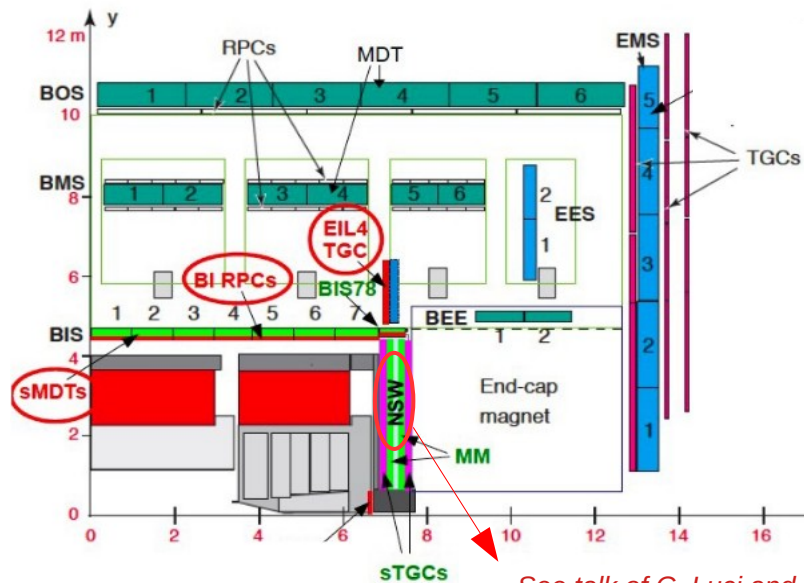
- all hit data is sent off detector to trigger logic boards with L0 trigger rate of 1 MHz

Addition layers of sMDT, RPC, and TGC

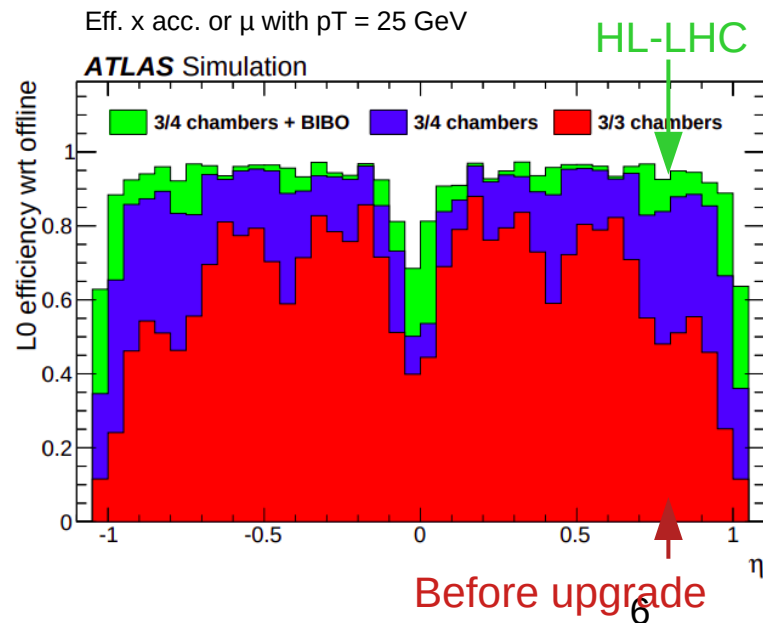
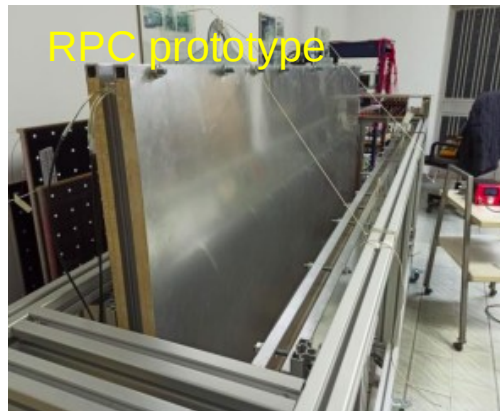
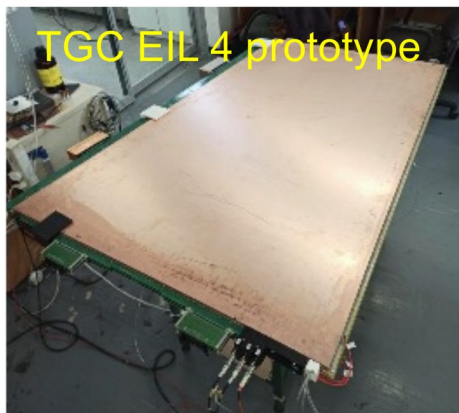
- Improve coverage, trigger uniformity & momentum resolution, reduce fake rates

Current status

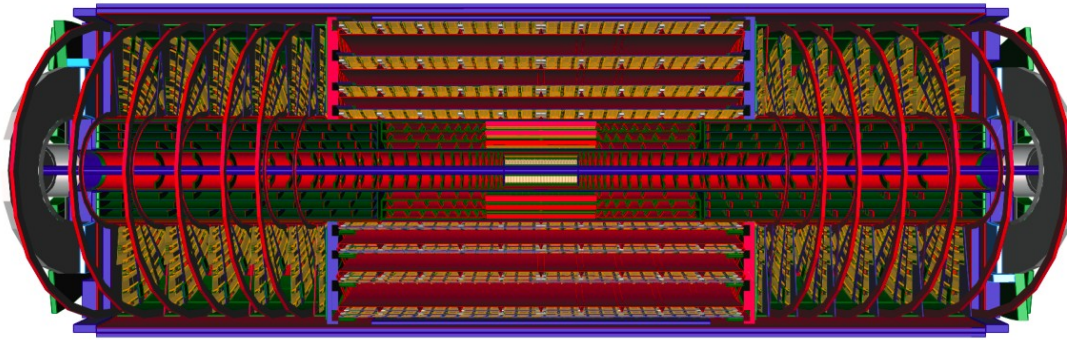
- sMDT: chambers in production, electronics pre-production
- RPC: FE prototypes submitted, prototype chamber nearly complete
- TGC: Triplet prototype completed, FE ASIC production complete



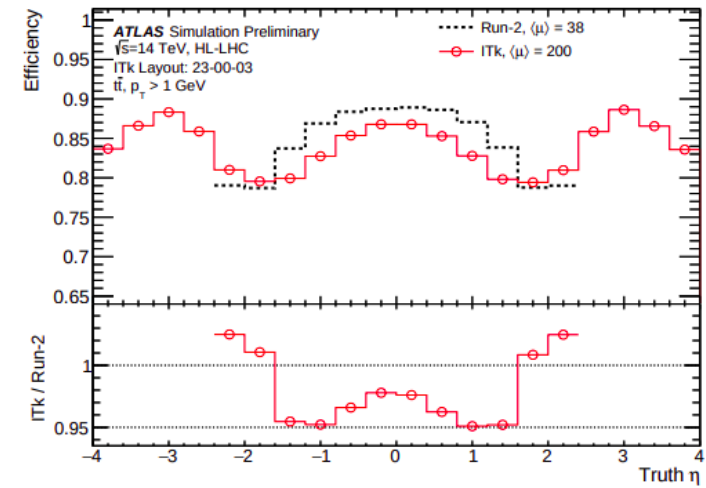
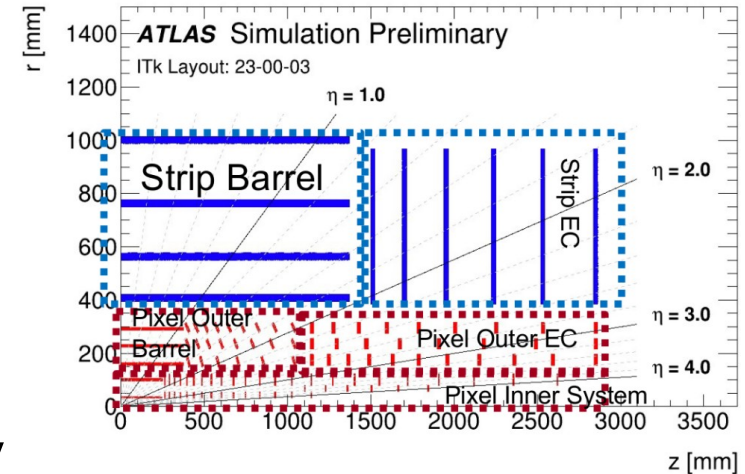
See talk of C. Luci and S. Kabana



Inner Tracker (ITk)



- Complete replacement of the current Inner Detector (Pixel, SCT, TRT) with **Silicon**-only system
- Pixel (Inner system, outer barrel, outer endcap, 13 m²) and Strip detector (barrel, endcaps, 168 m²)
- Eta coverage increases **from 2.5 to 4**
- Reduced material and finer segmentation
- At least 9 silicon hits per track
- Radiation tolerant up to **1E16 neq/cm²** (inner Pixel)



ATL-PHYS-PUB-2021-024

ITk Pixel Detector

General features:

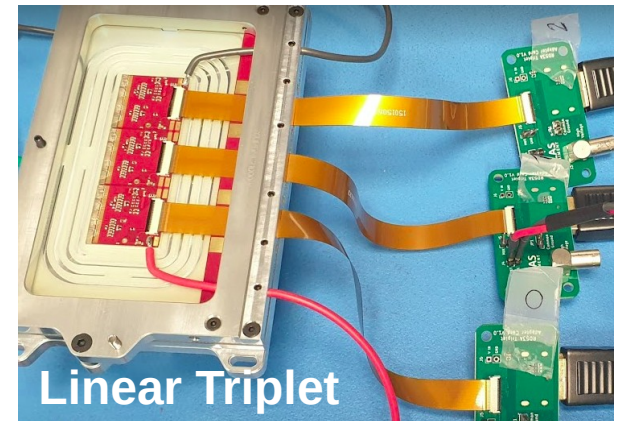
- Organized as three systems (inner, outer, outer endcaps)
- Five barrel-layers
- More than 5,000 M pixels, ~10 k modules
- Inner system replaceable (radiation damage)
- Serial powering
- Carbon fiber supports, thermal demonstrators

Sensors:

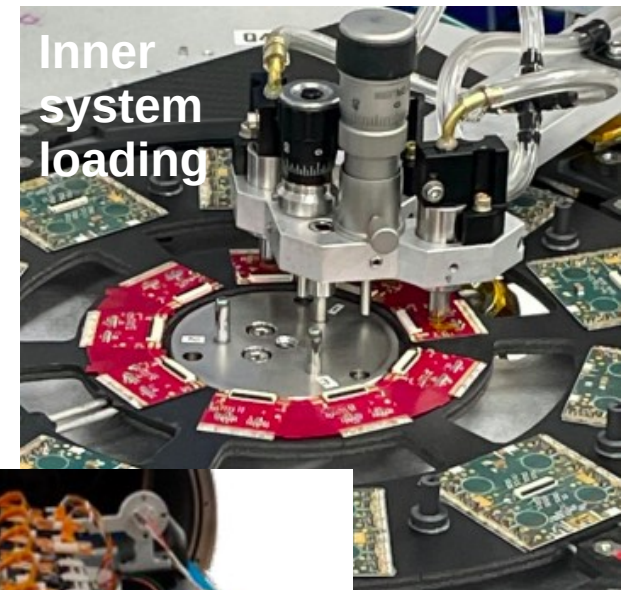
- Pixel sizes $25 \times 100 \mu\text{m}^2$ (innermost barrel) and $50 \times 50 \mu\text{m}^2$ (everywhere else)
- 3D sensors in innermost barrel/disks and planar sensors in the other layers
- 3 or 4 FE chips/module

Production status:

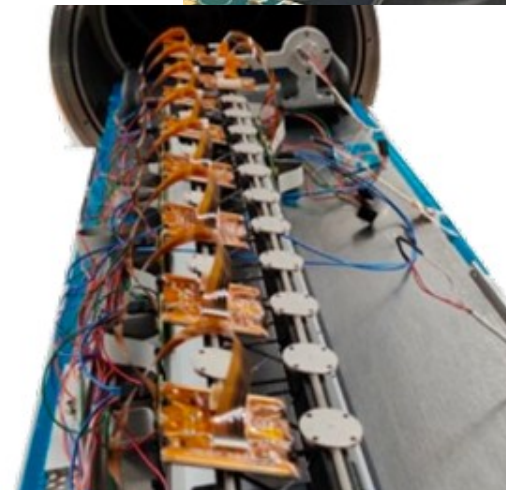
- All sensors are in pre-production
- Hybridization pre-production modules started
- ITkPixV2 readout chip has been submitted



Linear Triplet



Inner system loading



Thermal studies

ITk Strip Detector

General features:

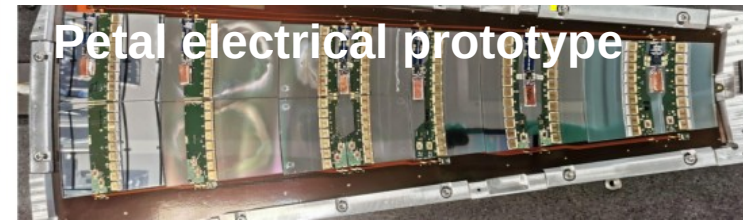
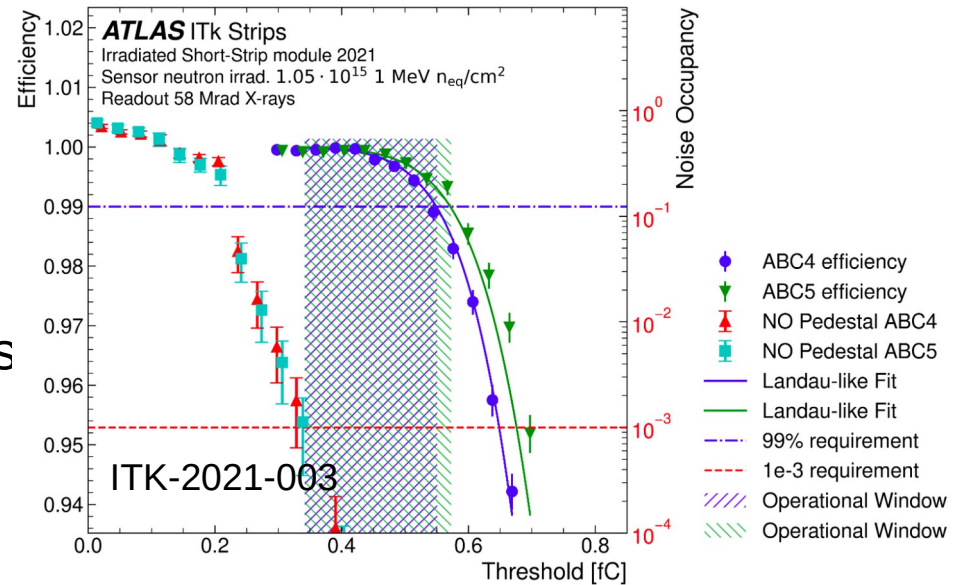
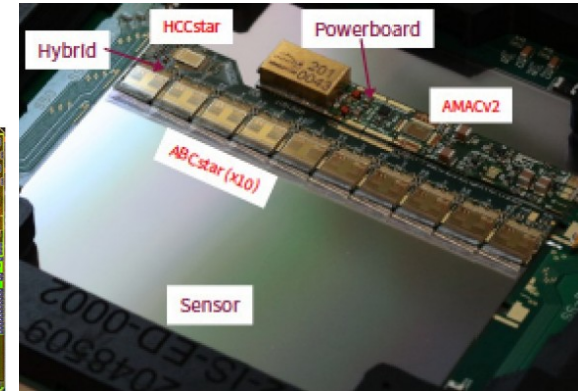
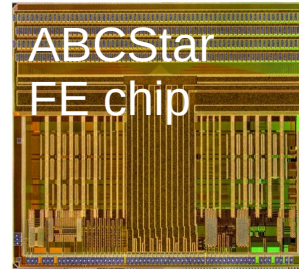
- Four-layer barrel and two six-disk endcaps
- Angular coverage of $|\eta| < 2.7$
- 18 k modules

Sensors/ASICs:

- Strip width $\sim 75 \mu\text{m}$
- ~ 60 M channels
- ABCStar, HCCStar and AMAC chips
- Radiation: $1.6\text{E}15 \text{ neq/cm}^2$

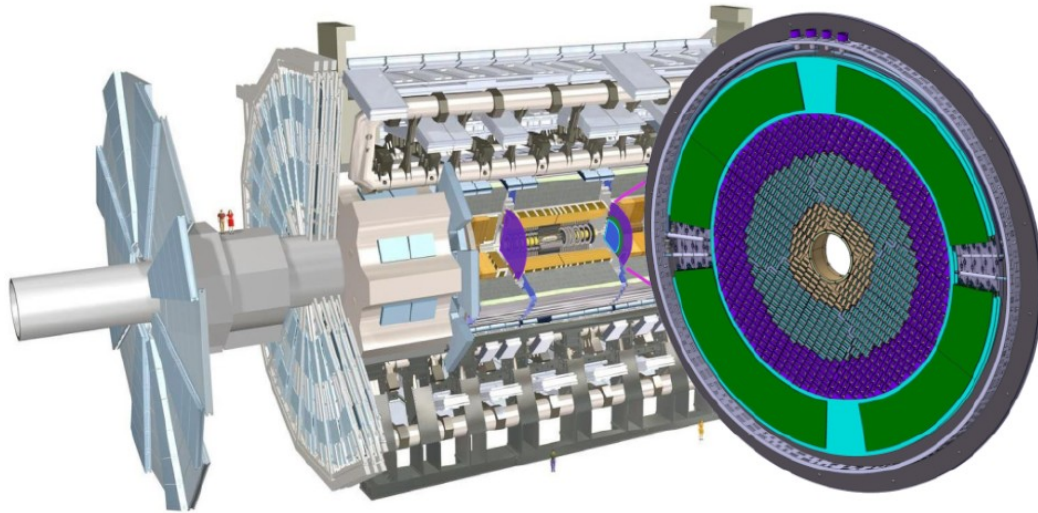
Production status:

- Sensors: In production.
- ASICs in production
- Hybrids and modules in pre-production
- Mechanics in production



9
~62 cm

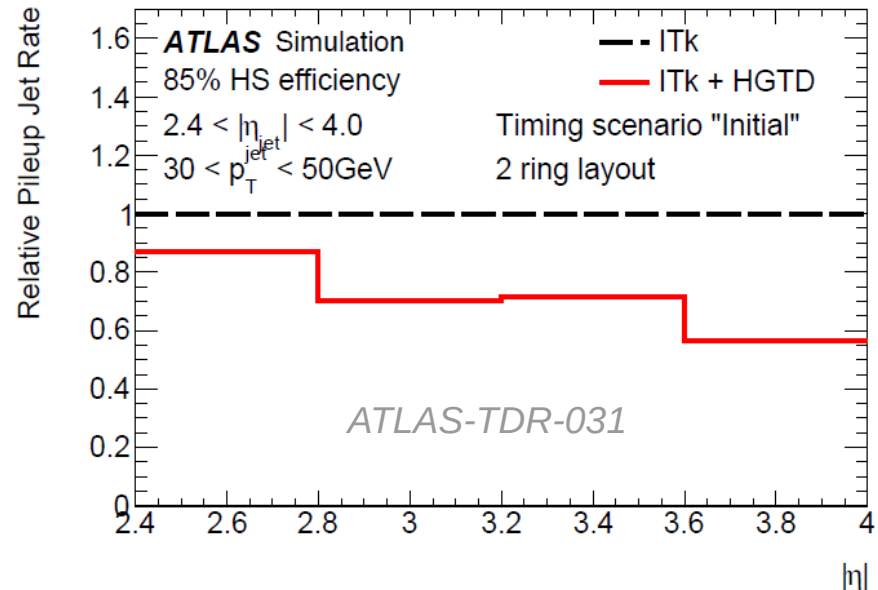
High Granularity Timing Detector



- HGTD designed to improve ATLAS performance in the forward region in view of increased pile up in the HL-LHC
- Also provides luminosity information

Target time resolution:
30-50 ps/track up to 4000/fb

- Located between barrel and end-cap calorimeters ($|z|=3.5$ m)
- Silicon detector modules mounted on disks
- Two sensor layers/disk
- Two disks/side (total 4 layers/side)
- Active area: $12 \text{ cm} < r < 64 \text{ cm}$
 - **$2.4 < |\eta| < 4.0$**
- Disk replacement plan to maintain $2.5\text{E}15 \text{ neq/cm}^2$ level



High Granularity Timing Detector

Sensor:

- 15x15 array with pad size: 1.3 x 1.3 mm²
- Single-event burnout (SEB) was observed on LGAD sensors during beam tests
- Mitigated by carbon-infused sensors (can be operated at decreased high voltage)

ASIC:

- First full size ALTIROC2 prototype very successful, not fully rad hard
- ALTIROC3 wafers recently received

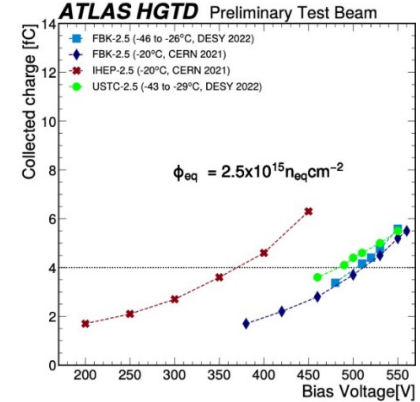
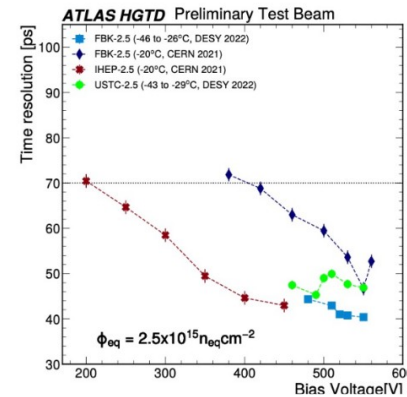
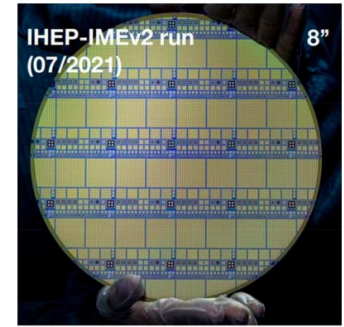
Modules:

- Modules (2 ALTIROCs bump bonded to 2 LGAD sensors) have been demonstrated to work

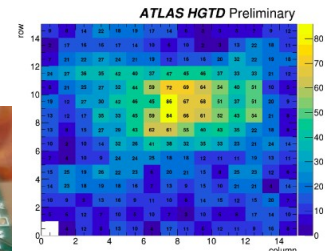
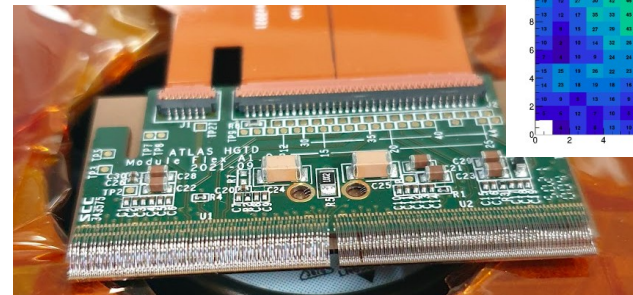
System tests:

- Thermal demonstrator
- Electrical demonstrator on-going

See S. Ridouani more detailed talk this afternoon



HGTDPublicPlots



Summary and Conclusions

- ATLAS detector currently undergoing mayor upgrade to optimize the experiment for HL-LHC data taking period
 - Objective is to maintain or improve physics performance in view of more demanding environment
- Trigger system upgrade: 100 kHz to 1 MHz
- Most detector electronics (DAQ and trigger systems) will be upgraded to cope with the luminosity increased and increased trigger/readout rate
- Muon detector upgrade (sMDT, TGC, RPC) to improve coverage and triggering
- An all-new silicon tracker (ITk) with 5 layer pixel and 4 layer strips which improves tracking up to $|\eta| < 4$
- The High Granularity Timing Detector (HGTD) based on LGADs will help to reduce pile-up effect in the forward region with timing measurements

Many interesting results in this conference and looking forward to physics with the high luminosity LHC!

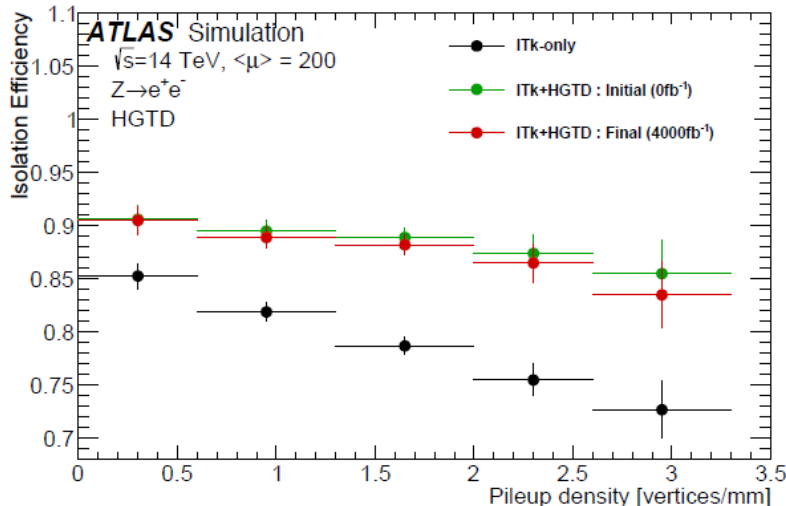
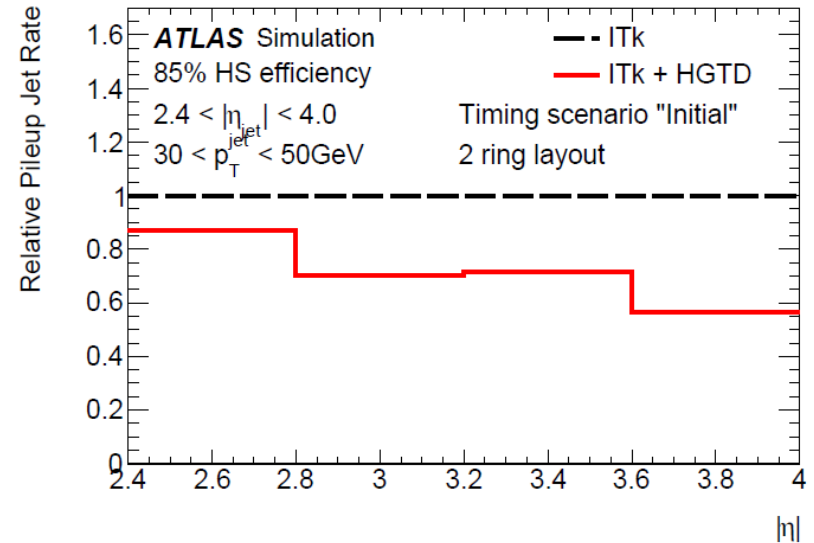
Back Up Slides

Impact of HGTD

Example, two “straight forward” improvements with HGTD

Pile up rejection

- PU jets identified by looking at the tracks associated to a jet
- HGTD can help identifying PU tracks, specially at large η

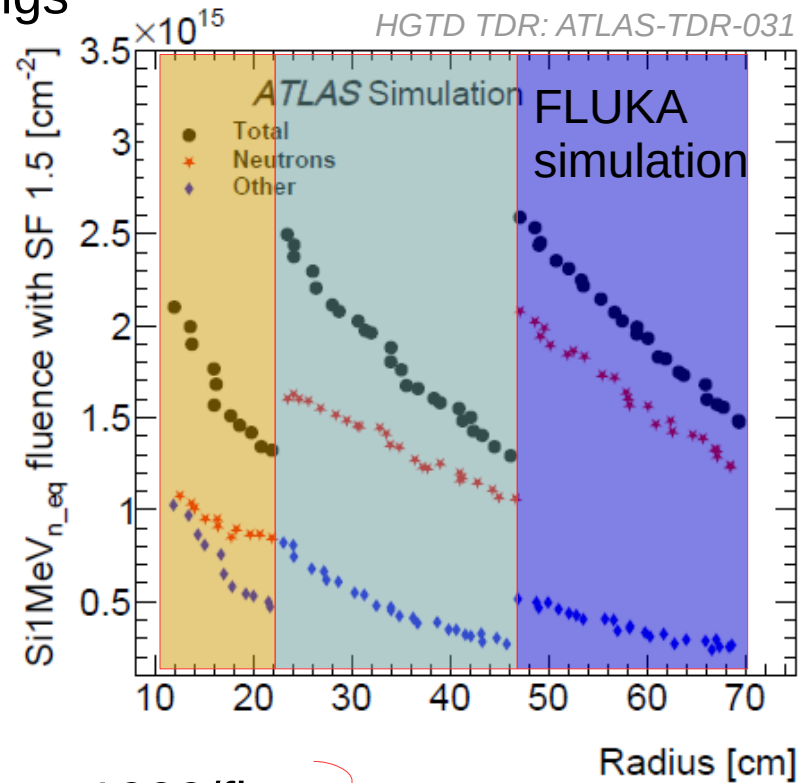
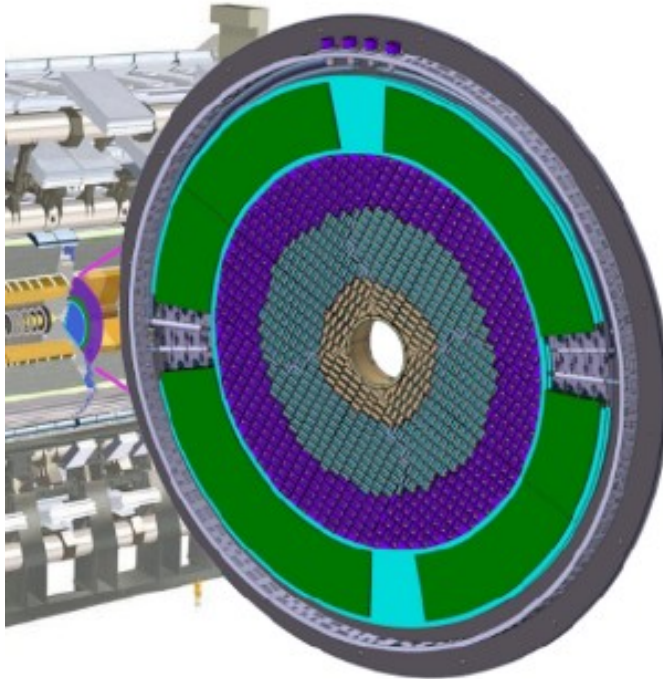


Electron isolation efficiency

- PU tracks can cause electrons to fail isolation requirements
- HGTD can help maintain high efficiency, specially at high pile up

HGTD Radiation Hardness

- The strategy to cope with the high radiation environment is to segment the detector into replaceable rings



- Inner ring (12-23 cm) replaced every 1000/fb
- Middle ring (23-47 cm) replaced every 2000/fb
- Outer ring (47-64 cm) never replaced

Maximum fluence:
 $2.5 \times 10^{15} \text{ 1MeV } n_{\text{eq}} / \text{cm}^2$
 and 2MGy at the end
 of HL-LHC (4000/fb)