Precision Timing at High-Luminosity LHC with the CMS MIP Timing Detector

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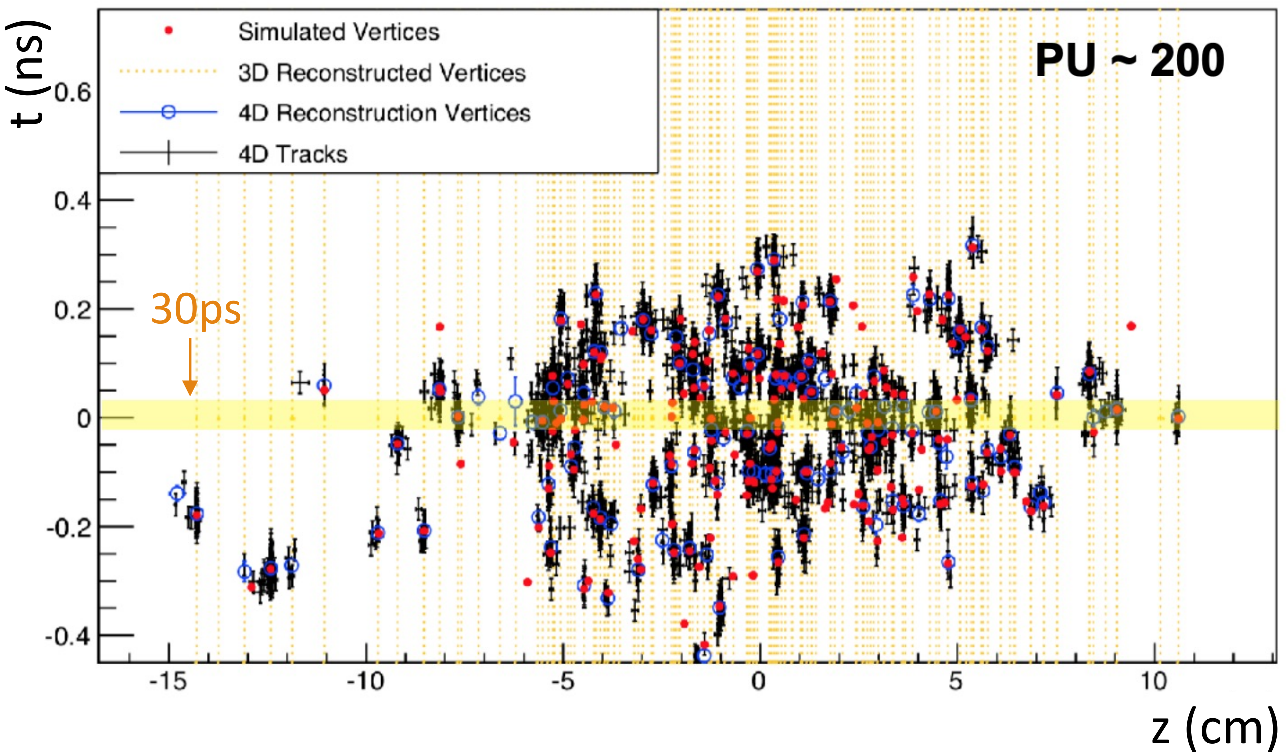
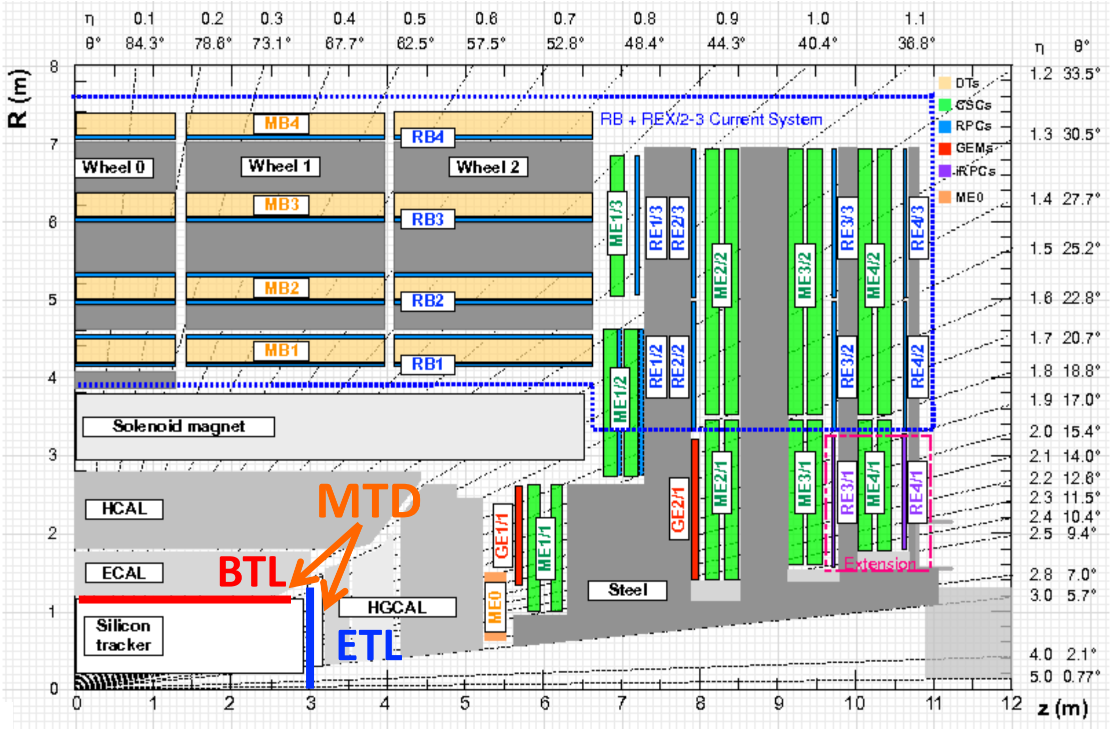
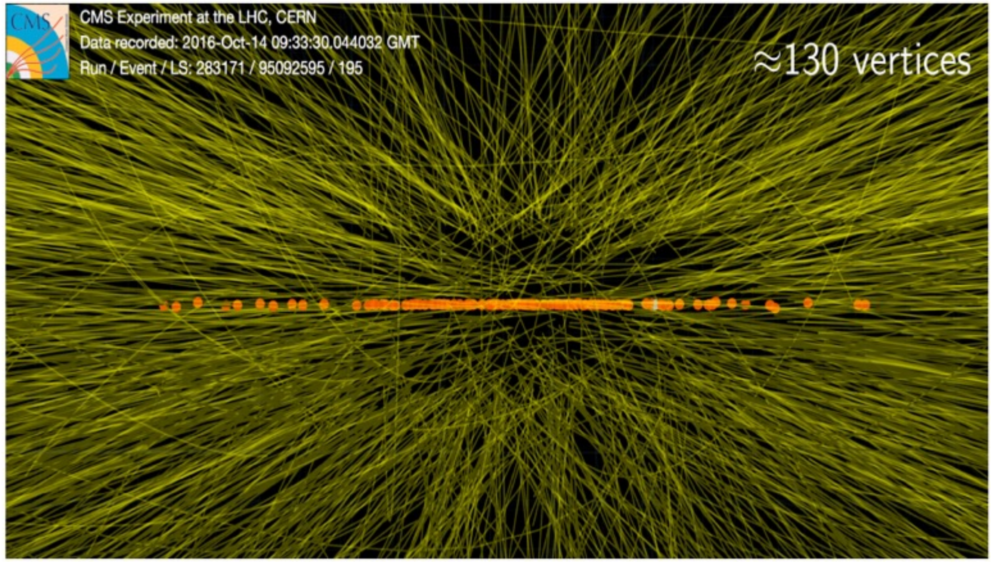
MIP Timing Detector (MTD) for CMS Phase-2 Upgrade





- Important to maintain detector performance during HL-LHC running
  - Time information will help to reduce pileup effects from approximately 200 simultaneous interactions
- MIP timing detector (MTD) consists of barrel timing layer (BTL) and endcap timing layer (ETL), providing 30-50 ps time resolution per track
  - BTL: LYSO crystal scintillator + SiPM readout
  - ETL: Silicon based sensor (LGAD) + ASIC readout
  - Two different detector technologies for radiation hardness and costs

MTD Physics motivation: pile-up mitigation



- Important to maintain detector performance during HL-LHC running
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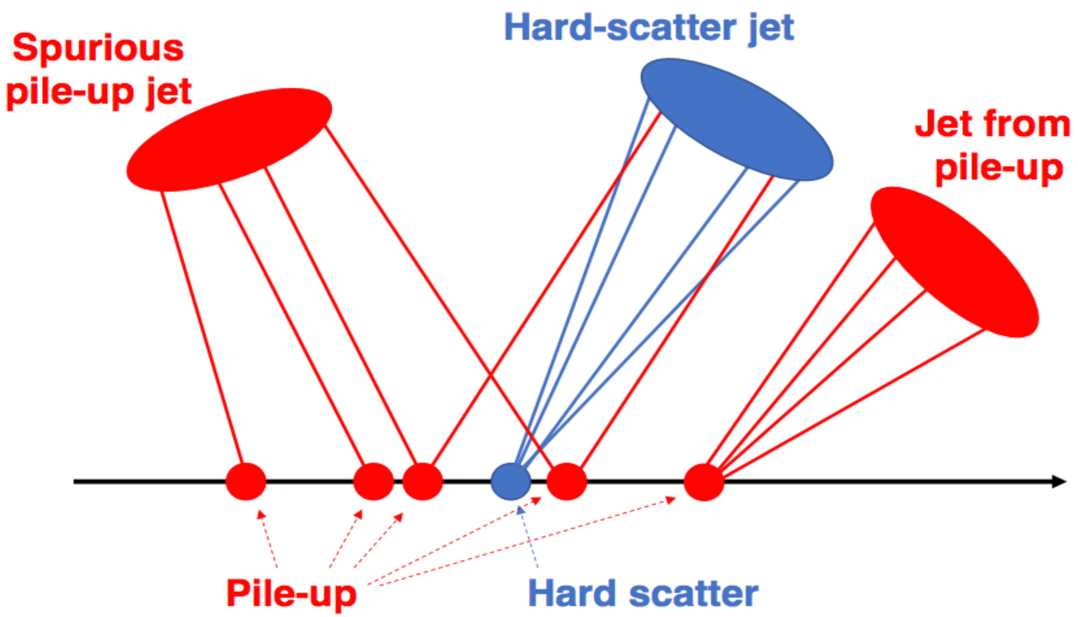
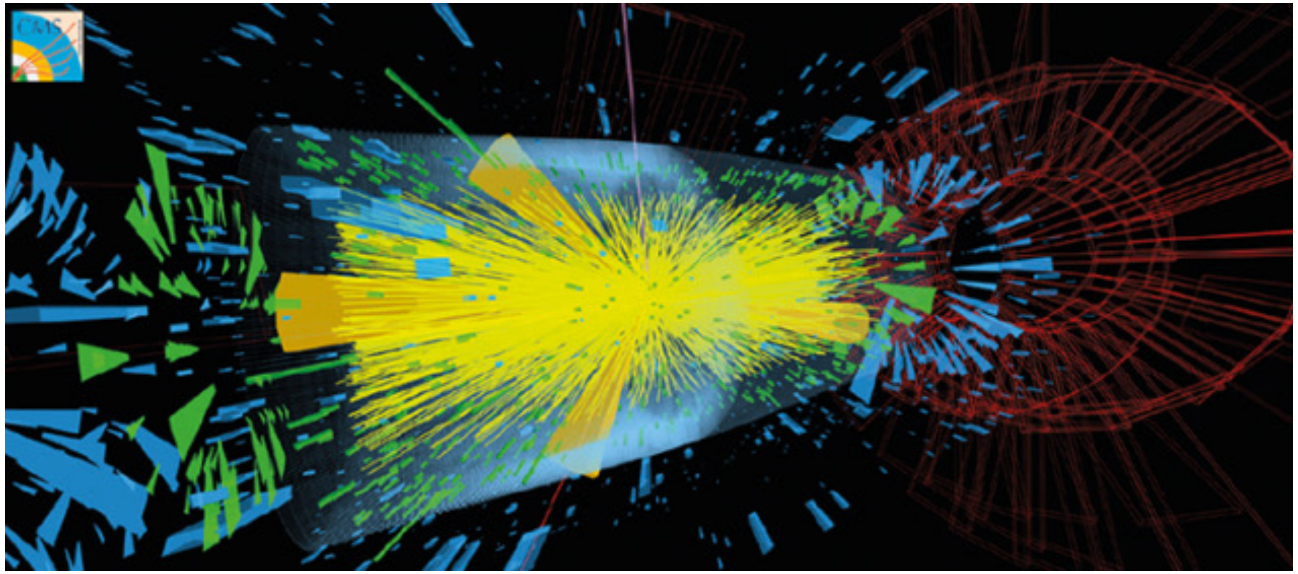
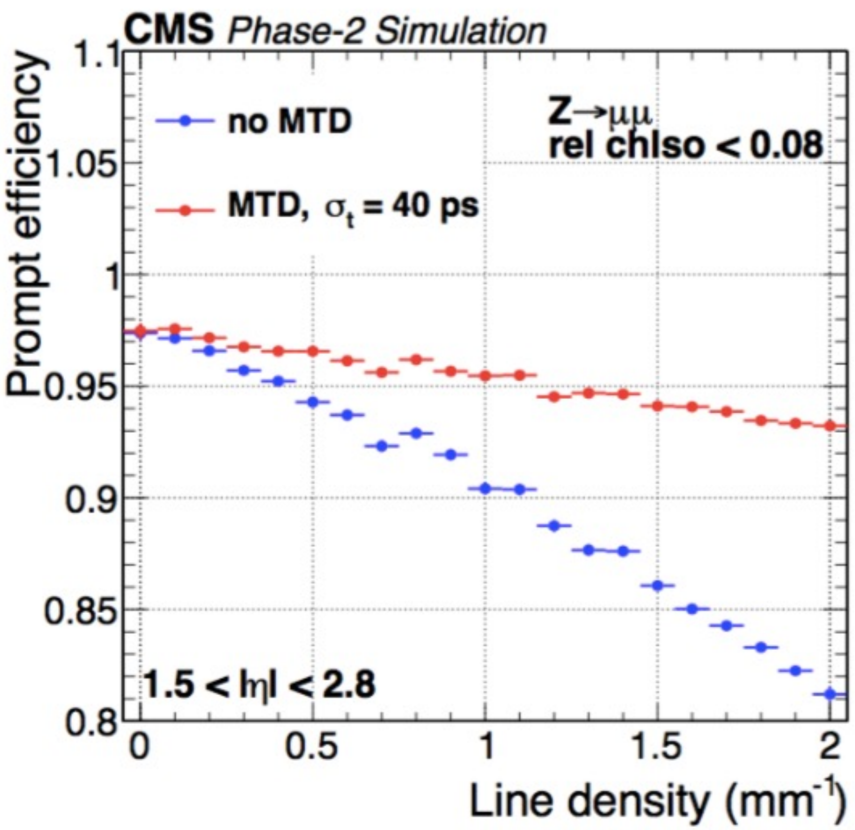
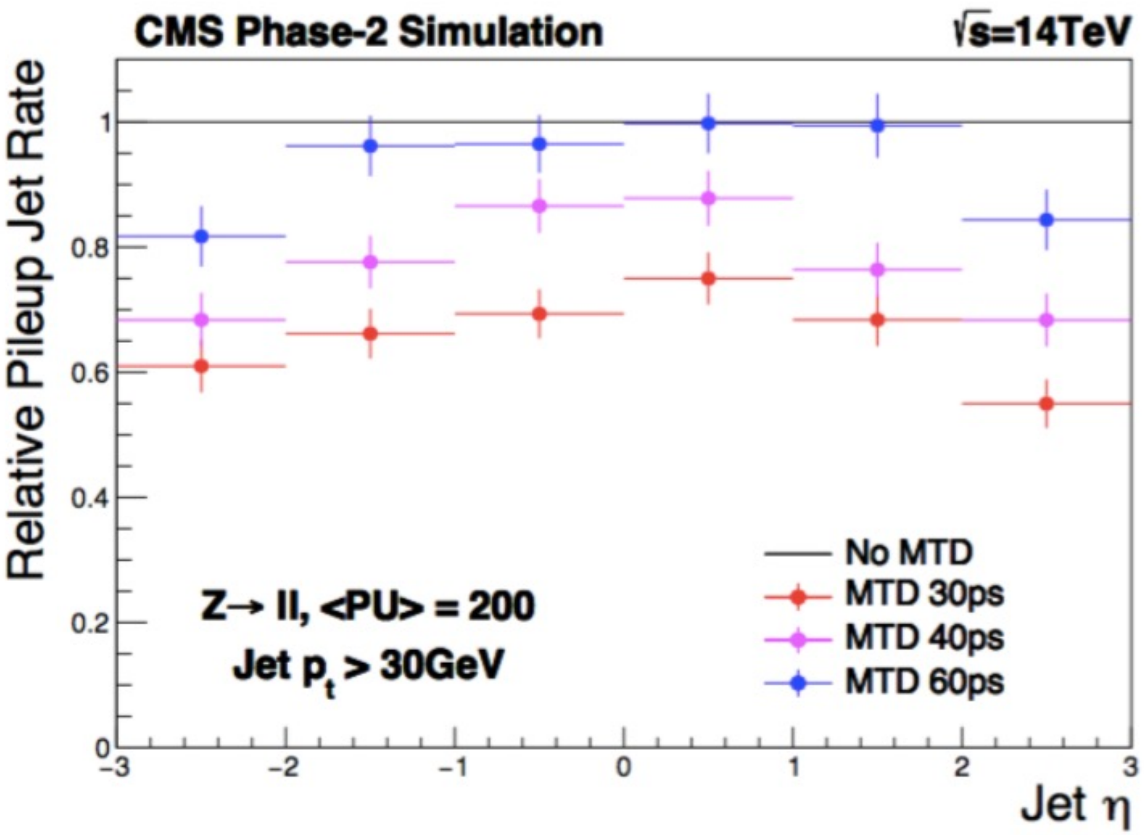




The display of an event with a Higgs boson produced in the VBF process on top of 200 pile-up collisions.

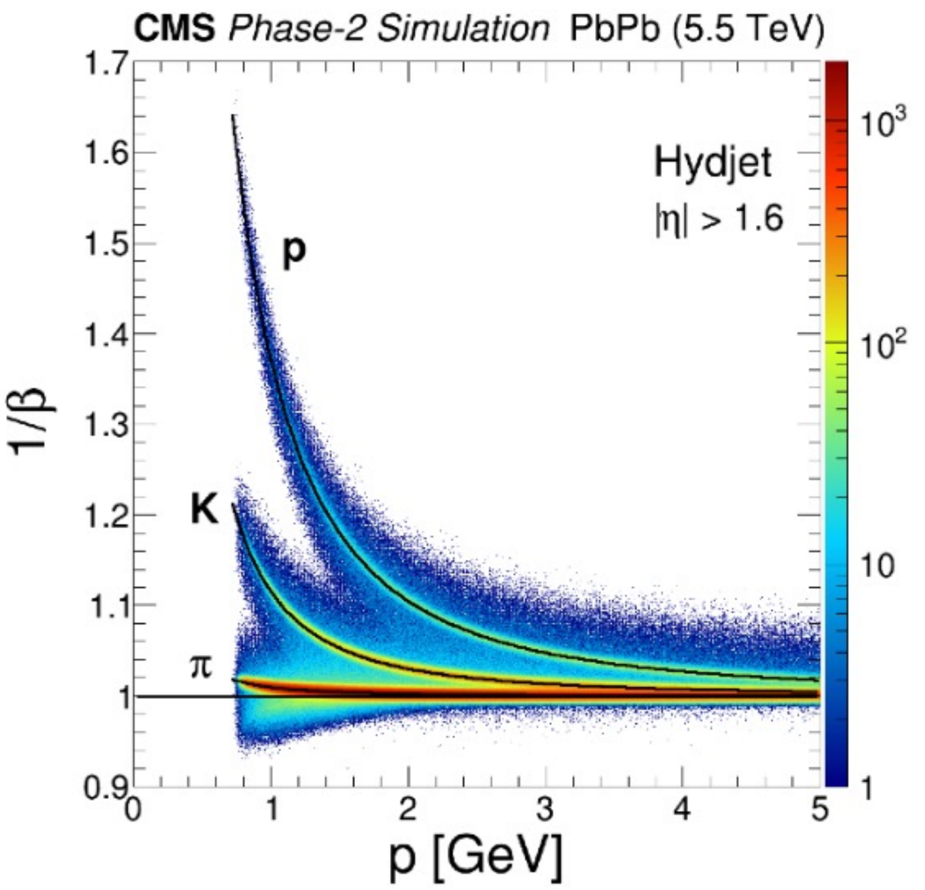
MTD Physics motivation: pile-up mitigation

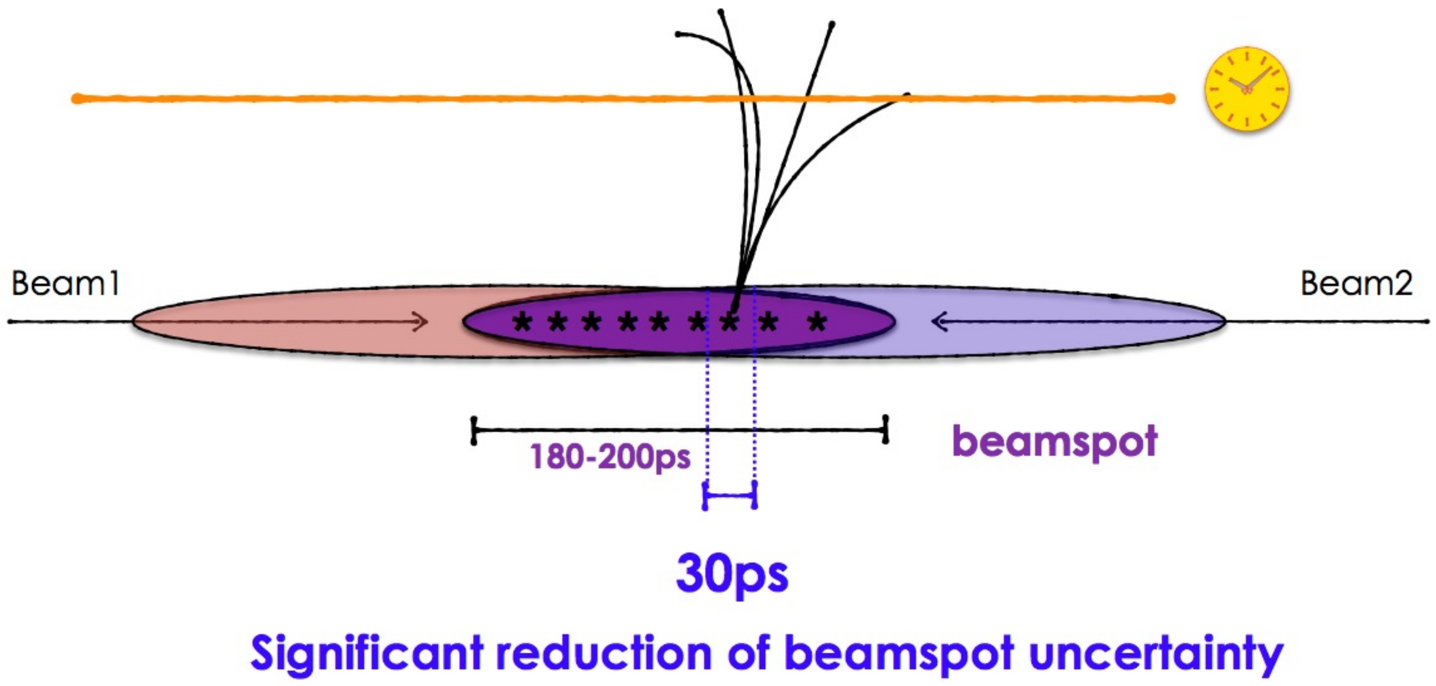




- The mitigation of pile up effect improves all physics objects
- 4D vertexing (position+time) can remove
  - Spurious pileup tracks from "isolation cone" around leptons
  - Rejects spurious jets formed from pileup particles.

MTD Physics motivation: particle ID



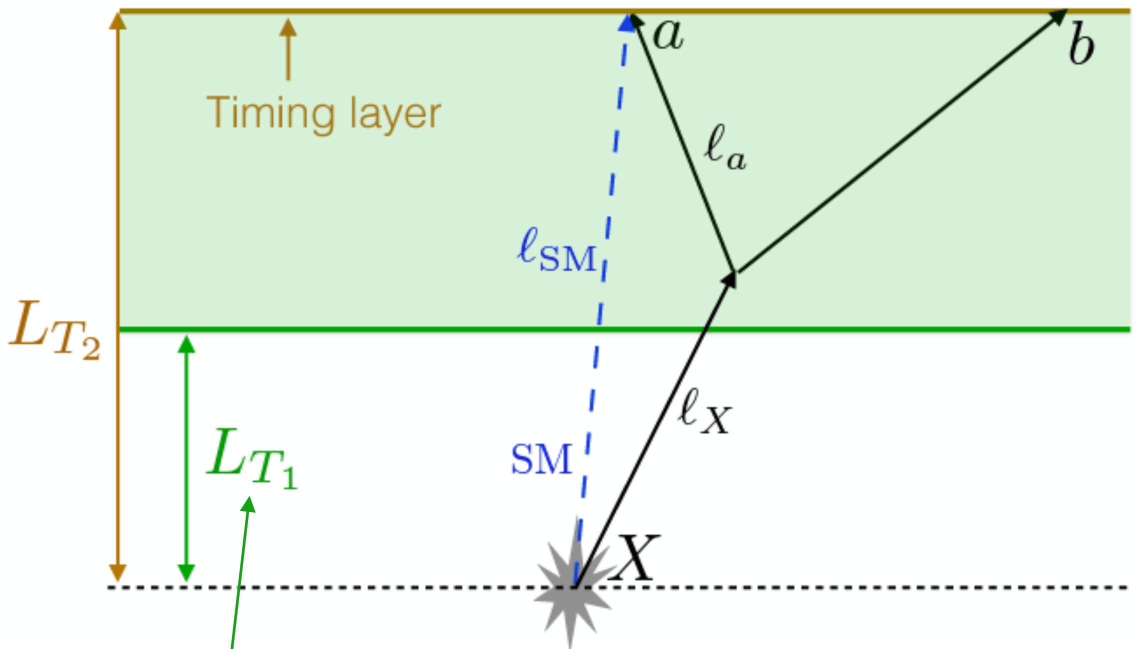


- MTD can provide significant improvement for particle ID
  - Heavy ion charm tag.
- Significant gains for searches for long-lived new particles.

4D vertex reconstruction of primary and secondary vertices

Provides a close kinematic for Long Lived Particles decaying within MTD

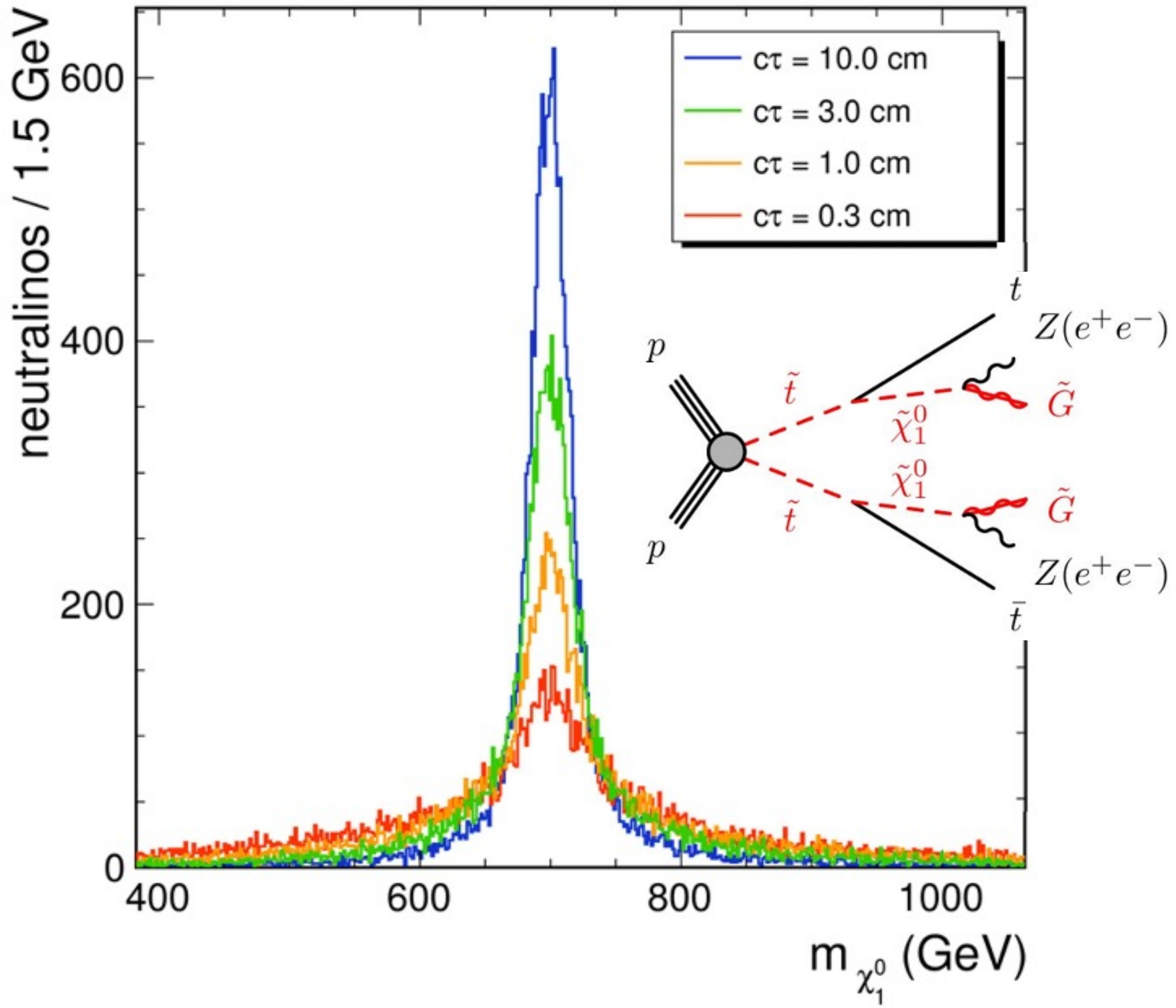
PRL 122.131801



$$\Delta t^i_{\mathrm{delay}} = \frac{\ell_X}{\beta_X} + \frac{\ell_i}{\beta_i} - \frac{\ell_{SM}}{\beta_{SM}}$$

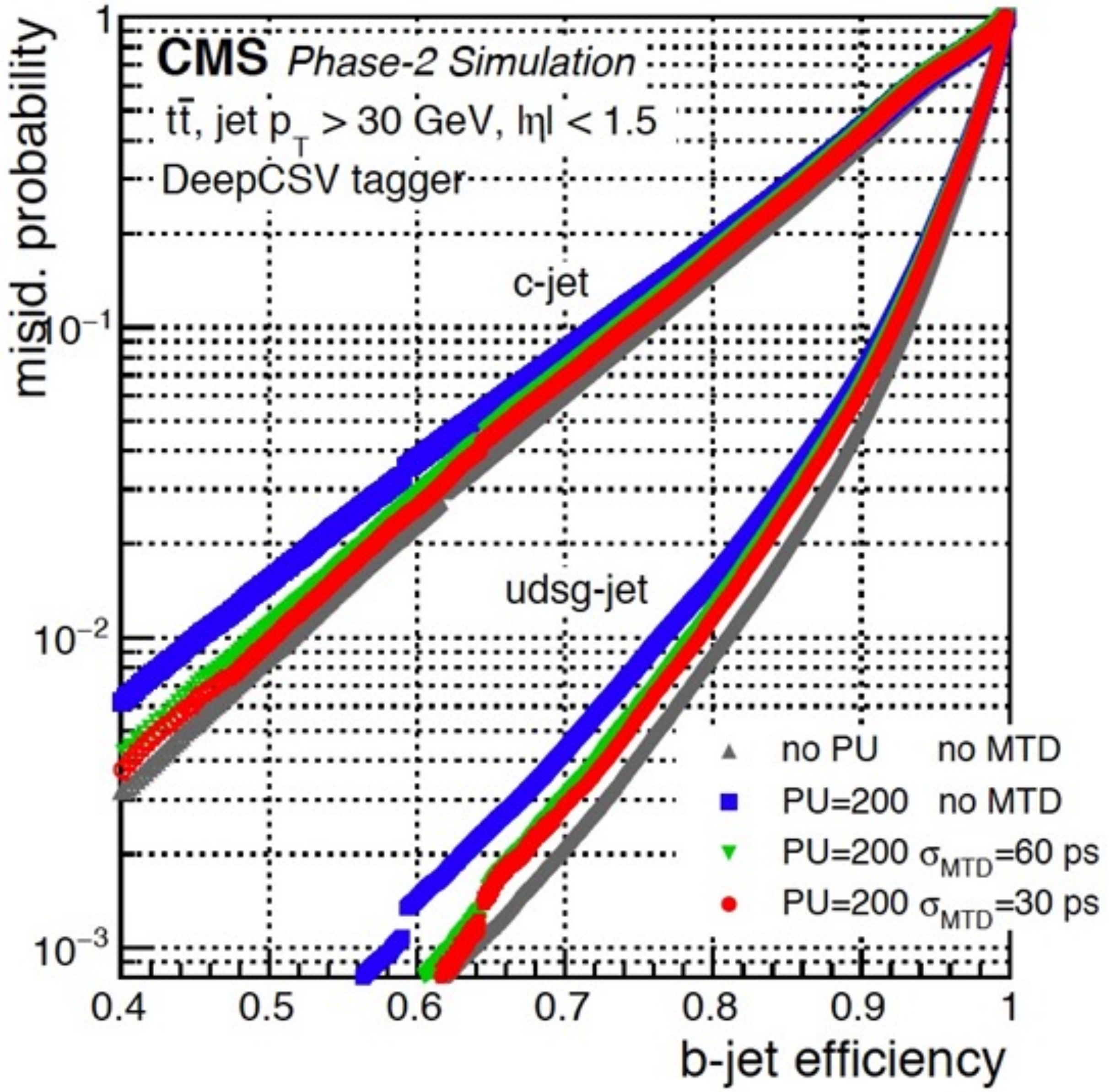
Minimal displacement requirement

700 GeV neutralino (SUSY)

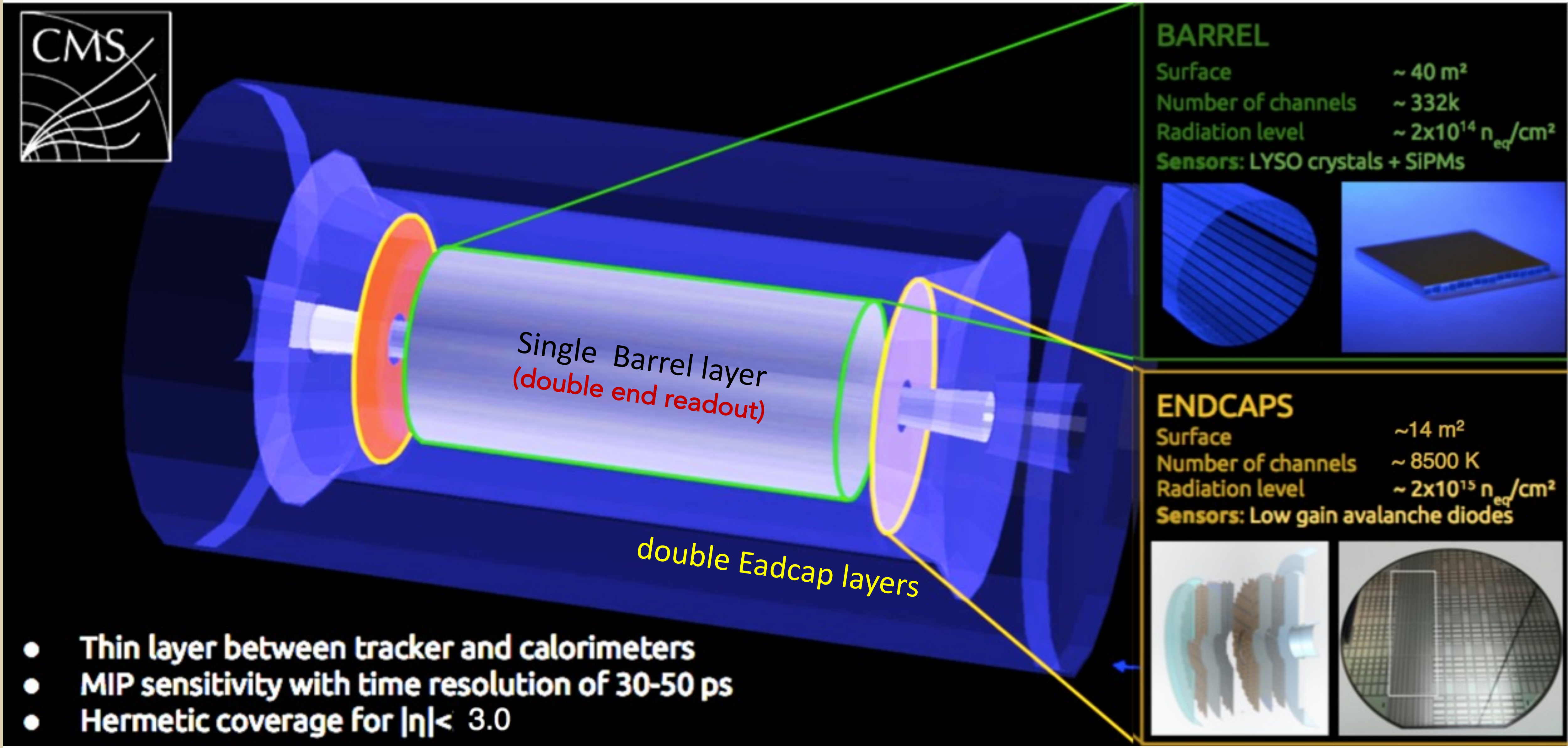


b-tagging performance with MTD

- b-quark jets are important
  - Primary decay mode of the Higgs, via $H \rightarrow b\bar{b}$
  - Exclusive decay mode of the top quark, via $t \rightarrow Wb$
- Significant improvement with MTD for b-quark identification efficiency
  - While reduced c-jet or light jets mistag rate

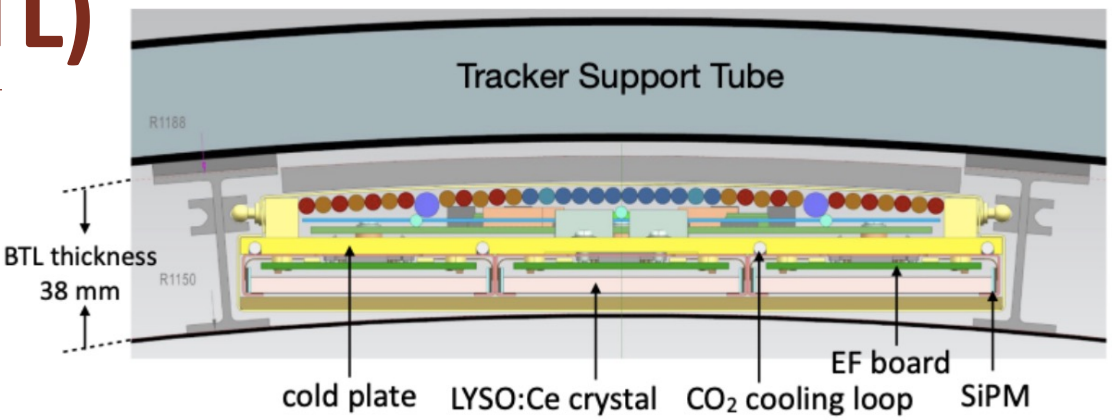


Mip Timing Detector (MTD)

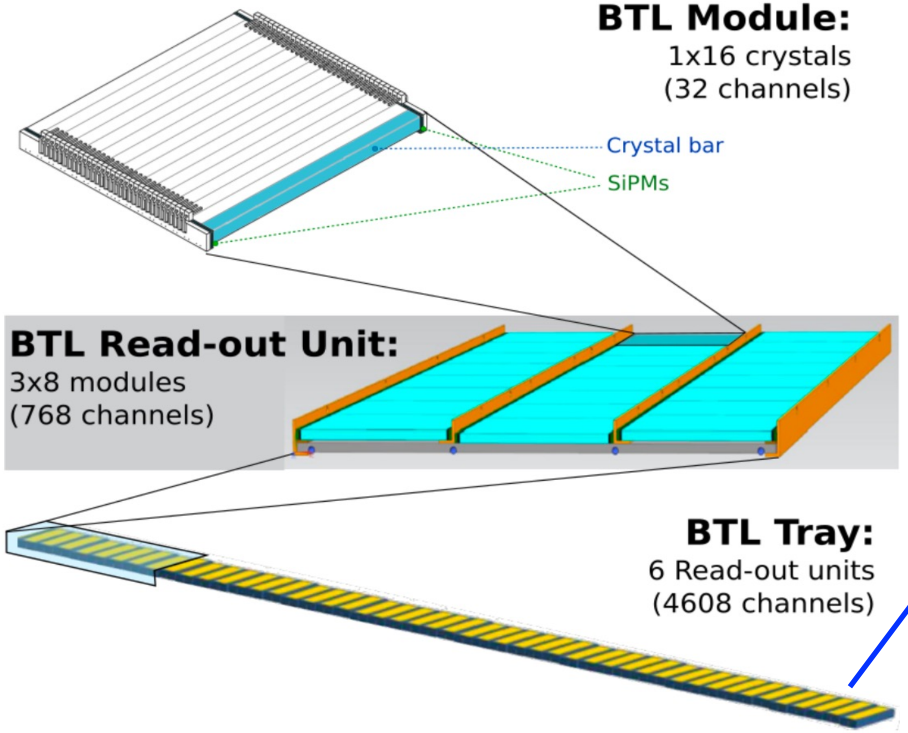


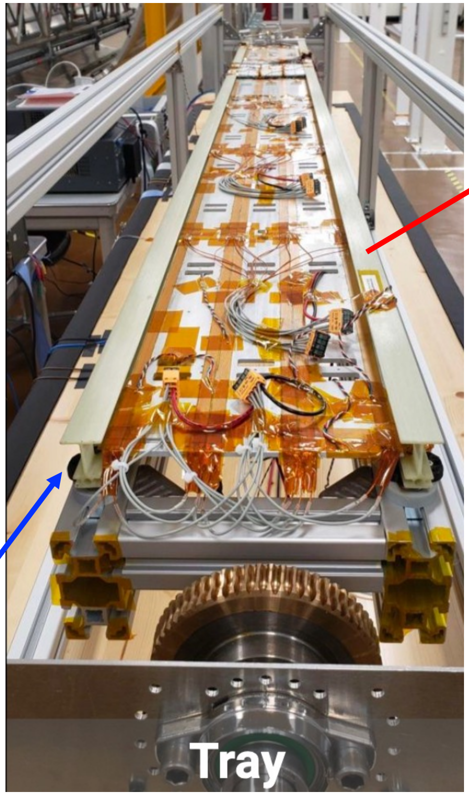
MTD Barrel Timing Layer (BTL)

- 3.8 cm thin cylindrical detector
  - located inside the tracker support tube, |η| < 1.45
  - ~5 m long, 38 m^2 surface



2 SiPMs per crystal

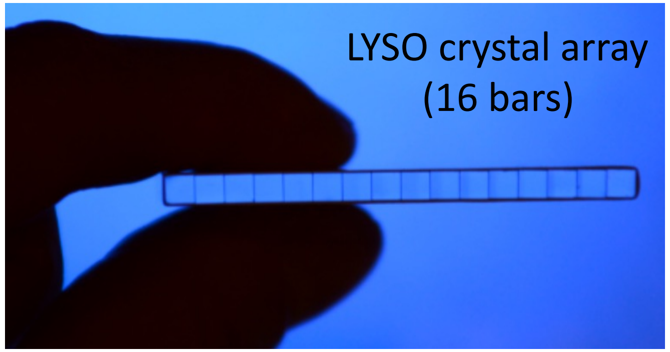


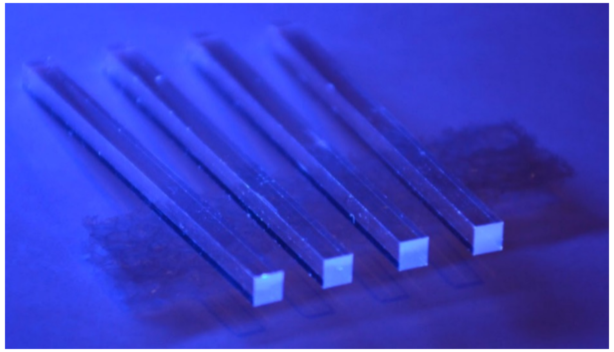


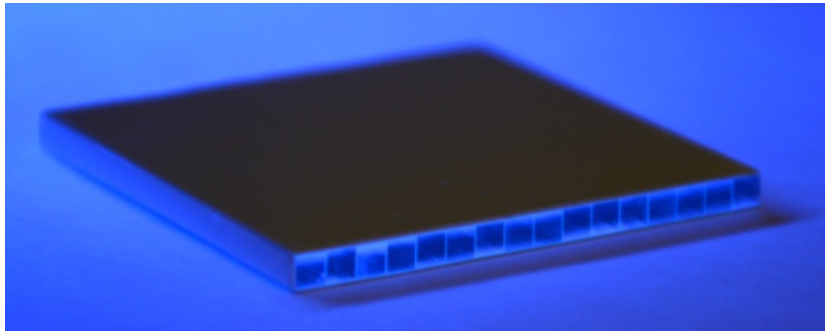
- BTL construction: starting in early 2024!

BTL sensors : LYSO crystal

- LYSO crystal bars (166k)
  - Cerium-doped lutetium yttrium orthosilicate (LYSO:Ce) scintillation medium
  - Well established in PET applications and vendors widely available
  - High radiation tolerance
  - τ_{rise} : ~100 ps, τ_{decay} : ~ 40 ns
  - High Light Yield : 40000 γ/MeV

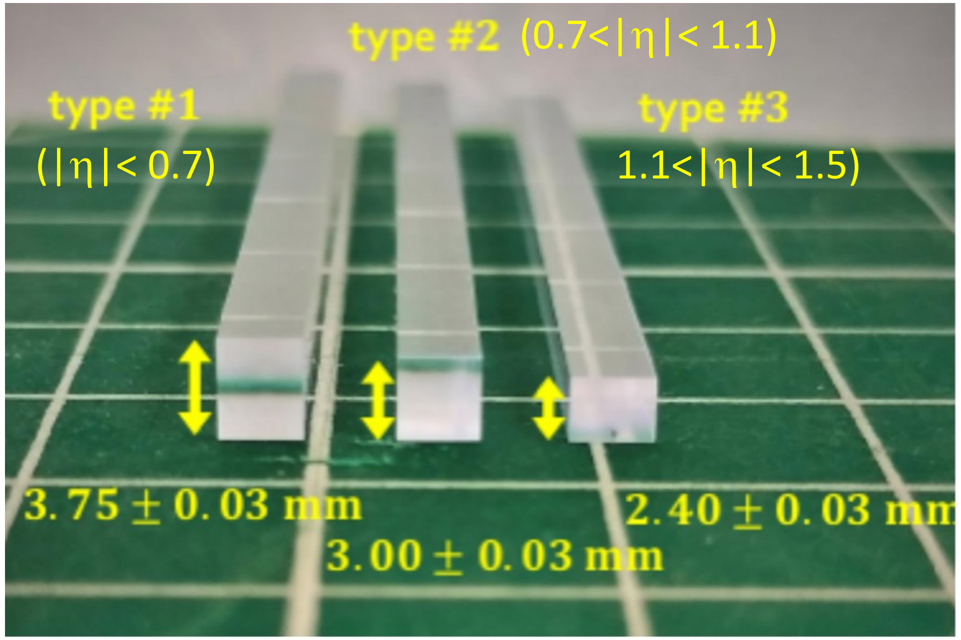






- LYSO current status
  - Single vendor selected
    - Considerably better offer
    - One of best vendor for performance-wise
    - Reliable vendor (large production capacity)
  - Pre-production in progress
    - Ordered in March (2% of the total LYSO arrays)
    - QA/QC and construction database ready

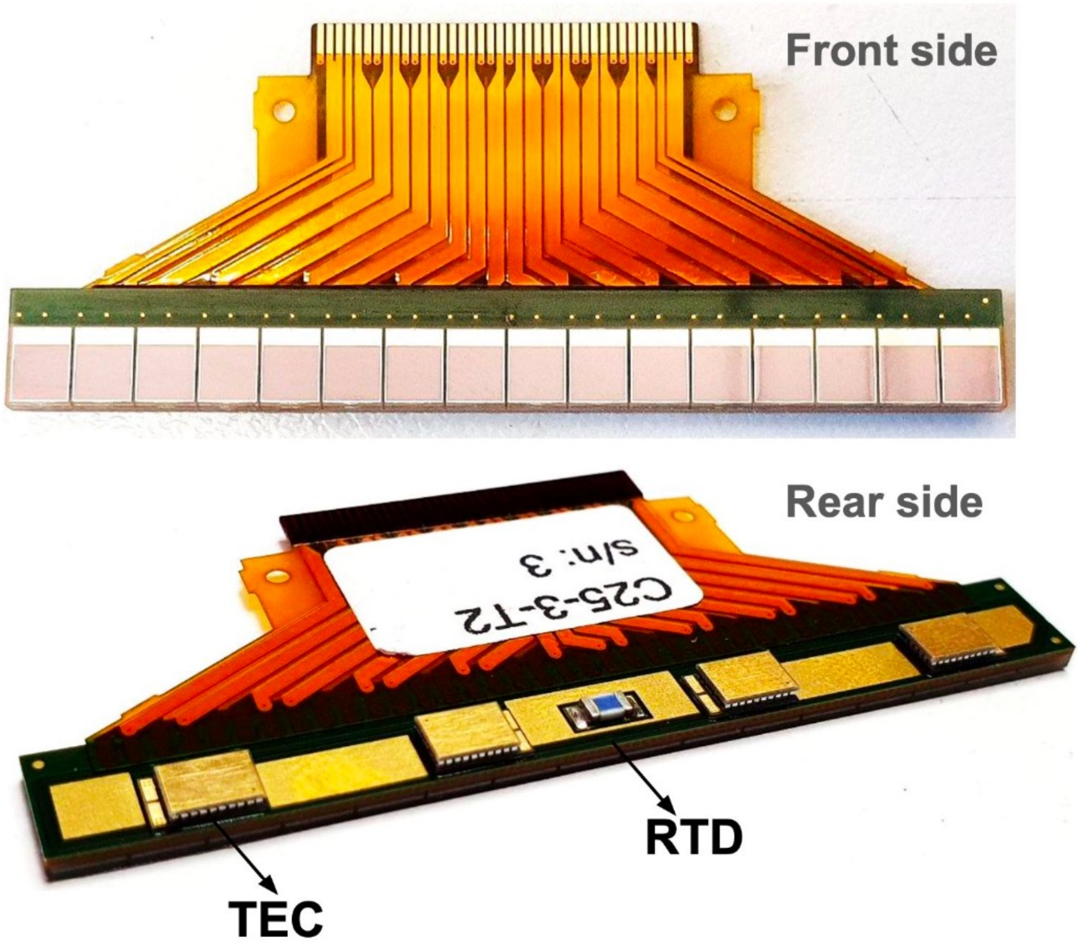
Maximize the crystal light output for 3 η regions



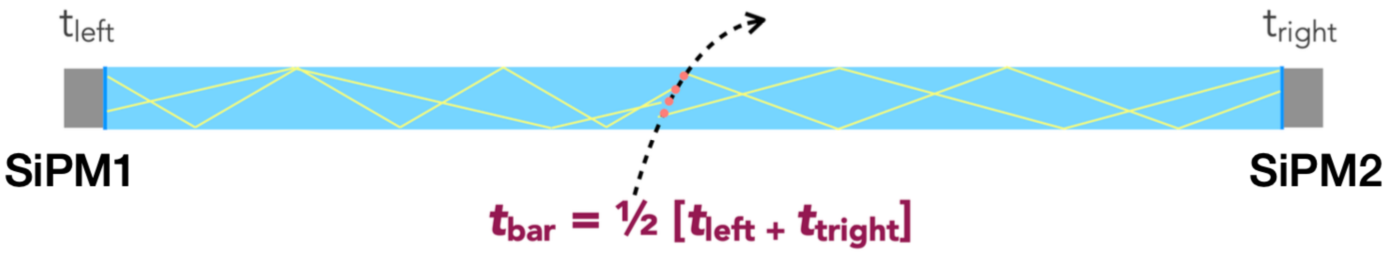
BTL sensors : SiPM

- SiPM (166k x 2 = 332k channel)
  - Well consolidated technology
  - Photon Detection Efficiency (PDE) : 20–40%
  - Compact, robust, insensitive to magnetic fields
  - Good radiation hardness
  - Fast recovery time <10 ns
  - High dynamic range (10^5)
- SiPM current status
  - Optimized cell size (25 µm) as a default for BTL
    - Additional performance gain to boost signal
  - SiPM die size (3.8×2.9 mm^2) fixed to match with the thickest LYSO geometry
- SiPM plans
  - Tender starts in July
  - Sign the production contract in September
  - First batch delivered ~ Feb. 2024 (for 7 months)

SiPM Module



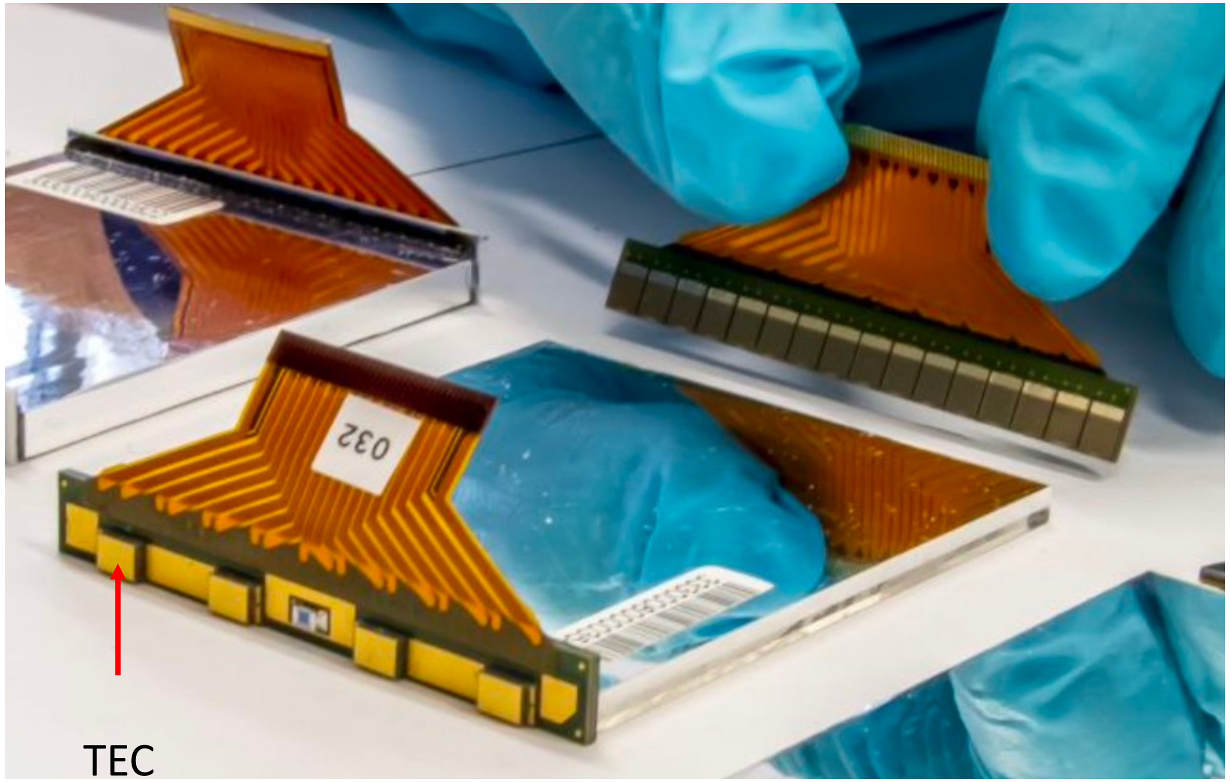
BTL sensors : LYSO crystal and SiPM

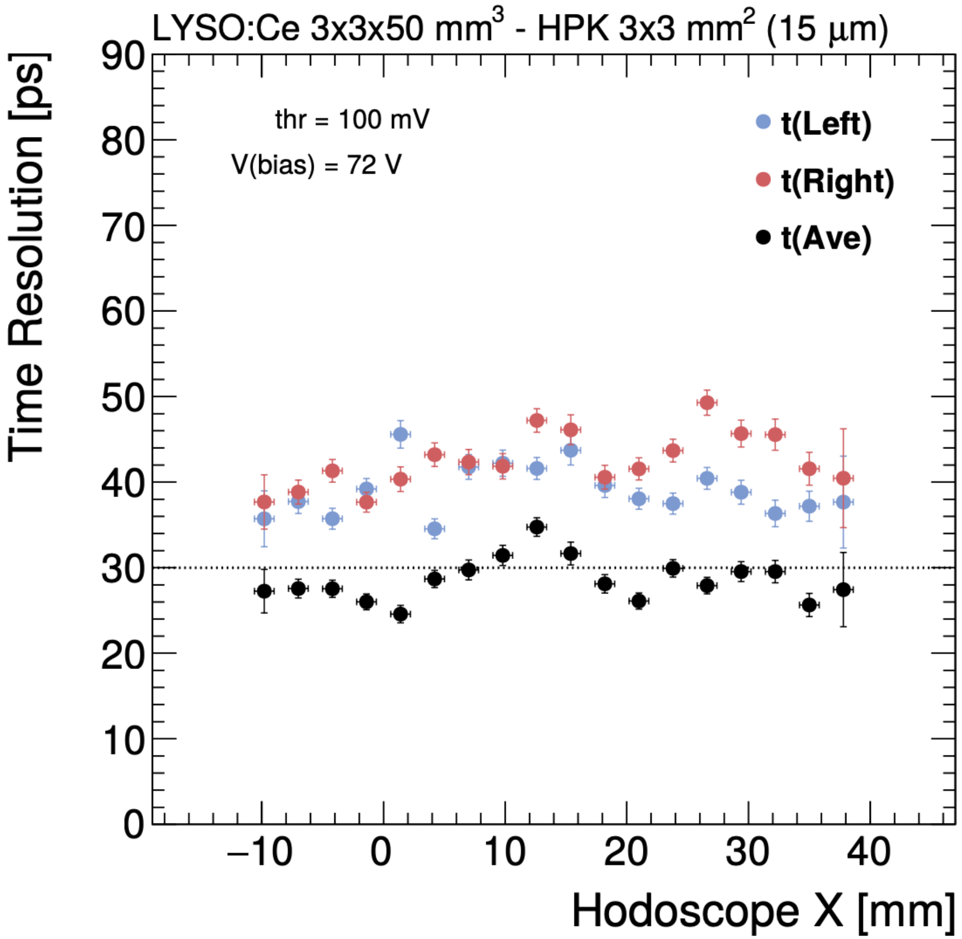


LYSO bars with double end readout:

- Improve timing resolution by a factor of $\sqrt{2}$ than single-end

Sensor Module (LYSO + SiPM & TEC)

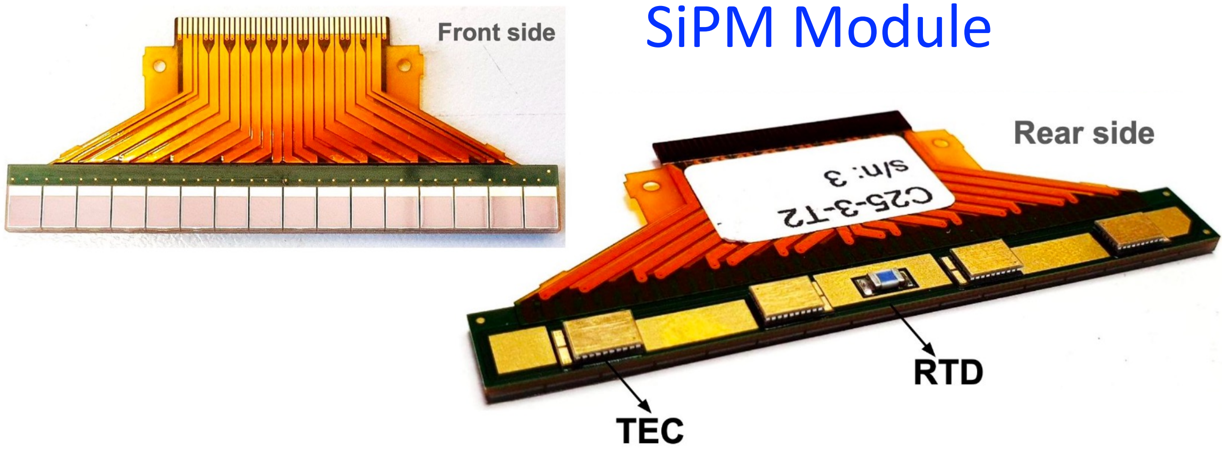


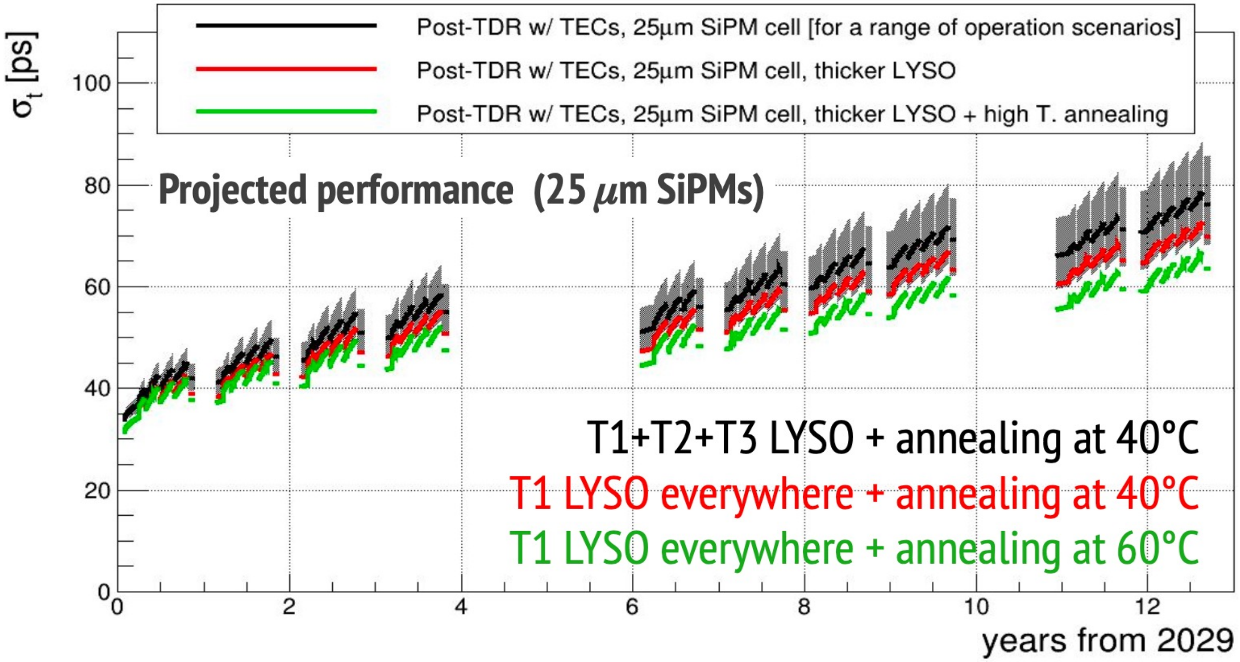


BTL Performance Optimization

- A dark count in the SiPM corresponds to a single cell firing due to a thermally generated electron.
- The dark count rate (DCR)
  - Proportional to the active area of the SiPM
    - **Lowering $V_{over\ voltage}$ and optimizing S/N ratio**
      ~ factor 2 less DCR
  - Decreasing at lower temperatures by about a factor two every 7–10 ◦C
    - **Further lowering SiPM's temperature to -45°C using Thermoelectric coolers (TEC)**
      ~ factor 2-3 less DCR
  - Increasing with radiation damage
    - **Annealing at room +65 °C during LHC shutdown and technical stops** ~ factor 2 less DCR
    - **Noise filtering with signal processing technique DLED in TOFHIR** ~ factor 2 less DCR

SiPM Module

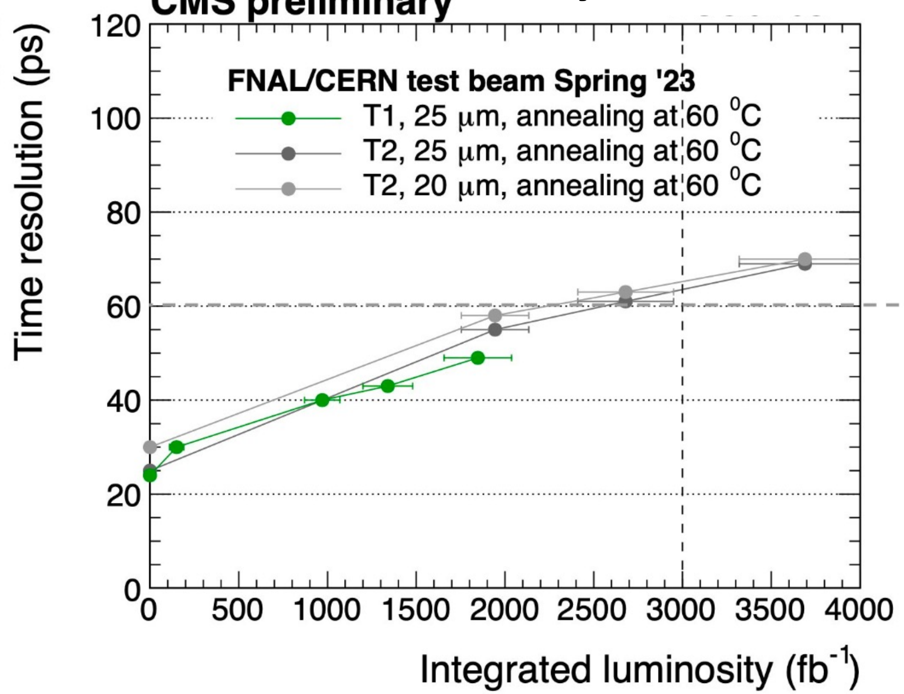




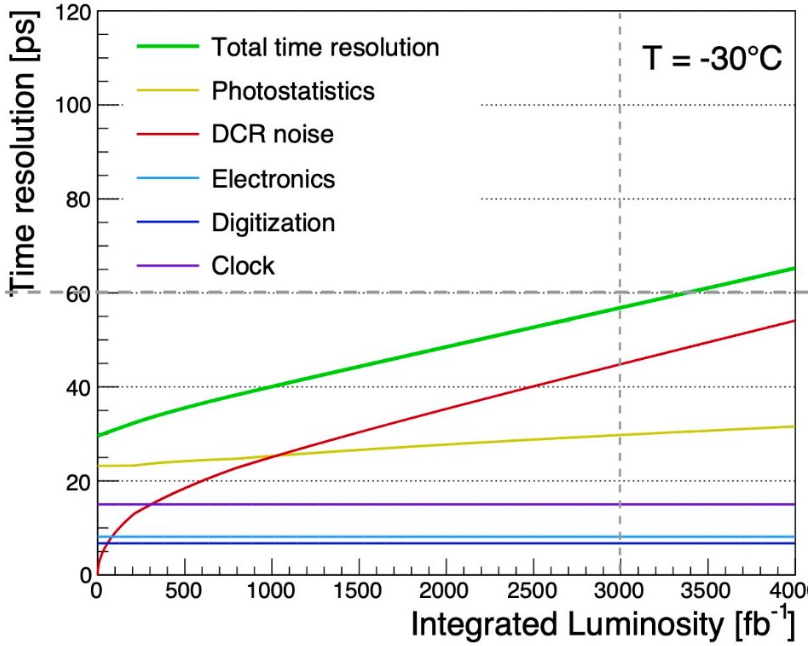
The BTL prototyping phase is completed

- Changing configuration of BTL with respect to the TDR (**Almost same performance!**)
  - Smart thermal management with TECs (additional cooling and annealing)
  - SiPM cell size choice : 25 µm for boosting signal
  - Thicker LYSO arrays for larger energy deposits
  - TOFHIR2C optimization for electronic noise reductions

May '23 TB result



CMS MTD TDR

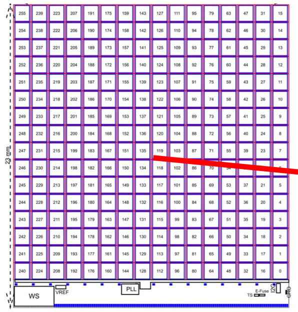


close to TDR performance

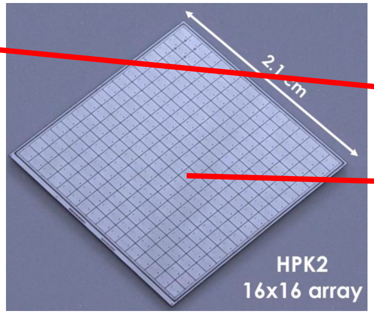
- Ready for starting procurement and the production & assembly phase

MTD Endcap Timing Layer (ETL)

- Two double- sided disks for each side
  - Maximize geometrical acceptance (85% per disk)
  - Coverage : 1.6 < |η| < 3.0
  - Average of 1.8 hits per track
  - **Time resolution per track < 35 ps**
    - based on single hit resolution < 50 ps
- Low-Gain Avalanche Diode (LGAD) sensor bump bonded readout ASIC (ETROC)

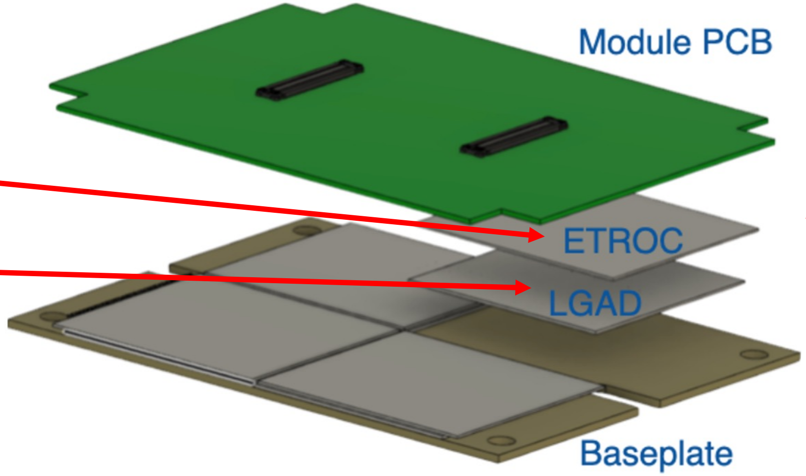


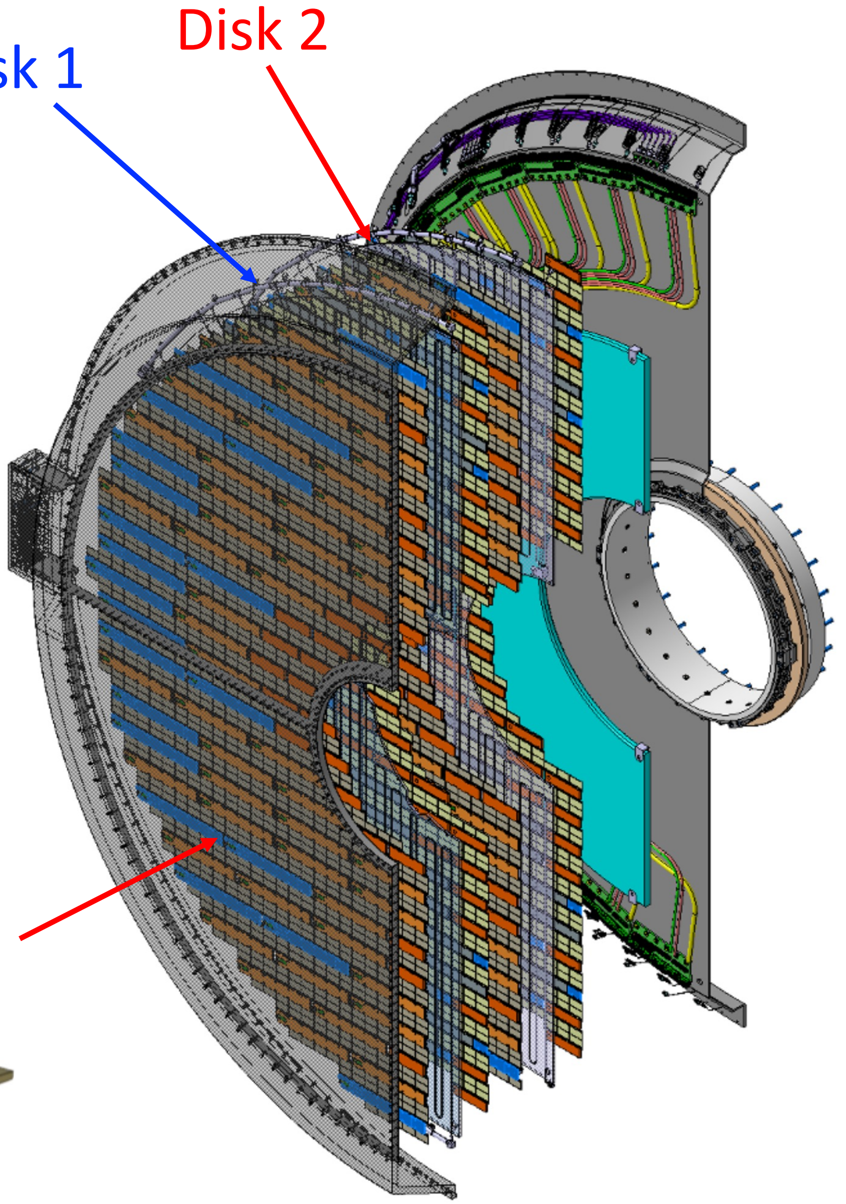
ETROC (ASIC)



LGAD sensor

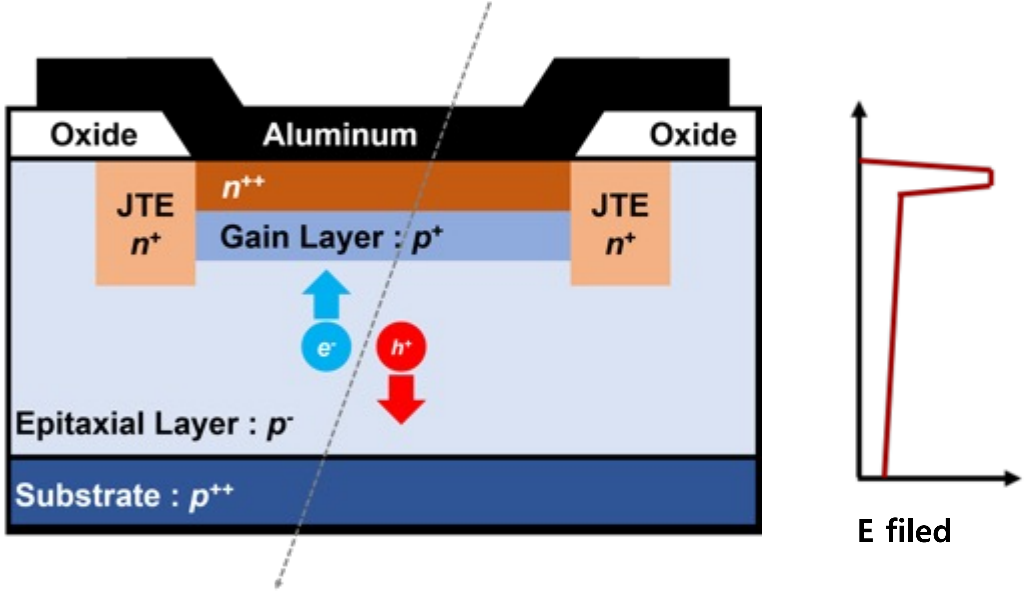
8000 modules (4 sensors each)

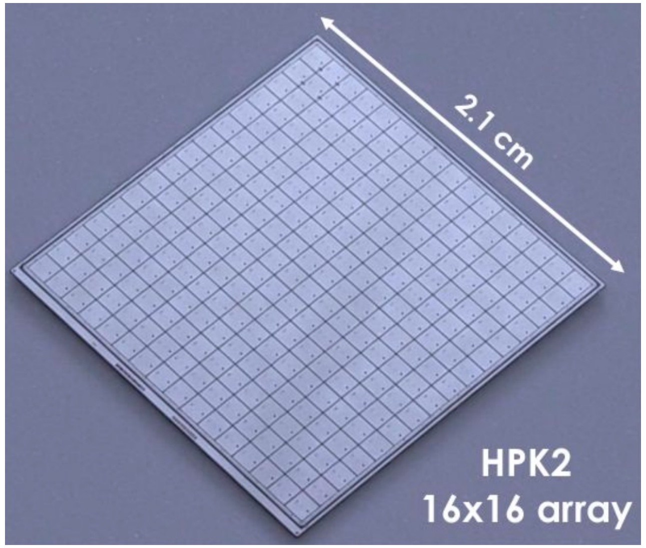




Low Gain Avalanche Diode (LGAD) sensors

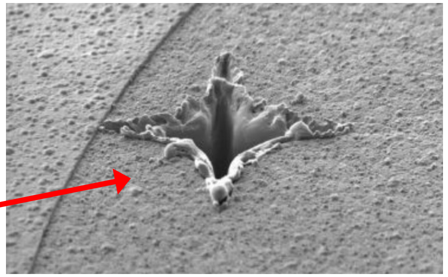
- LGAD characteristics (16x16 pixel matrix, 1.3x1.3 mm^2 pixel size)
  - Precision position reconstruction and timing resolution
  - Highly improved radiation tolerance
  - Moderate gain factor (10-30) to maximize S/N ratio -> Large signals with low noise
  - Thin implanted gain layer of overall thickness of 35–50 μm
  - Gain uniformity (>8 fC of charge)
- The additional Gain layer: highly boron-doped thin layer at the n-p junction
  - Generates the high field necessary to achieve charge multiplication.

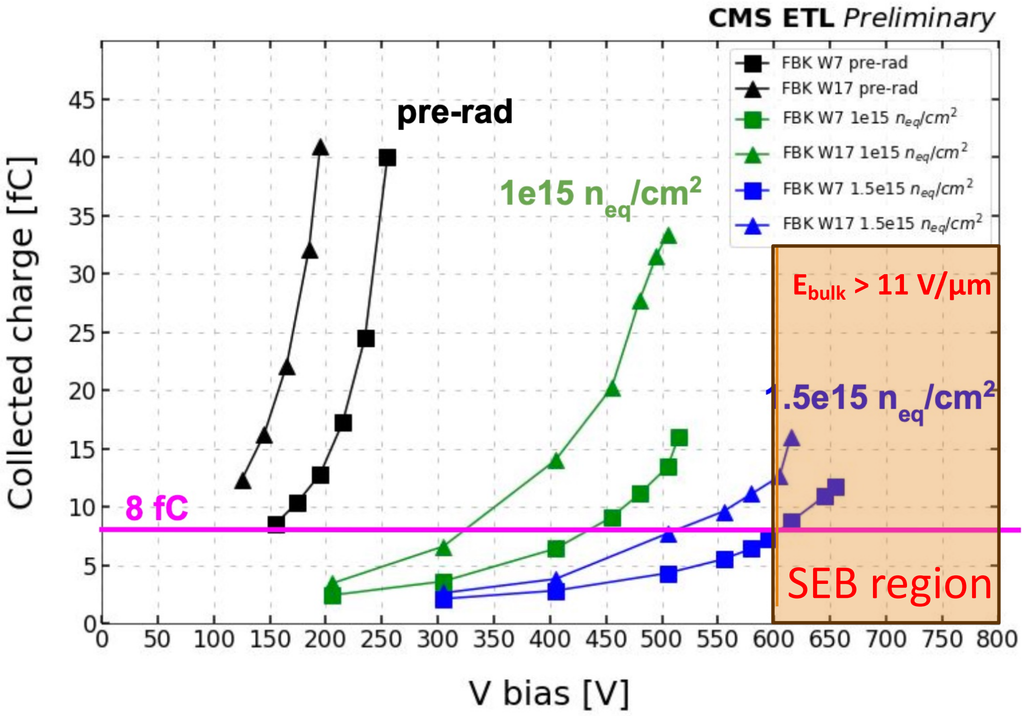


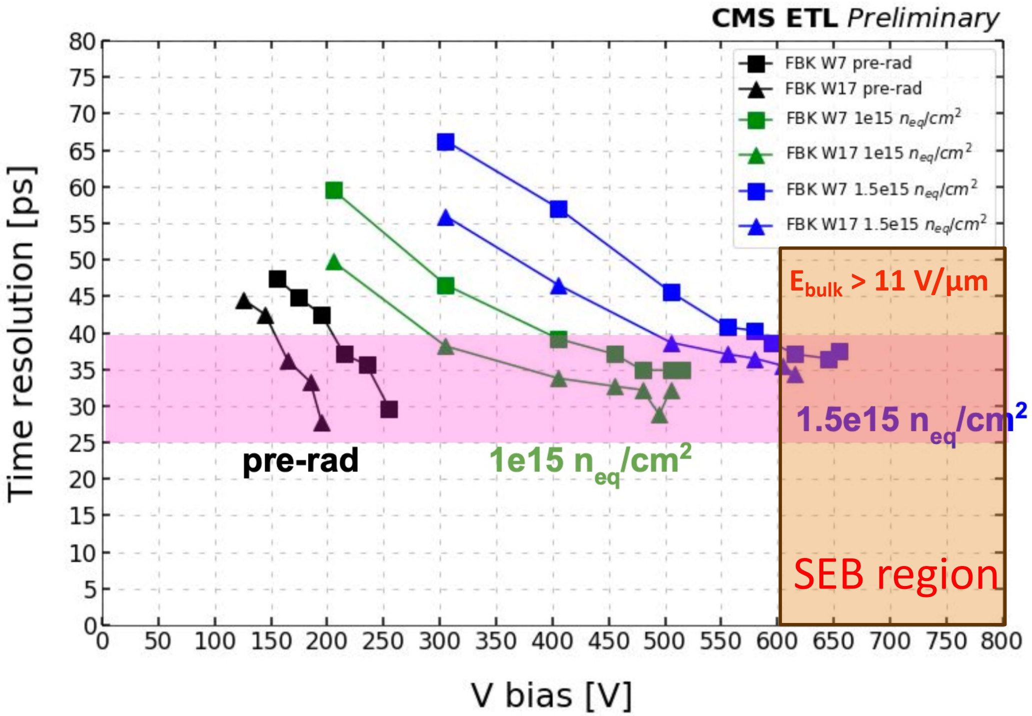


Performance tests for LGAD sensors

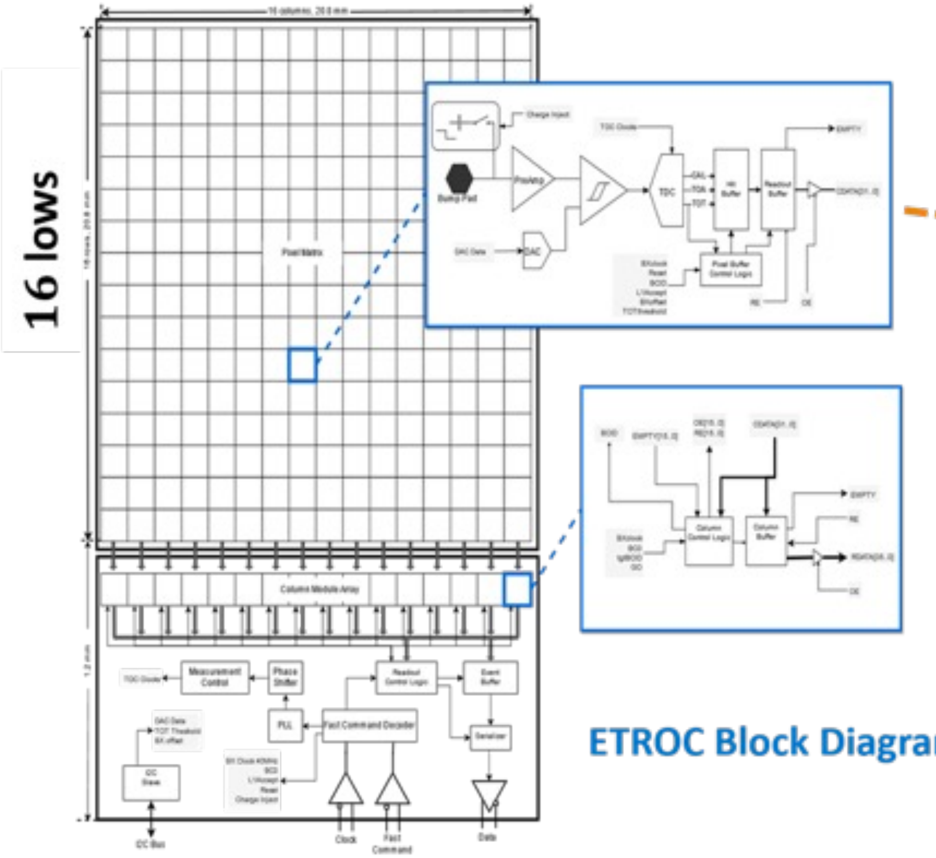
- Completed Market Survey for the procurement of the final LGADs Prototype.
  - Qualified 4 vendors for production of the final LGAD sensors
- Irradiated FBK sensors measured with a beta-source (Sr90) setup
  - Collected charge and time resolution was satisfied with requirements
  - Fully recover performance by increasing the bias voltage
- Single Event Burn-out (SEB) observed for $E_{bulk} > 11$ V/μm



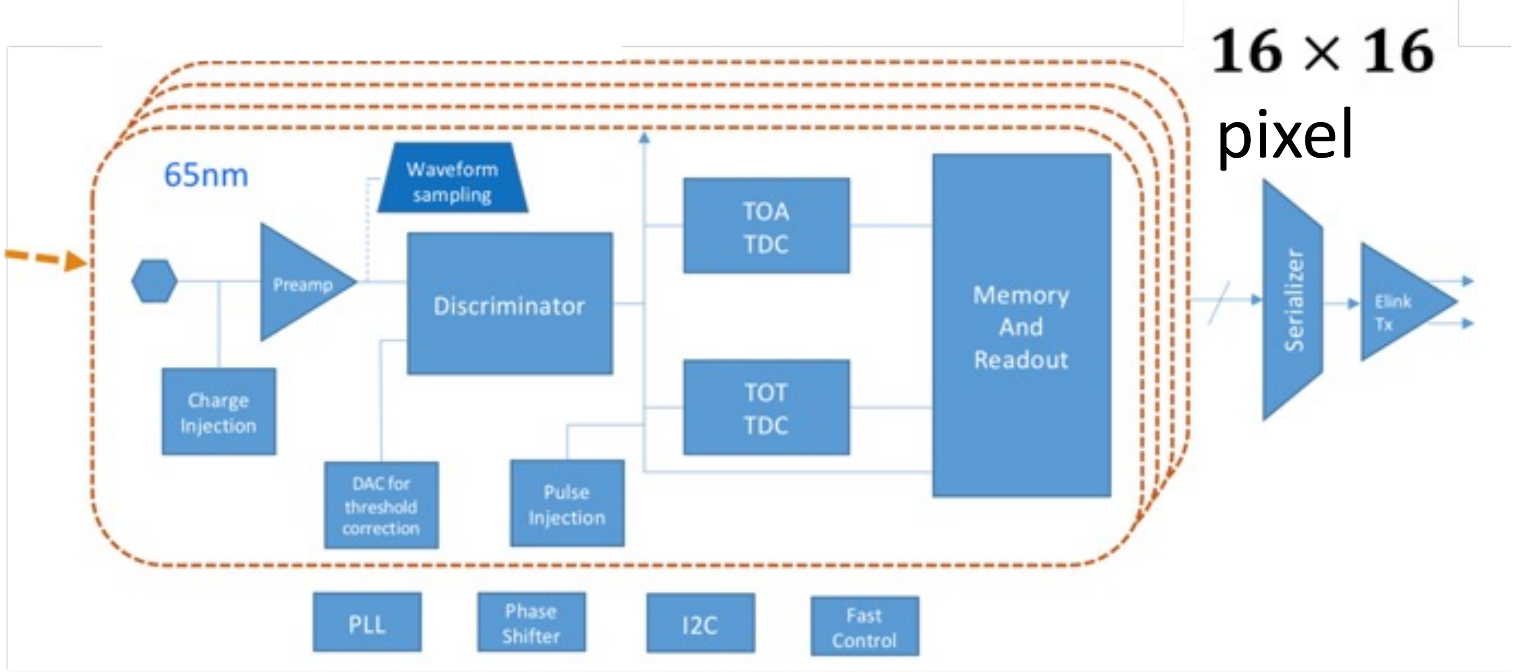




Endcap Timing Layer ReadOut Chip (ETROC)



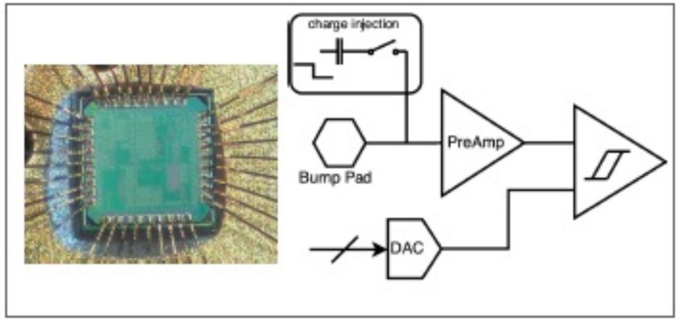
ETROC Block Diagram



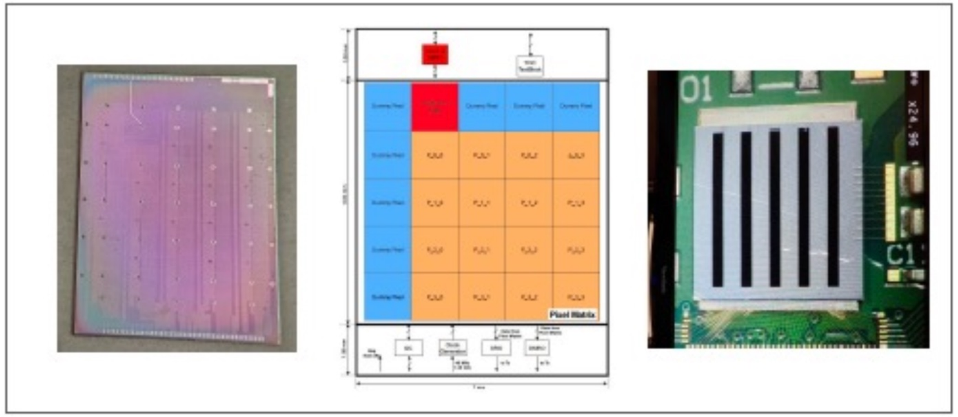
- Total ETROC size: 16 X 16 pixel cell
  - One pixel cell size: 1.3mm X 1.3mm to match the LGAD sensor pixel size
- Targeting signal charge (1MIP): 6 - 20 fC
- TDC (time-to-digital converter) range
  - ~5 ns TOA (time of arrival)
  - ~10 ns TOT (time over threshold)

ETROC Development Plan

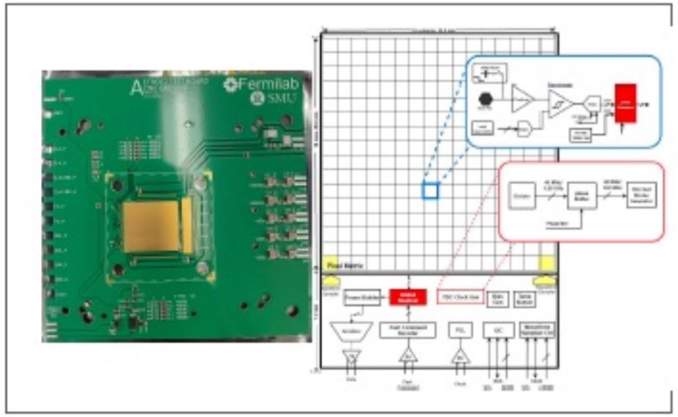
2018	2020	2023
ETROC0 (1x1)	ETROC1 (4x4)	ETROC2 (16x16)



- Analog front-end only
- Wire-bonded with LGAD sensor reached ~33 ps time resolution per hit with preamp. waveforms
- Passed 100 Mrad TID



- Added low-power TDC and 4x4 H-tree for clock distribution
- Bump-bonded with LGAD sensor reached ~42 ps time resolution per hit with TDC data



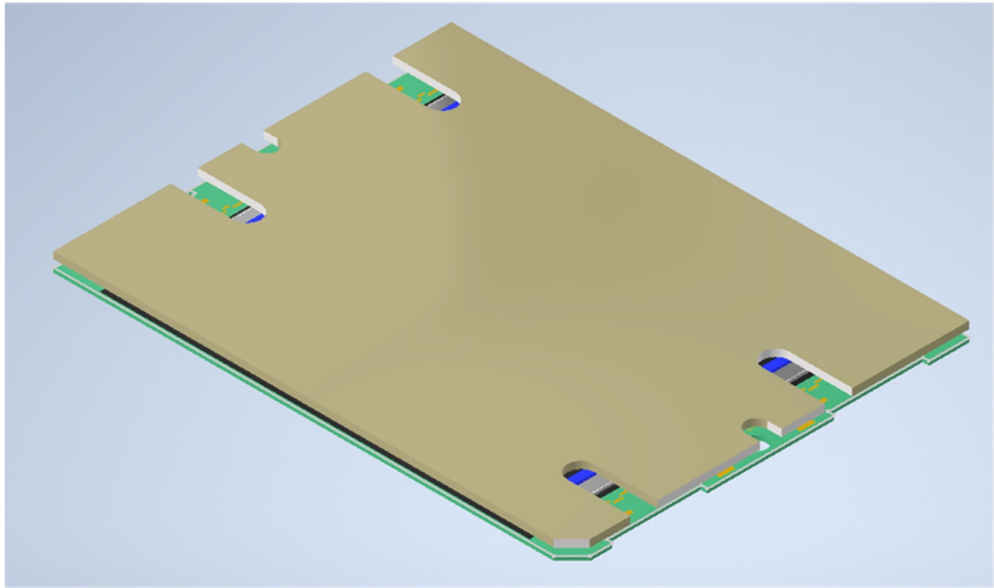
- First full-size chip (16x16) with all desired functionalities included
- All analog blocks silicon-proven; all digital blocks were verified in FPGA emulator

❑ ETROC3 : Final chip

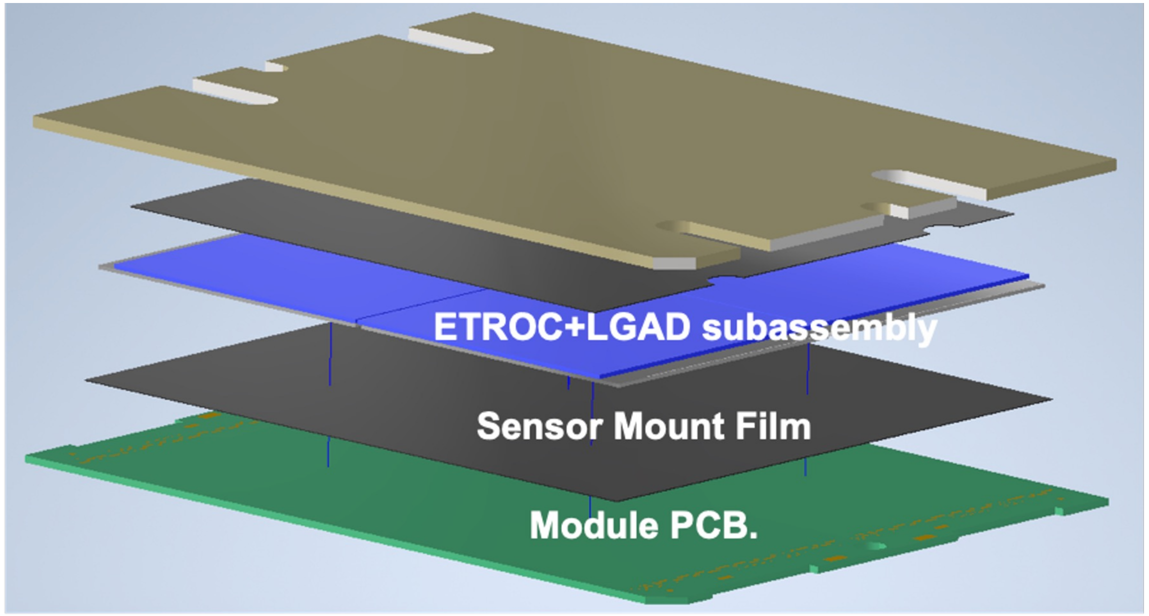
- The same functionalities as ETROC2, with improvements based on what will be learned from extensive ETROC2 testing
- Submission scheduled for 2024

ETL Module design overview

- Module design overview



PCB + subassembly

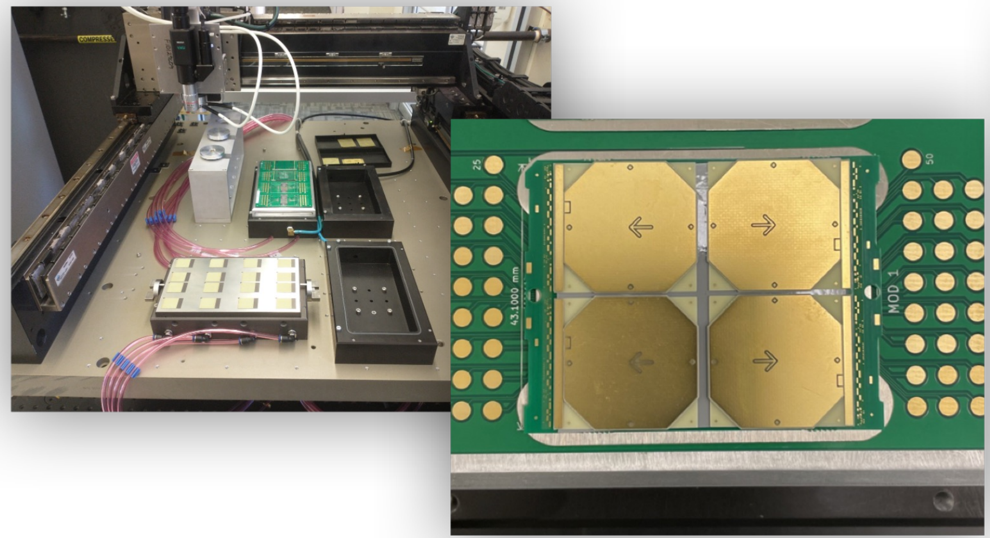


Basic scheme of a module

- Module PCB
  - Printed circuit board that serves as the power and readout interface for the module
- 4x ETROC+LGAD subassembly
  - 2x2 arrangement of bump-bonded assemblies
  - Each of a 16x16 pixel LGAD sensor and an “ETROC” readout chip

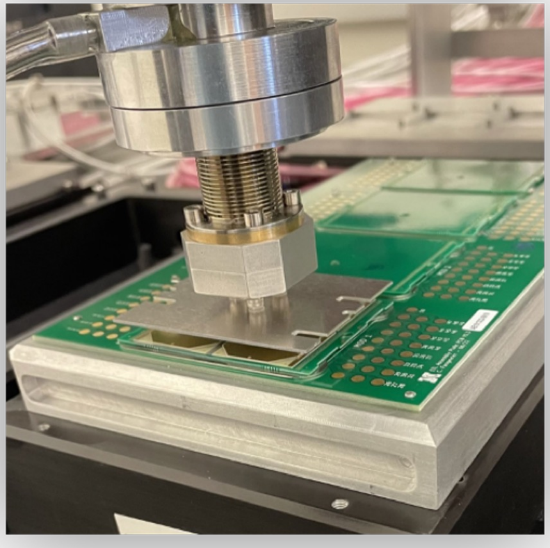
Assembling the ETL Modules

- The ETL detector will need ~8 thousand modules
- Each module will be made of 4 LGAD sensors and ETROCs
- An automated robotic gantry will be used for precision placement at the 10 micron level
- All modules will then be assembled into disks at CERN



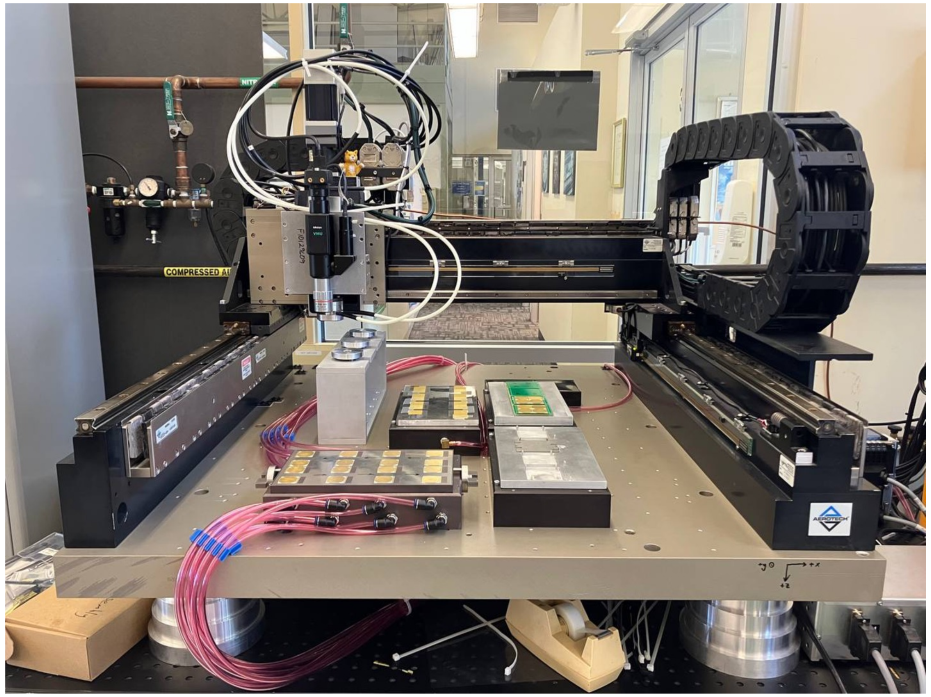
Pick & place sensor + PCB

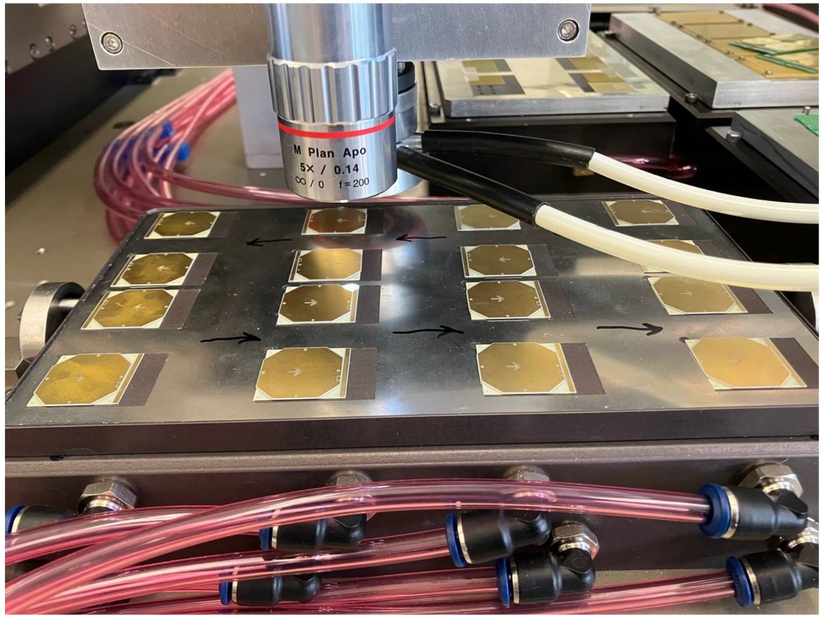
Wirebond and encapsulating

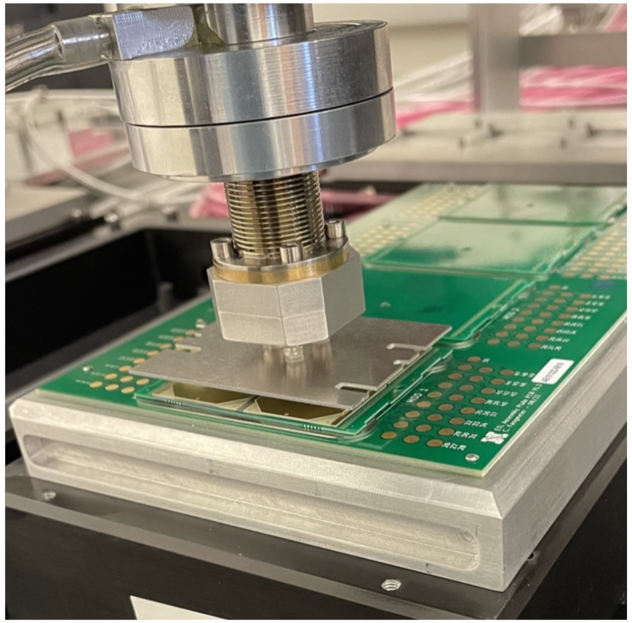


Apply film to baseplate, pick and place, and cure film

ETL Module assembly with Gantry







- Aerotech 3+1 axis gantries were used for ETL module assembly.
- Based on a vacuum pump
  - Modules PCBs and sensors are securely fixed.
  - Vacuum arm is used for picking and moving sub-assembly.
- The robot arm rail is moved using magnetic force, enabling precise operations
- The camera measures and automatically corrects the position, rotation, and tilt of the sensors

Summary

- The CMS MIP Timing Detector will measure precision timing of charged particles produced inside CMS.
  - Provides significant pileup mitigation, furthering the experiment's mission in the HL-LHC era.
  - Brings new capabilities to CMS that could help to search new phenomena in the HL-LHC.
- BTL will be instrumented with LYSO crystals + SiPMs, read-out by the TOFHIR
  - Beginning of life performance (30-40 ps) within requirements
  - End-of-life performance (~ 60 ps) close to requirements
  - The BTL prototyping phase is completed and now entering production phase
- ETL will be instrumented with LGADs read out by the ETROC
  - Performance at beginning and end of life within requirements (single hit resolution < 50 ps)
  - LGAD market survey done → Will enter a tender process soon.
  - Full-scale 16x16 ETROC2 arrived and Initial system test with bare ETROC2 in progress.
- Common MTD DAQ system is being developed together for the ETL and BTL.
- Mechanical engineering of the full detector system is preparing.

Backup

Detector module : BTL