Preliminary Design of Waveform Digitizer for Jinping Neutrino Experiment at CJPL

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Author: Lin Jiang, Jingjun Wen, Tao Xue, Liangjun Wei, Xiaowei Guo, Haoyan Yang, Qiutong Pan, Litao Yang, Jianmin Li, Yinong Liu

Motivation

The proposed Jinping Neutrino Experiment (JNE) aims to study MeV-scale neutrinos, including solar neutrinos, geoneutrinos, and supernova relic neutrinos, etc. A 1-ton detector, built as a prototype of the JNE at CJPL-I hall A, has been running since 2017. This paper reports the preliminary design of waveform digitizer "WRX0608A1" for JNE at CJPL. Single block digitizer can support 6-channels 1GSPS, 13-bit sampling.

Hardware Design

- PMT signal characteristics
  - PMT:R1828-01 from Hamamatsu
  - The effective bandwidth of the measured dark noise signal can reach 300MHz
- WRX0608A1
  - Based on 6U-CPCI standard
  - 12-layer PCB, board material is FR-4
  - Six 1GSPS/13-bit channels
  - Based on Xilinx 7K325T FPGA
  - DC coupling with 500MHz anti-aliasing filter
  - ZYNQBee2 based on ZYNQ7010 is used for system slow control
  - 64-bit DDR3 SDRAM with a maximum capacity of 4GB
  - Aurora based 10Gbps backplane transport link
  - Two QSFP+ ports on the front panel, theoretical transmission bandwidth 80Gbps

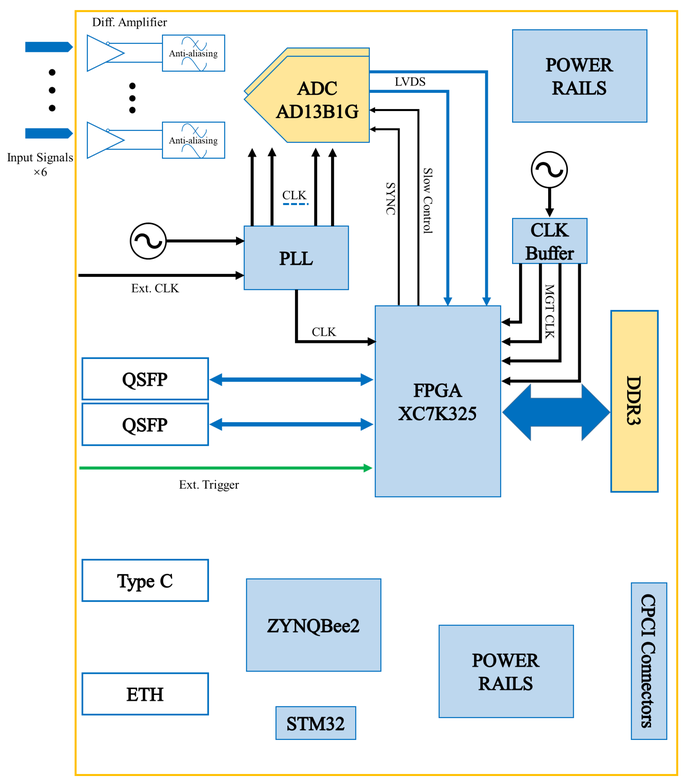

Fig. The architecture of waveform digitizer WRX0608A1.

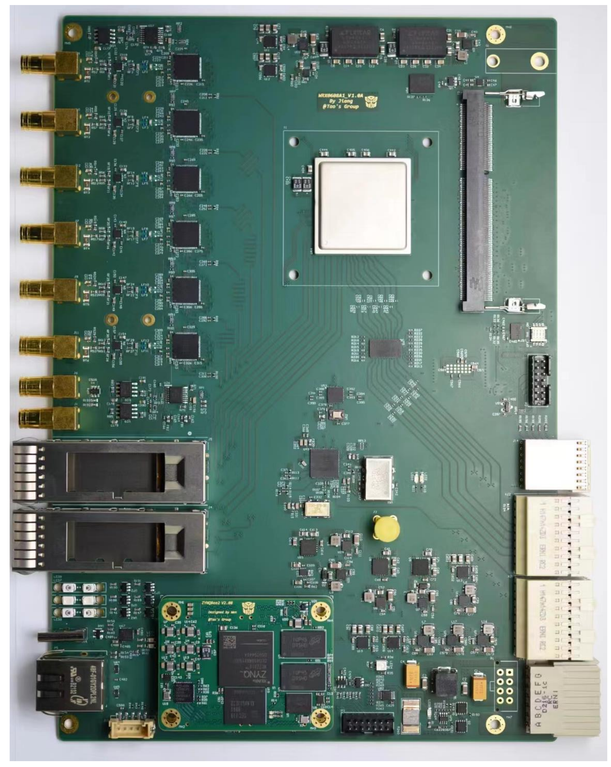

Fig. The PCB photo of waveform digitizer WRX0608A1.

Experiments

The parallel 500MHz 13-bit, DDR data from the ADC is output 125MHz, 104-bit data through SelectIO IP core and stored in the ring buffer. When the external trigger signal arrives, the data will be packaged, including the packet header, channel number, event number, time stamp, data and packet end.

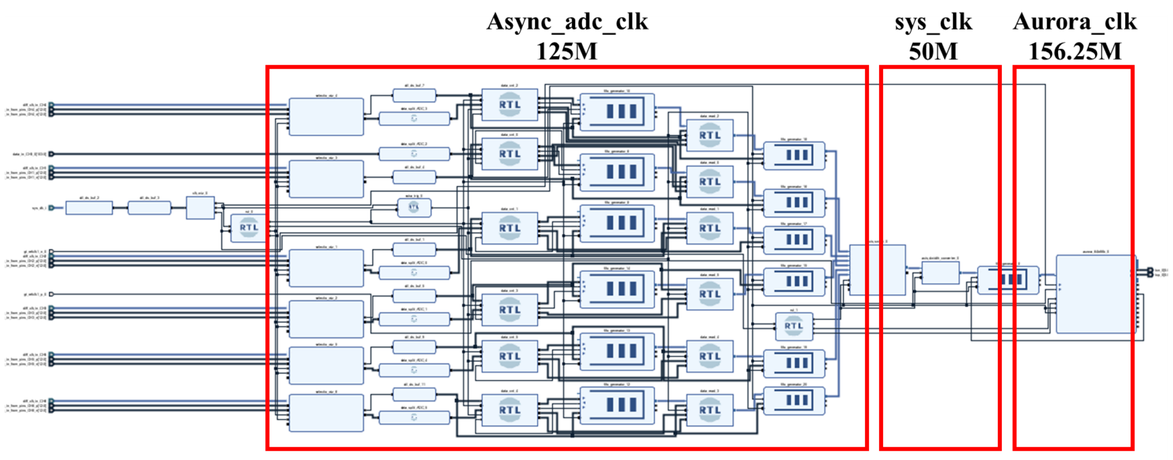

Fig. FPGA implementation of single board 6 channels data acquisition.

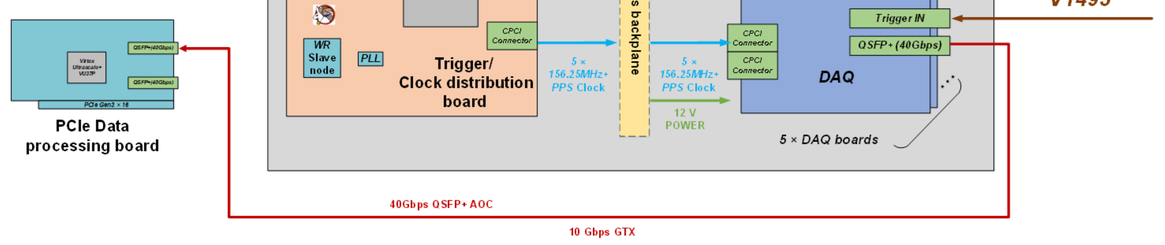

Fig. Architecture of a readout electronics system with 30 sampling channels externally triggered.

The triggered data is transferred to the PCIe card, such as the Xilinx Alevo U50, through the QSFP+ port on the front panel, and is eventually stored on the server. Trigger and clock distribution boards distribute synchronous clocks to all waveform digitizer.

ADC's effective number of bits (ENOB), QSFP+ interface eye diagram scan and 6-channel data acquisition were tested in detail.

Result

The ADC's ENOB was actually tested using SMA100B from R&S®. The results show that under 1MHz sine wave, ENOB>10bit, which means that it can meet the needs of neutrino experiments.

The QSFP+ interfaces have been tested in self-loopback mode used 40G loopback module. The link speed is set to 10.3125 Gbps and the encoding method is PRBS 7-bit. The open area and the open UI of all eight lanes better than 3900 and 50%, respectively. When the BER is 6.393e-15, there is no bit error.

MGTX_B118 Channel	Open Area	Open UI
Channel 0	4216	53.85%
Channel 1	3904	55.38%
Channel 2	3978	52.31%
Channel 3	4543	50.77%

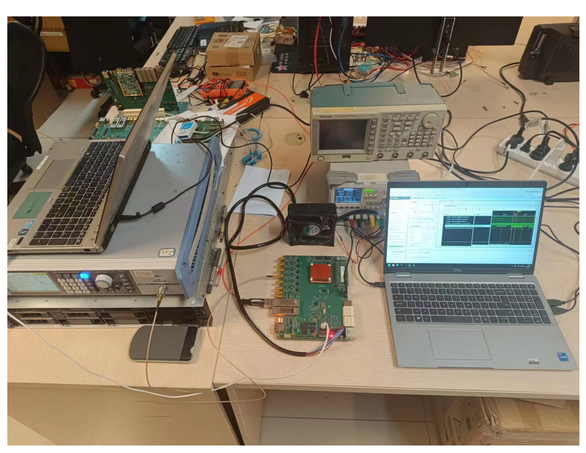

Fig. Experimental setup of ADC ENOB test.

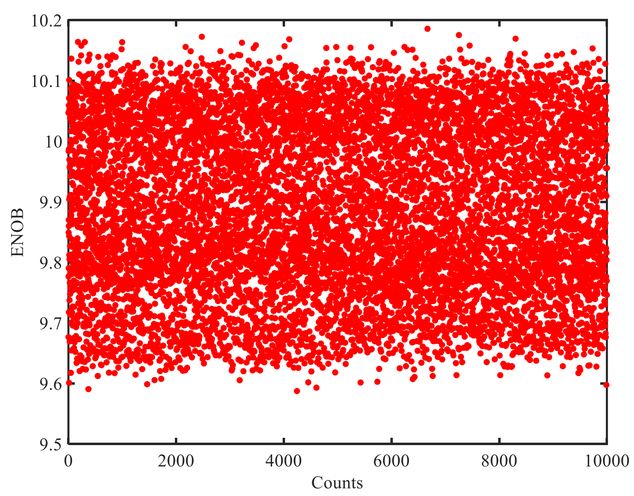

Fig. ADC ENOB test results.

At the same time, we also carried out the system construction and data transmission test of two boards with a total of 16 channels. The data of the two "WRX0608A1" is independently sent through the QSFP+ interface on the front panel, converted into a 10Gbps link through a four-to-one AOC cable, and then the two 10Gbps links are combined into a 40Gbps link through an adapter and sent to the PCIe board. The test of self-increment data collected shows that there is no error code in the data transmission process.

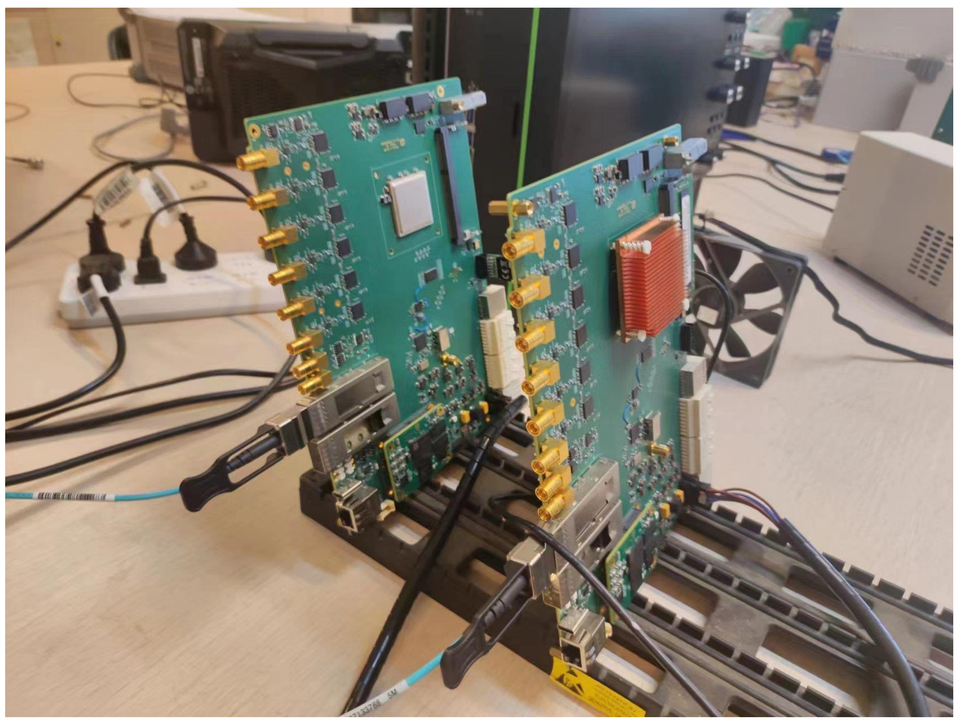

Fig. Experimental setup of 12-channels data acquisition.

Lin Jiang, Department of Engineering Physics, Tsinghua University. Email: l-jiang18@mails.tsinghua.edu.cn