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Preliminary Design of Waveform Digitizer for Jinping Neutrino Experiment at CJPL

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This paper reports the preliminary design of waveform digitizer “WRX0608A1” for Jinping neutrino experiment at CJPL. Single block digitizer can support 6-channels 1GSPS, 13-bit sampling. The WRX0608A1 is a 12-layer PCB, hosting 6 ADCs, one FPGA (Xilinx Kintex 7 XC7K325T), one PLL (TI LMK04803), one DDR3 SODIMM (Micron MT8KTF51264HZ-1G9P1), one re-driver (TI DS125BR820), two QSFP interfaces and other parts. The ADC’s effective number of bits (ENOB) was actually tested using SMA100B from R&S®, band-pass filter Q70T-10M-1M-50-720A and low-pass filter J97T-14M-50-69A from TTE. The results show that under 10MHz sine wave, ENOB>10bit, which means that it can meet the needs of neutrino experiments. The open area and the open UI of QSFP all eight lanes’ eye diagram are better than 3900 and 50%, respectively. When the BER is $6.393e-15$, there is no bit error. Similarly, we used two WRX0608A1, one trigger board and one eight-slot backplane for backplane high-speed signal integrity testing. Under the lane speed of 10.3125 Gbps, there is no bit error in the test. The joint debugging experiment of the waveform digitizer and the detector and the research on the trigger algorithm are in progress.

Submitted on behalf of a Collaboration?

No

Primary authors: Mr YANG, Haoyan (Tsinghua University); Prof. LI, Jianmin (Tsinghua University); Mr WEN, Jingjun (Tsinghua University); Mr WEI, Liangjun (Tsinghua University); Mr JIANG, Lin (Tsinghua University); Mr 潘, 秋彤 (清华大学); Prof. XUE, Tao (Tsinghua University); Mr GUO, Xiaowei (Tsinghua University); Prof. LIU, Yinong (Tsinghua University)

Presenter: Mr JIANG, Lin (Tsinghua University)

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