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Development of cryogenic CMOS ASICs for HPGe detectors for dark matter and neutrino detection experiments

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Germanium detectors have been widely used for both dark matter and neutrino-less double beta decay experiments due to its high energy resolution, low threshold and working at medium-low temperature. Hence large scale experiments up to ~ 1t detectors have been proposed, including LEGEND and CDEX. In order to achieve best performance, readout electronics, especially the front-end electronics should be mounted as close to the detector as possible. Custom designed ASICs (Application Specific Integrated Circuit) are demanded to satisfy the stringent requirement for low noise, low mass, highly integration and operation at cryogenic temperature. This paper will introduce the progress on the development of ASICs for HPGe detectors, including a low noise and wide dynamic range preamplifier and SCA (switched capacitor array) based waveform sampling chip with on-chip digitizer. A noise level of 108 eV FWHM has been measured with a 0.5 kg HPGe detector. Detailed chip design and test results will be present.

Submitted on behalf of a Collaboration?

No

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