ATLAS Muon Drift Tube Front-end Electronics Upgrade for HL-LHC Runs

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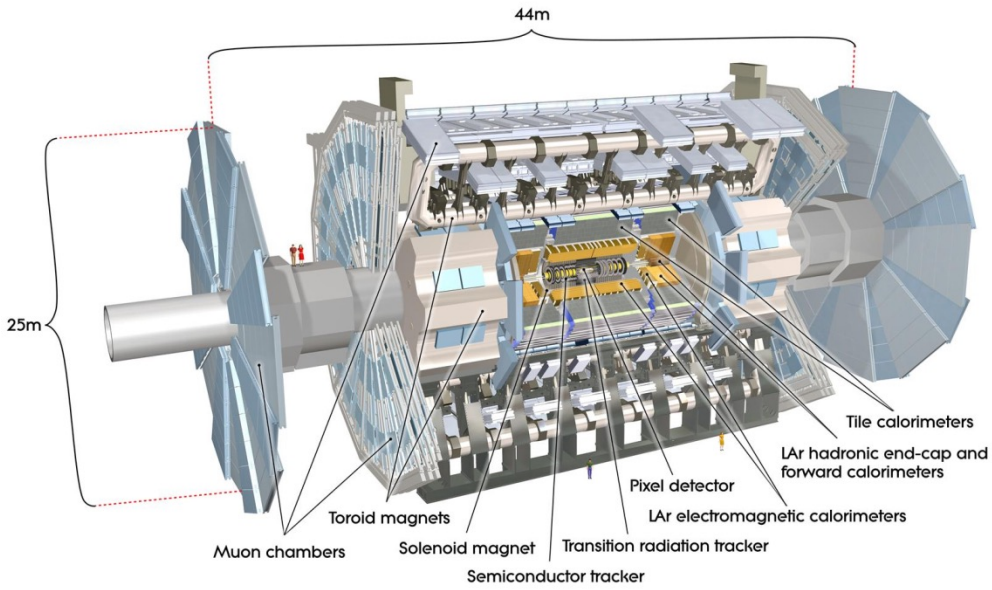
On behalf of the ATLAS Muon System

March 27th, 2023

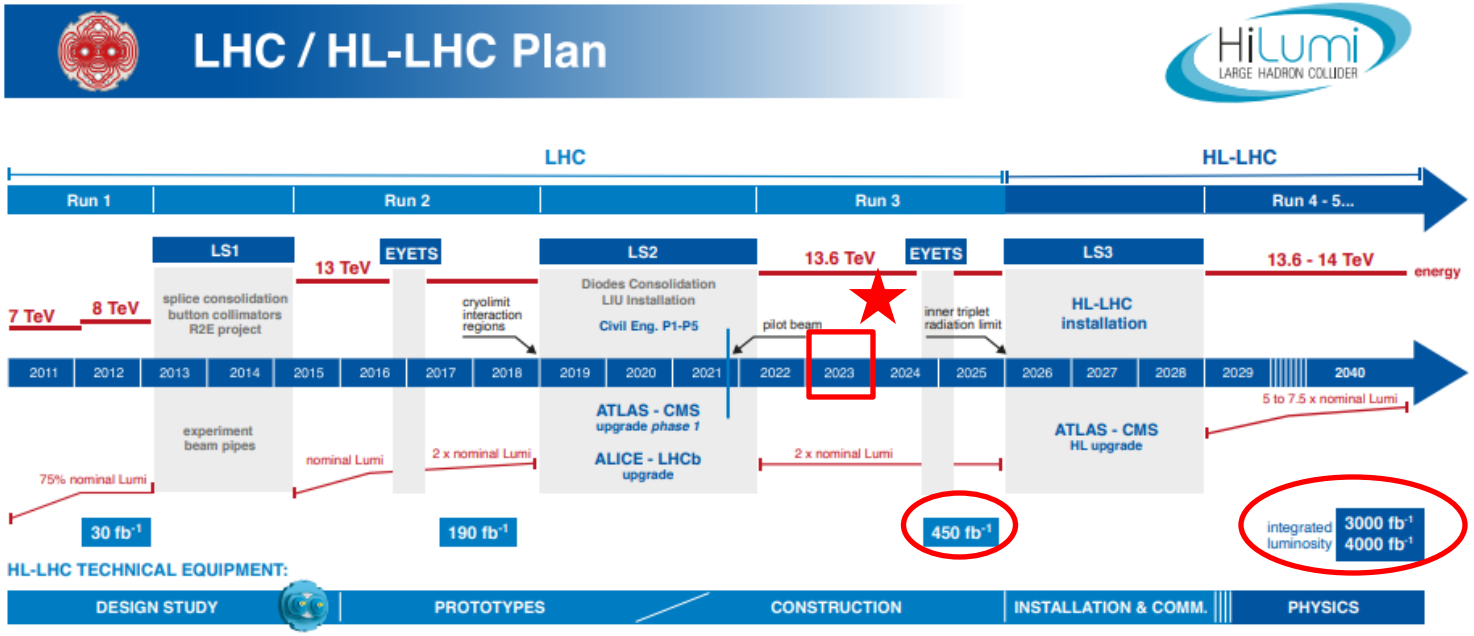
Outline

- Introduction
- Frontend Electronic System Upgrade
  - ASD
  - TDC
  - Mezzanine Card
  - CSM
- Integration Test Plan
- Summary



Introduction

❑ The roadmap to High-Luminosity LHC



- HL-LHC: increase of Luminosity to $5{\sim}7 * 10^{34} cm^{-2} s^{-1}$
  - Higher pile-up
  - Higher particle rates
  - Higher radiation level

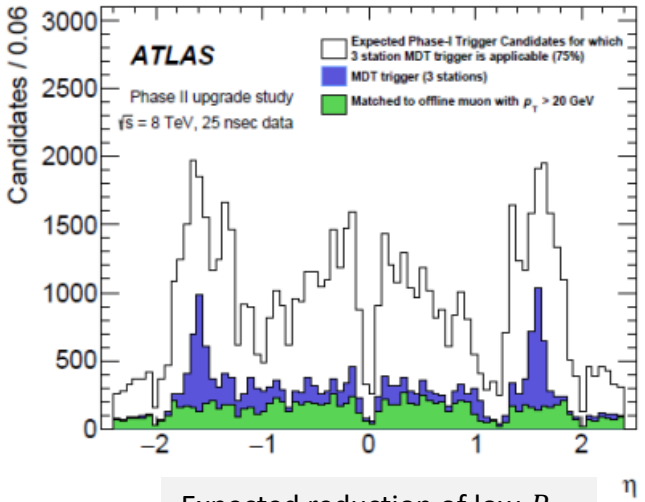
  } Major detector/electronics upgrade

- Muon Spectrometer Upgrade: 2 Phases during long shut down 2 and 3

Introduction

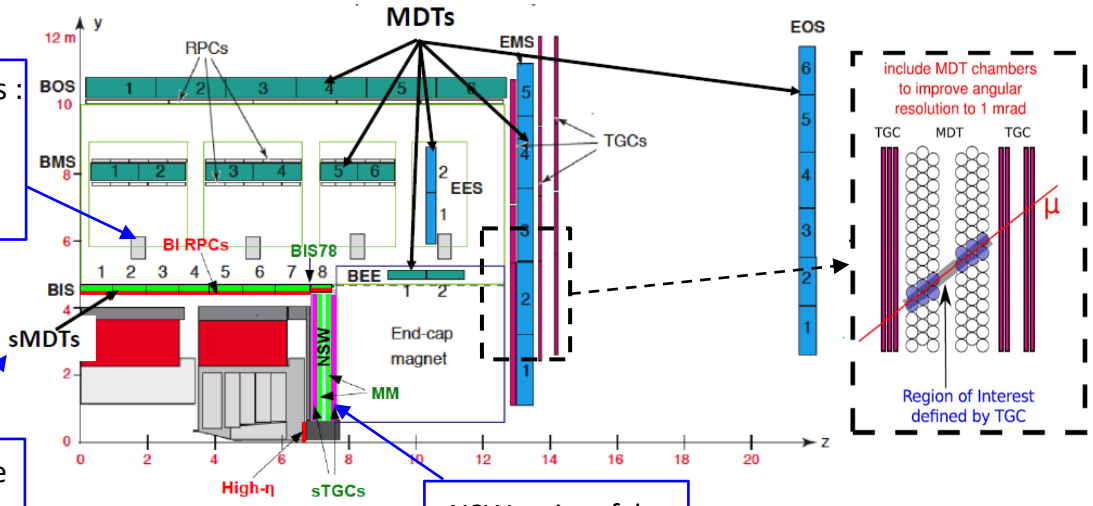
❑ ATLAS Muon Spectrometer @ HL-LHC

- Improve Muon transverse momentum (P_T) resolution
  - RPC and sMDT chambers will replace current MDT chambers (inner barrel) to allow for a 3-station RPC trigger
  - P_T selectivity of tracks for the trigger will be improved by using better position resolution @ L0 triggering
- Cope with High-Lumi Requirements
  - MDT (Monitor Drift Tubes) readout electronics system must be upgraded
  - 1150 chambers with 354k tubes covering an area of 5500 m^2



Expected reduction of low-P_T fake triggers using the MDT

New thin-gap RPCs : close acceptance gaps of the barrel muon trigger



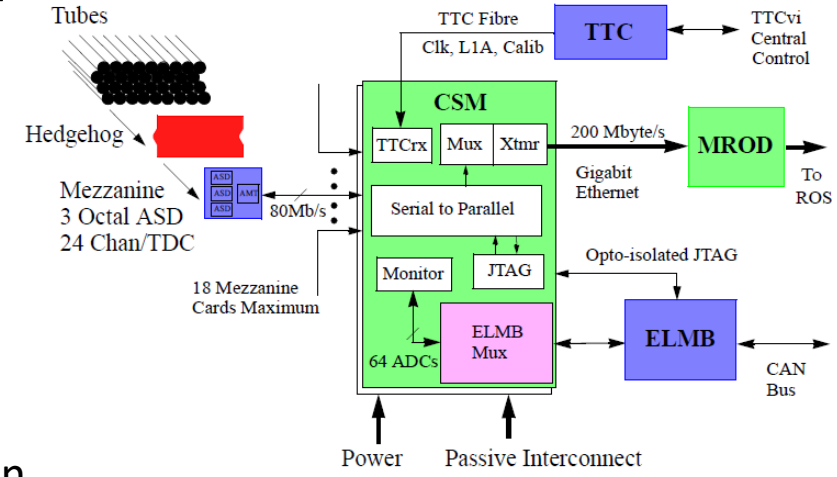
sMDTs: free space for new PRCs

NSW: reject fake muon triggers

MDT Electronics System

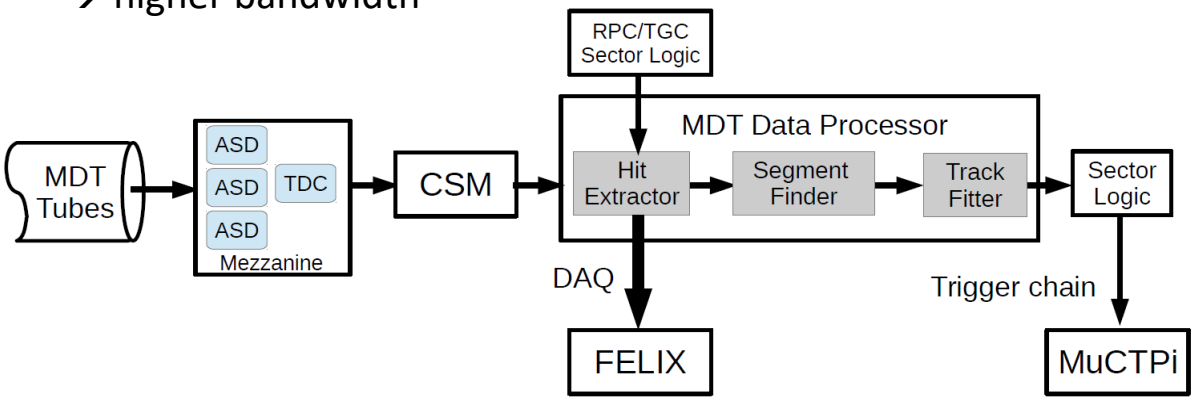
❑ MDT Electroincs @ Current System

- MDT & Trigg. Chambers are read out independently
  - MDT readout only on L1 trigger → lower bandwidth
  - Trigger mode used at the Front-end



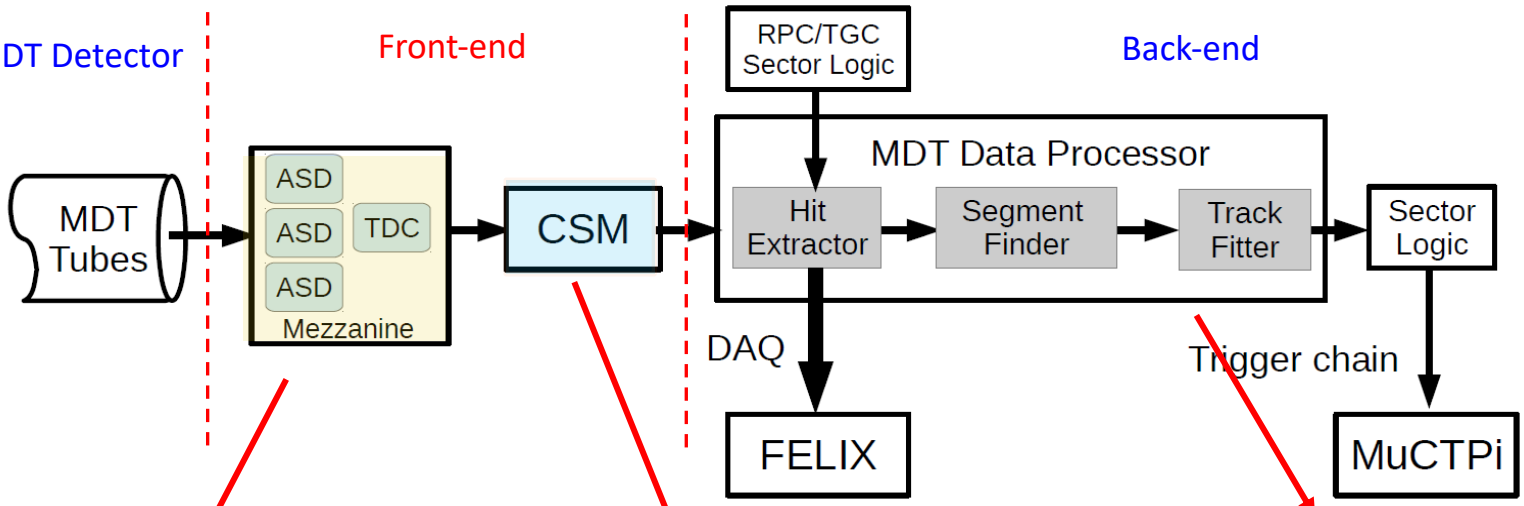
❑ MDT Electroincs @ HL-LHC

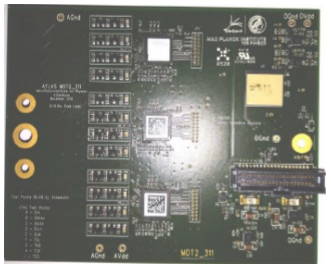
- MDT data is used to "sharpen" trigger decision
  - Find accurate pT using ROI seed from trigger chambers and confirm/reject trigger hypothesis
  - Triggerless at FE and track fitting in the counting room → higher bandwidth

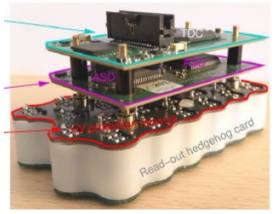


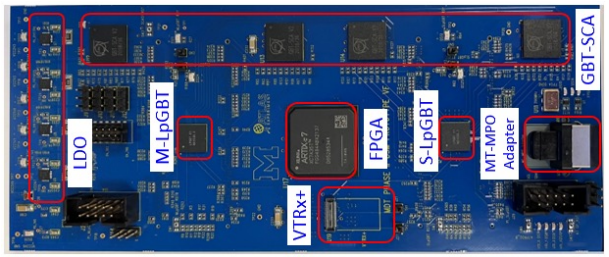
General Concept:
Move decision making to the counting room

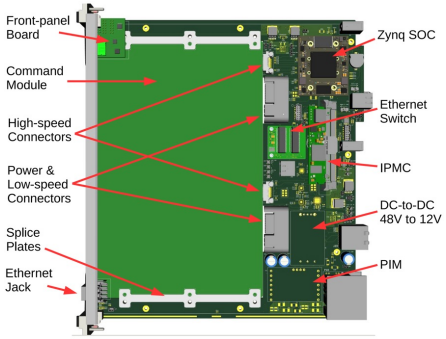
MDT Electronics System @ HL-LHC











New ASD & TDC ; New Mezz

- New triggerless operation
- Support higher readout bandwidth
- ~80k ASDs & ~22k TDCs will be produced
- New Stacked Mezz for sMDT

New CSM: GBT chipset based

- Flexible handle both old/new Mezz.
- Fix latency & ~20Gbps bandwidth
- Fan-out configuration information for Mezz
- Collect monitior information for MDT FE elx
- Will deliver 1350 boards

MDT Data Processor

- Provide MDT trigger candidate to the global L0 trigger level
- Precision data readout
- Will deliver 64 ATCA cards

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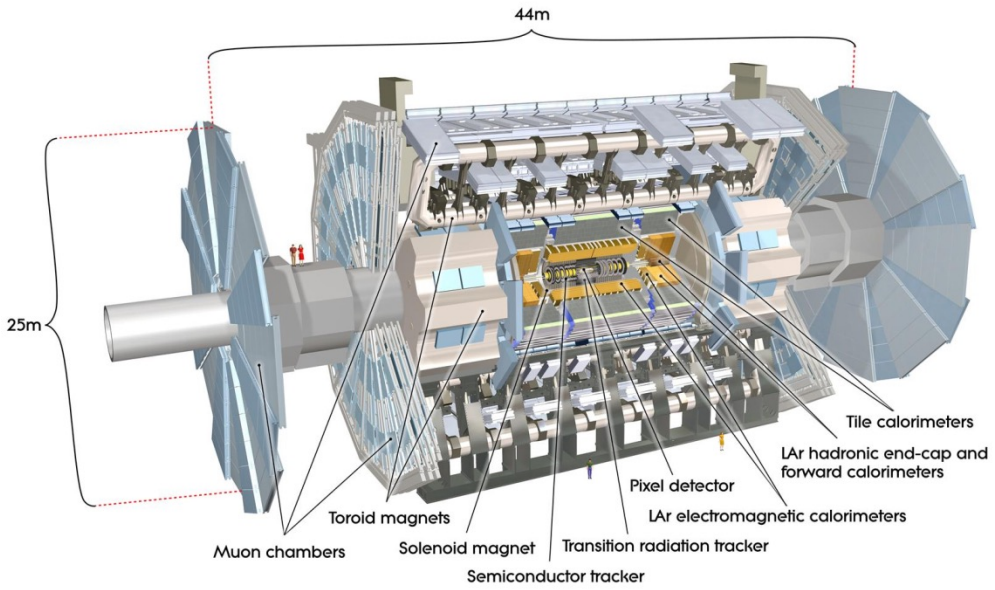
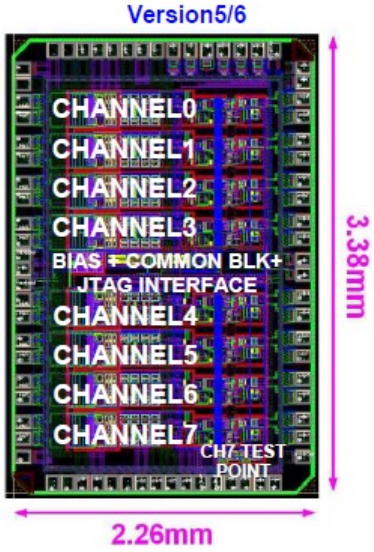


Amplifier-Shaper-Discriminator ASIC

❑ ASD Design

- 8-Chs ASD: GF 130nm CMOS process (7.6 mm^2)
- 4 key parts
  - Pre-amplifier: charge-sensitive
  - Shaper: differential amplification (DA1-DA3)
  - Wilkinson ADC & Discriminator
  - LVDS Output Driver (reduced swing)



ASD Layout

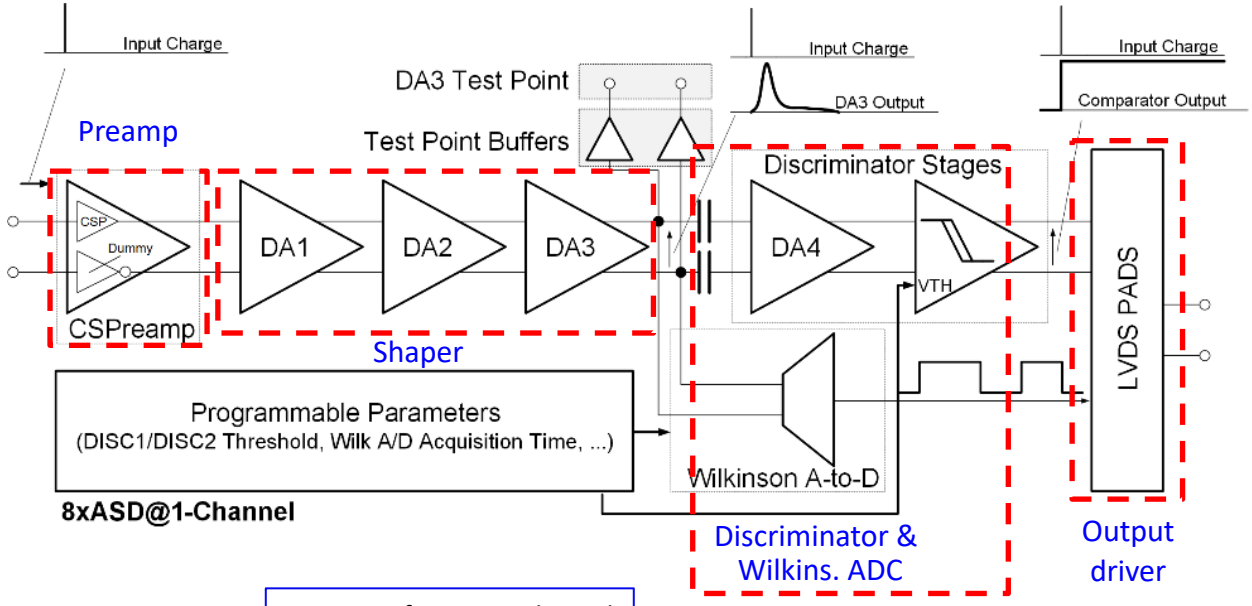
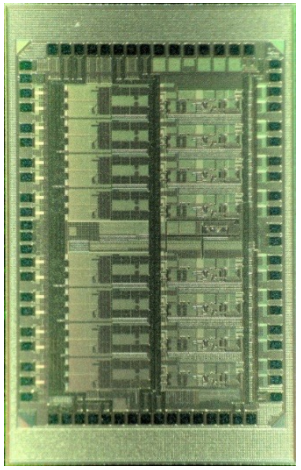


Diagram of one ASD Channel



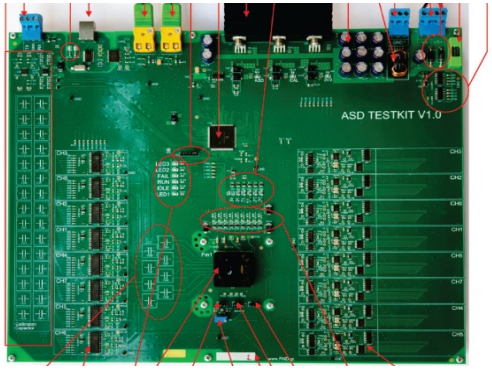
microscope photo of ASD ASIC

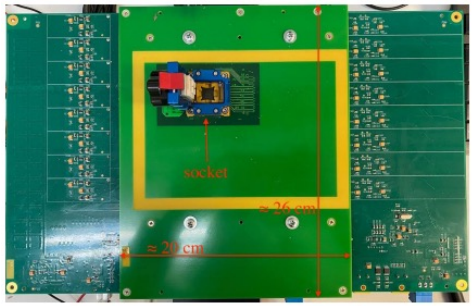
Amplifier-Shaper-Discriminator ASIC

❑ ASD Project Status

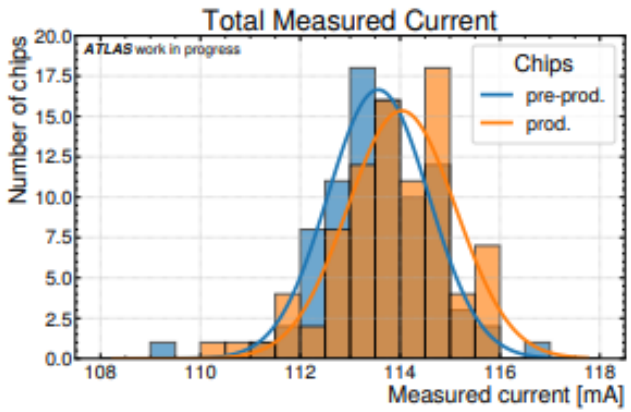
- Preproduciton of 7.5k ASD chip was done in 2019, yeild rate: ~92.4%
- Production of ASD chip was completed @ end of 2020
- 83k production ASD chips produced and packed in 2021
- Test 1175 production ASD chips for verification of new tester, yield rate: ~86%
- Chip production test: starts in spring 2023

*Ref: https://cds.cern.ch/record/2852416/files/ATL-COM-MUON-2023-008.pdf

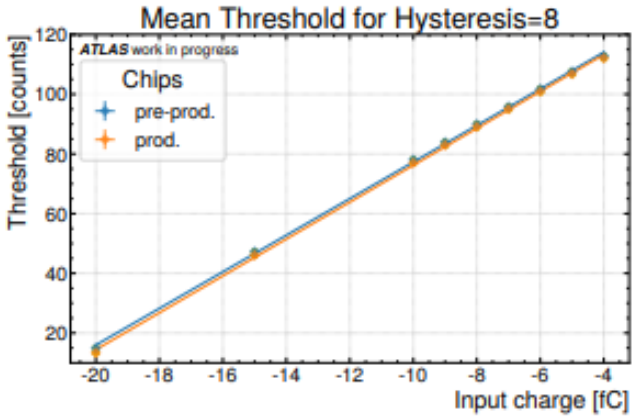




Preproduction and Production ASD chip testers



(a) Basic Health Measurement



(b) Threshold Measurement

Comparison between pre-production chips and the first batch of production chips

Time-Digital-Converter ASIC

❑ TDC Design

- 24 CHs input, 2 CHs outputs (320Mbps)
- 4 key parts
  - ePLL (extended Phase-locked loop)
  - Timing circuit: fine + coarse time (0.78ns bin)
  - TDC logic
    - Trigger-less + Trigger mode
    - New output protocol
    - High speed interface
  - Interface: serial output, configuration, clocks…
- Triple Module Redundancy: all configuration registers, clock trees…

No. of channels	24
Least time count	0.78 ns
Dynamic range	17 bits (102.4 μs)
Integral non-linearity	±40 ps
Differential non-linearity	±40 ps
Double hit resolution	<10 ns
Input clock frequency	40 MHz
Max. recommended hit rate	400 kHz per channel
Edge/pair time measurements	Configurable
Output data rate	Configurable: 80 Mbps one line, 160/320 Mbps two lines
Triggerless/trigger modes	Configurable
Triggerless: Latency	<500 ns at 400 kHz per tube
Trigger: Buffer sizes	Hit buffer: 16/channel, channel FIFO: 4/channel, Readout FIFO: 16
Channel enable/disable	Yes
Input/Output signal	SLVS
Radiation tolerance	>20 kRad
Power consumption	<360 mW
Fabrication process	TSMC 130 nm CMOS process

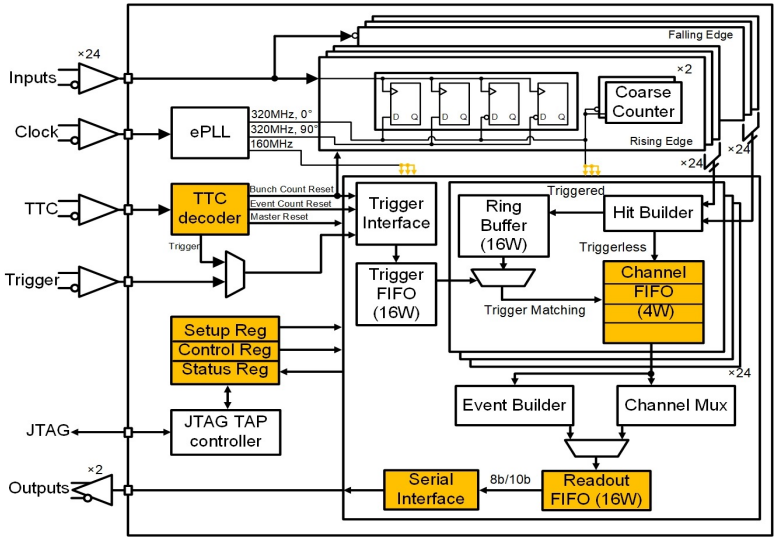
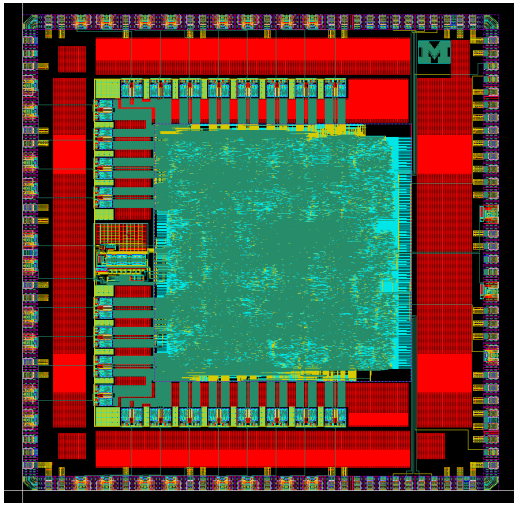


Diagram of TDC V2 with TMR implemented (yellow blocks)



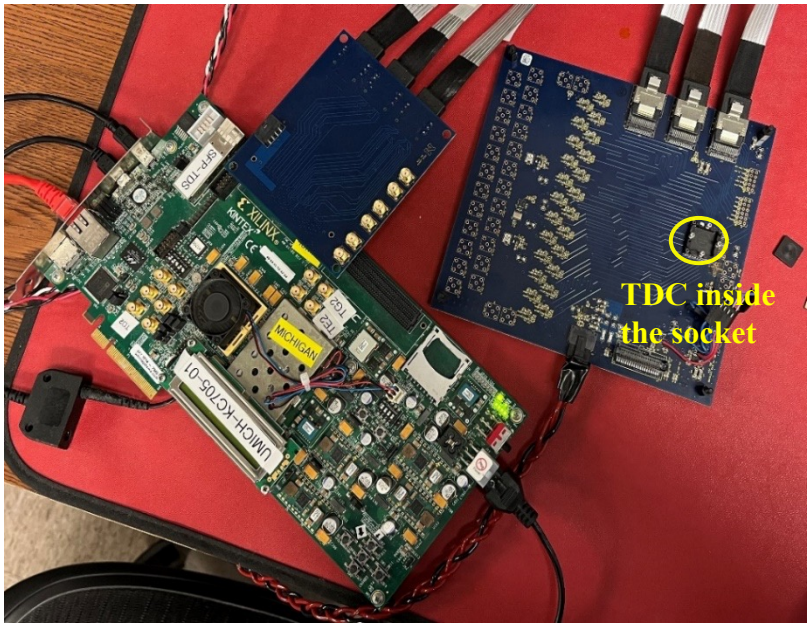
TDC ASIC Layout

Time-Digital-Converter ASIC

❑ TDC Project Status

- 16 wafers received in July, 2022
- In total 3,726 packaged TDC chips (2 wafers) received on the first week of January 2023
- 100 chips have been tested and no design problems found.
- 15 chips were sent to MPI to be assembled on a few mezz. cards for joint tests.
- One automatic test platform is ready @ UM

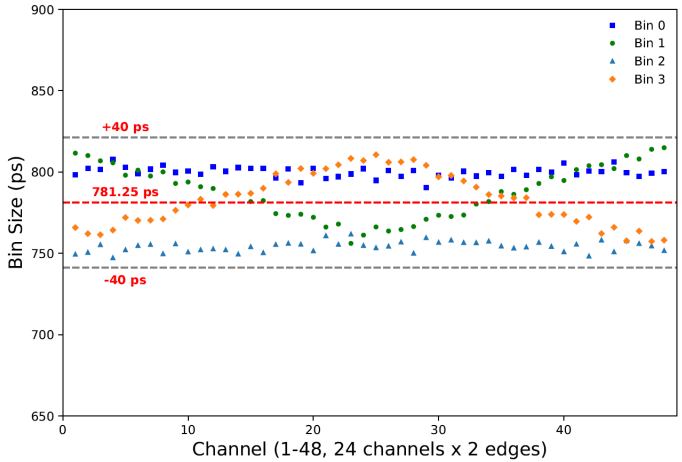
Packaged chips in the tray



* Two or three more stations will be produced for parallel testing

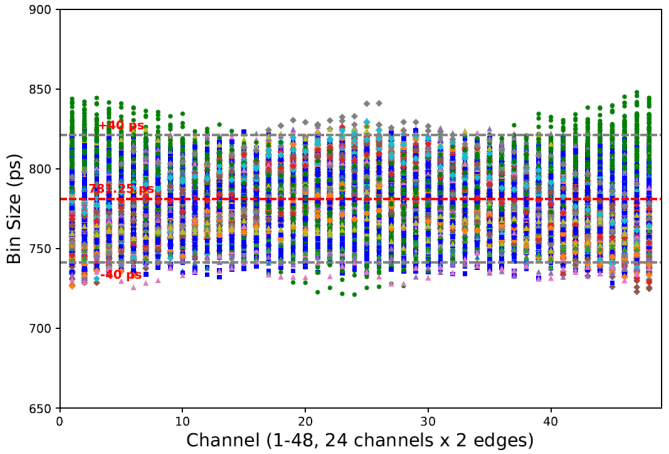
Time-Digital-Converter ASIC

❑ Test results

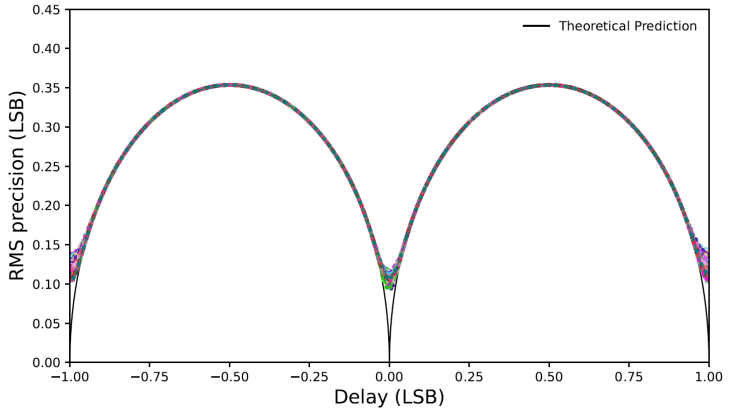


Fine-time bin size of one TDC (48 slices)

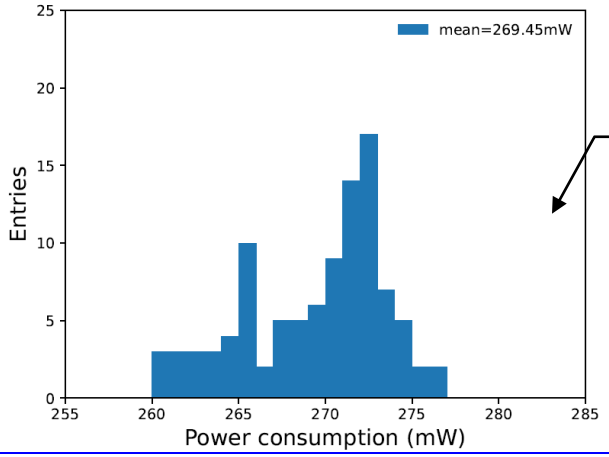
Bin size for most channels falls within ±50 ps
(4/100 have bin size variation larger than 50 ps)



Fine-time bin size of 100 TDCs



Timing resolution (RMS) of 4 TDCs (192 slices)



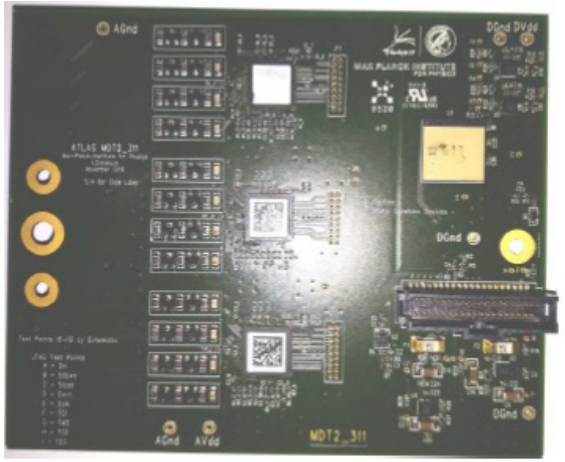
TDC @ 320 Mbps,
triggerless mode

Average power consumption 269 mW @ 1.20 V for 100 chips

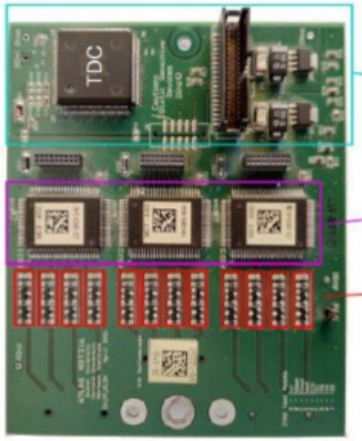
Mezzanine Card

❑ Status

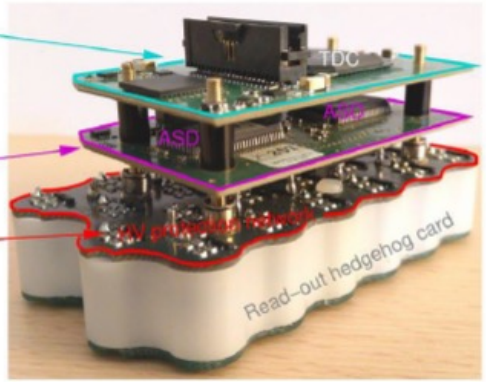
- Flat card (MDT316, MDT436, MDT446)
  - MDT2_316 board with 3 LDO has been tested good with the mezzanine card tester of the University of Würzburg (MDT2_316 board with 2 LDOs is on the way)
  - MDT2_436 and MDT2_446 boards (for 4-layer chambers) are being produced with halogen-free material (2 LDOs/card)
  - Final Design Review in Apr. 2023
- Stacked card (for sMDT)
  - Final Design has been approved in Nov. 2022
  - 3 LDOs/card will be used (LP3964EMP-ADJ/NOPB)



Prototype MDT Mezzanine Card



Legacy MDT Mezzanine

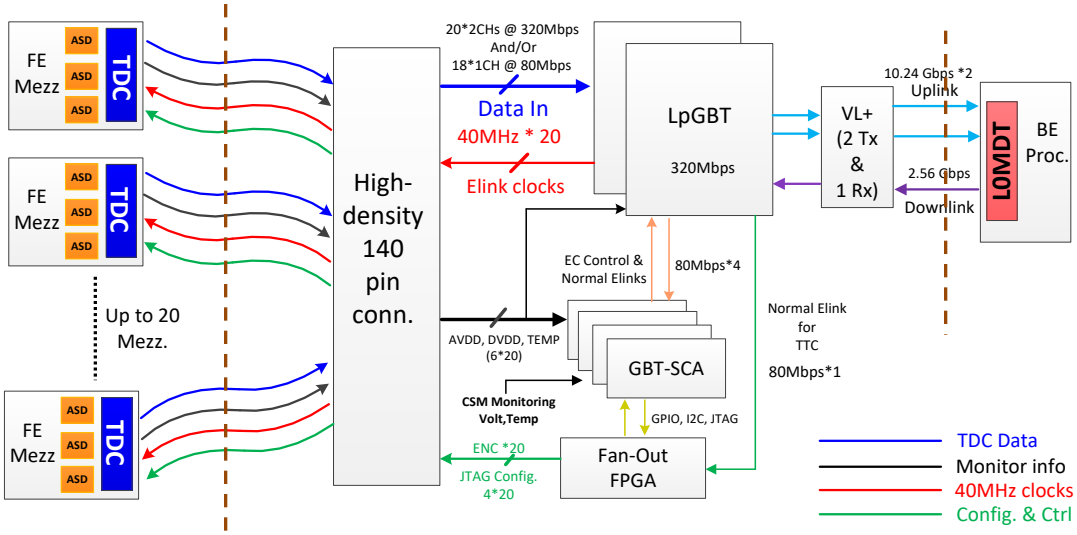


sMDT stacked Mezzanine

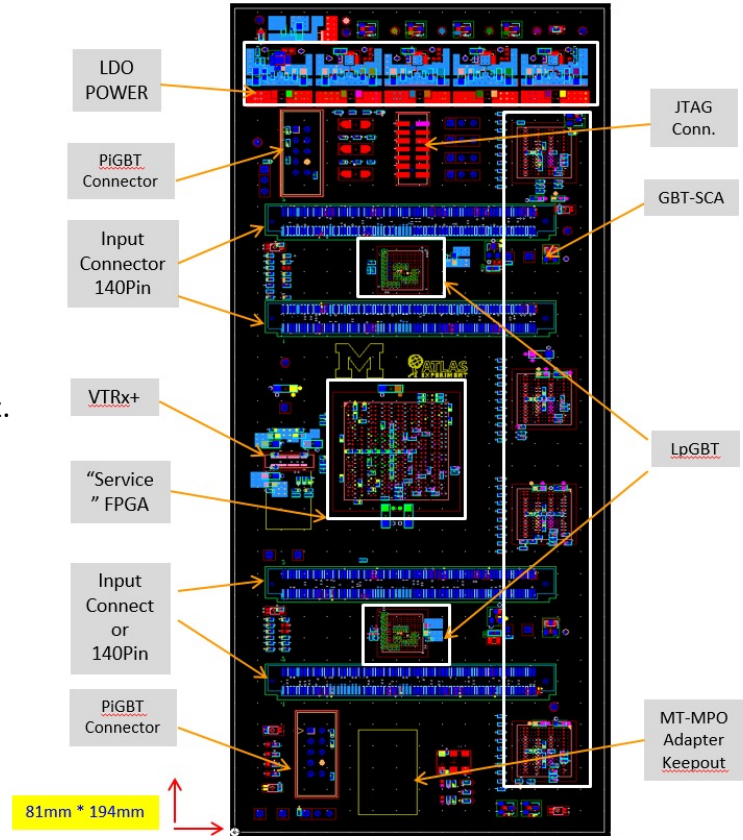
Chamber Service Module

❑ CSM Design

- Handle upto 20 Mezzanines:
  - Input (40 CHs * 320Mbps)
  - Output (uplink fiber 2*10.24Gbps, downlink fiber 1* 2.56Gbps)
- 4 key parts
  - LpGBT *2 (master-slave mode)
  - GBT-SCA*4 : monitoring & configuration
  - Fan-out FPGA: receive configuration info and broadcast to all 20 Mezz.
  - VTRx+: optical module



LpGBT-CSM Functionality Block Diagram

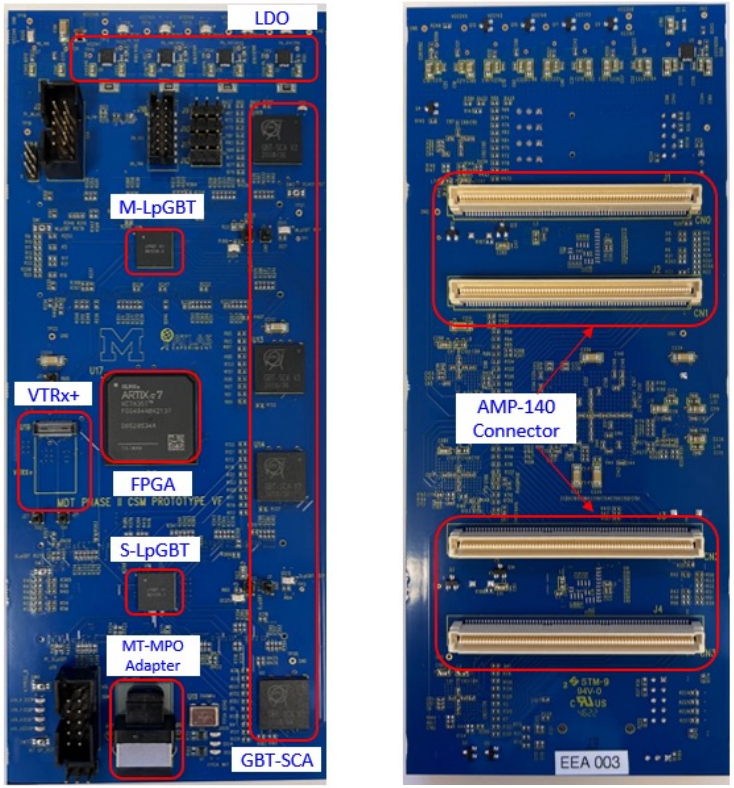


Layout of CSM prototype v2

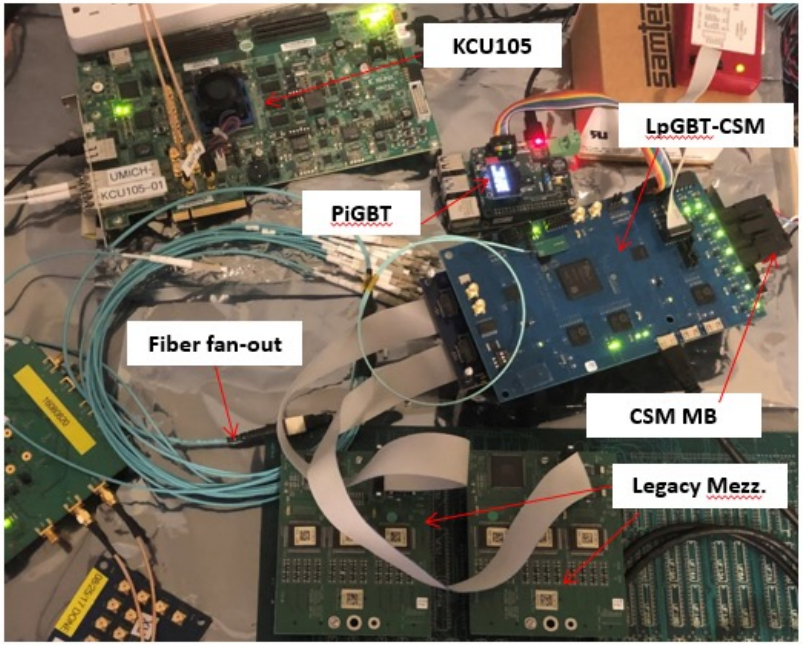
Chamber Service Module

❑ CSM Project Status

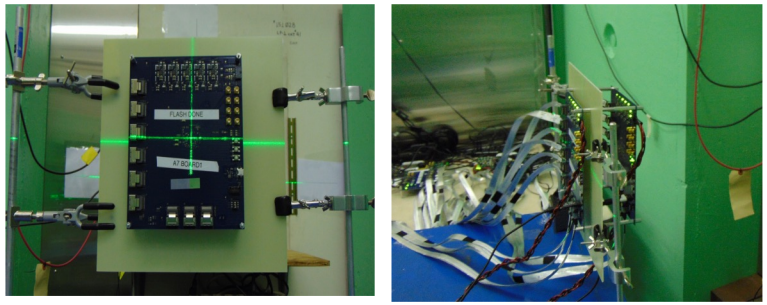
- Final CSM Prototype: pass standalone & integration tests
- Radiation tests of CSM FPGA, LDO have been successfully done @ LANSCE, BNL, PSI...
- Final Design review: May. 2023



Photos of CSM final prototype (Top & Bottom)



Test setup of legacy Mezz. and CSM prototype



CSM FPGA rad-test boards @LANSCE

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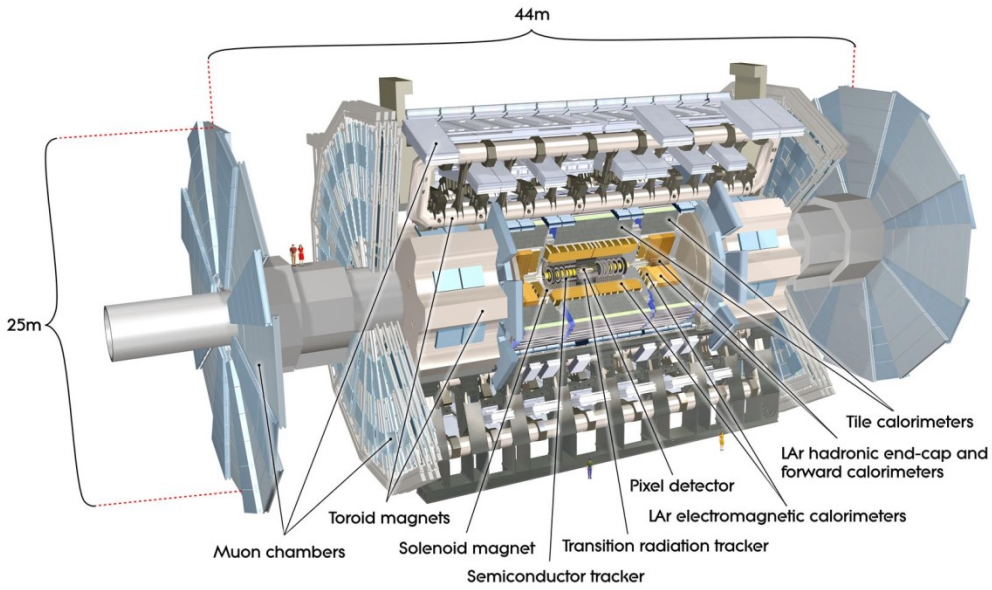
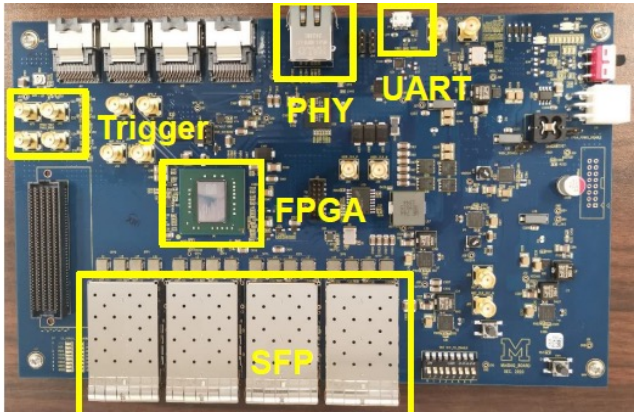


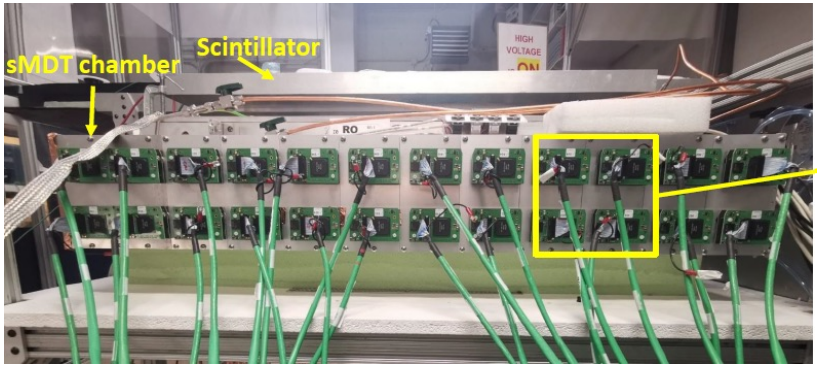
Integration Test Plan

❑ Integration Tests of the FE Electronics

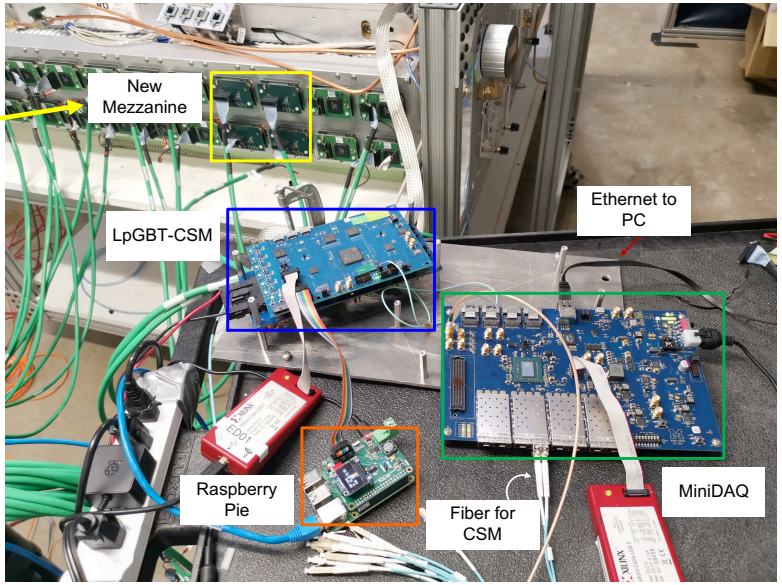
- MiniDAQ board (a light version of L0MDT)
  - L0MDT (MDT data processor) is not ready yet
  - Integration test of all new FE elx is very important
  - ✓ MiniDAQ Board is designed for sMDT/MDT chamber + FE elx integration and commissioning



Photos of MiniDAQ Board



New sMDT chamber (module 0) @ Umich

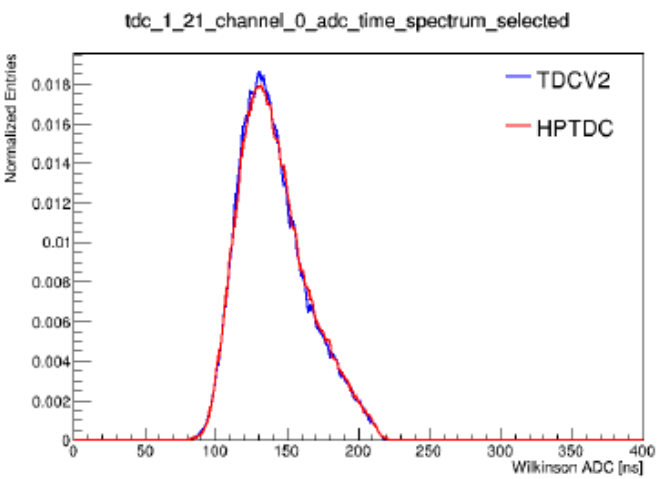


Integration tests of new MDT FE elx @ Umich

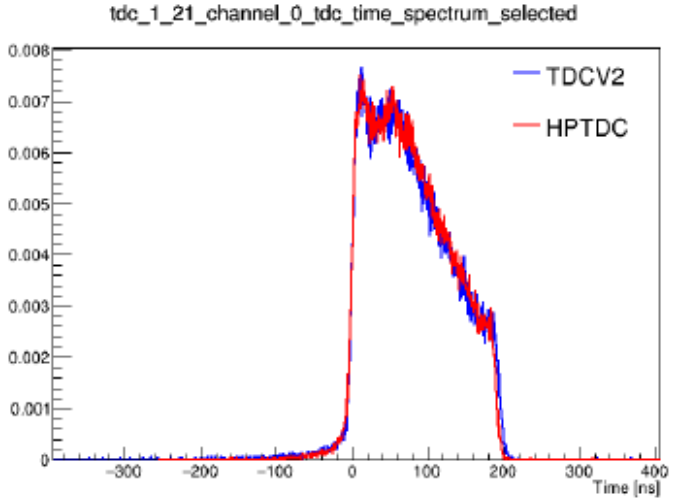
Integration Test Plan

❑ Integration Tests of the FE Electronics

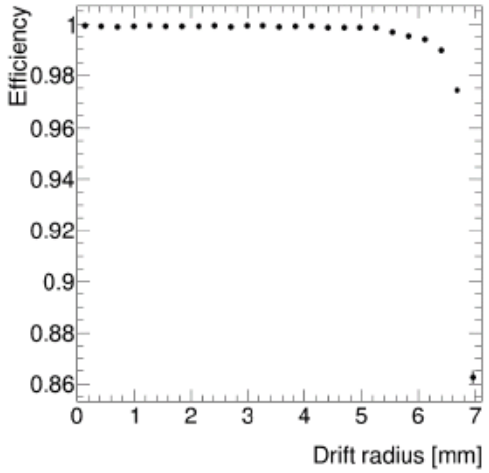
- Cosmic ray data in trigger-less mode @ MDT/sMDT detector
- Trigger matching performed inside the miniDAQ FPGA
- TDC/ADC spectrum and efficiency compared between new elx (trigger-less mode) and legacy elx (triggered mode)



Single tube ADC spectrum comparison



Single tube TDC spectrum comparison



Average tube efficiency

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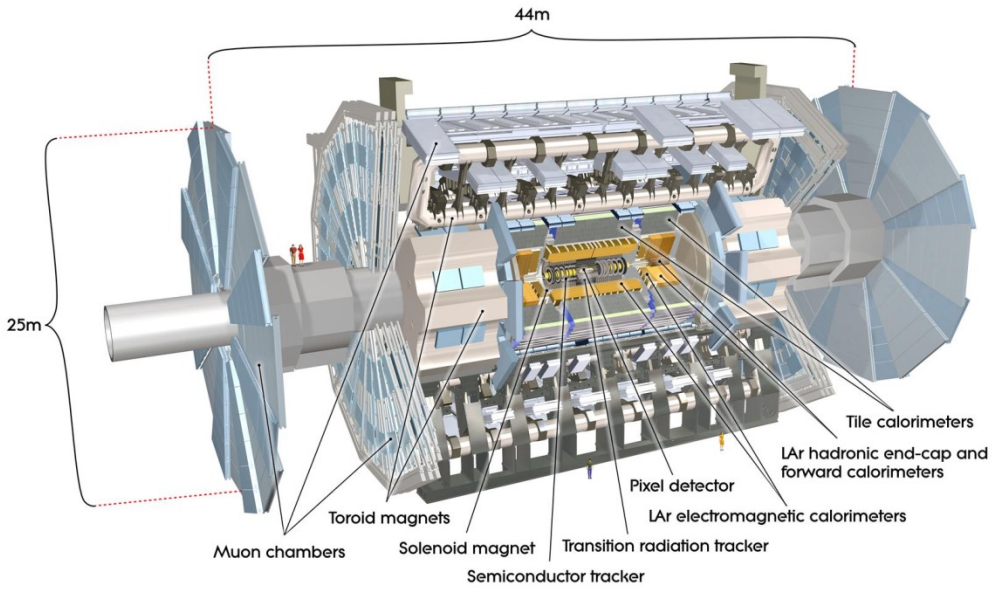

Summary

- To cope with high rates & improve P_T momentum resolution, upgrade all ATLAS MDT electronics system is required
- MDT FE upgrade projects have made lots of progress and passed major reviews
  - ASD: Production has been done & Testing is on-going
  - TDC: Production is on-going & ~4k TDC chips received in Jan. 2023
  - Mezzanine card & CSM : FDR in Apr. & May (design under approval)
- Ongoing development on the frontend electronics integration
  - Intergration: sMDT/MDT chambers → Mezz. card → CSM → L0MDT emulator in MiniDAQ
- General Schedules
  - ASD production test @ Q1.2023
  - TDC production on-going @ Q1.2023
  - Mezz. card production start @ Q1. 2024
  - CSM production start @ Q1. 2024

We are on track!

Thanks!