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Parallel session B7 - Systems, Installation and Commissioning 7 / 0

Low Power Front End for the Optical Module of a Neutrino Underwater Telescope

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A proposal for a new system to capture signals in the Optical Module (OM) of an Underwater Neutrino Telescope is described. It concentrates on the problem of power consumption in relation to precision. In particular, a solution for the interface between the photomultiplier (PMT) and the front-end electronics is presented.
We have used the most recent data coming from simulations of high energy neutrino events produced in a submarine detector in order to define the specifications of the front-end electronics that optimise the detector performance. As a result a new architecture has been defined for the chip that performs the sampling.

Summary:

An Underwater Neutrino Telescope uses large area PMTs inside OMs to detect the Cherenkov light from the muons generated by neutrinos in the seawater. The PMTs are put in a 17” glass sphere capable to stand at more than 350 Atm external pressures. The signals at the output of PMTs must be suitably coded and sent on-shore. The OM contains the PMT and its power supply board, the front-end electronics, the data pack and transfer electronics, the slow control interface and a set of environmental sensors.
The work described in this paper is aimed at the development of the low-power front-end for the Optical Modules (OM) of the NEMO submarine neutrino detector [2,3,4,7]. A mini-tower equipped with 16 OMs (NEMOPhase1 MiniTower) has been successfully deployed in December 2006 in front of the Catania harbour as a first prototype. It uses the front-end electronics described in [1]. The technological solutions adopted for the NEMO MiniTower provide results well in agreement with expectations. In the meantime, we have proceeded in our development of a solution which can fulfil all requirements of a km3-scale detector, in particular for what concerns power consumption, PMTs aging and signal dynamics.
Our work is based on the design of an Application Specific Integrated Circuit (ASIC) for the development of the Trigger, the PMT signal classification and fast sampling of the PMT signal, which is performed according to the signal classification. Moreover, commercial ADCs and a Field Programmable Gate Array (FPGA), provide digital encoding, data packing and then data transfer towards the shore station for acquisition.
A board containing the PMT interface electronics, the ASIC, the ADC and the FPGA constitutes the OM front-end. By means of the FPGA, this board receives the slow control and transmits the measurements of environmental parameters such as temperature, humidity etc., together with the data.

The final version of the chip, named LIRA05, has been tested and the single blocks, constituting its architecture, that is, the analog memory, the trigger and single photon classifier and the clock frequency multiplier, have been characterised. The board to test the whole front-end together with the PMT is being prepared.
The design of the front-end board and of the chip, in particular, are based on parameters and specifications that in some cases are not yet definitive, for the performance of the whole detector.
We have used the most recent data coming from simulations of high energy neutrino events produced in a submarine detector in order to define the specifications of the front-end electronics that optimise the detector performance. These simulations describe the signals collected by each PMT in the apparatus in response to particle events, taking into account the optical background due to 40K, the optical properties of the sea water, the orientation and position of the PMTs.
As a result a new architecture has been defined for the chip that performs the sampling.
This new device, called Smart Auto-triggering Sampler (SAS), will consist of functional blocks very similar to those already designed and successfully tested.

Poster session / 1

Distribution of the Timing, Trigger and Control Signals in the Endcap Cathode Strip Chamber System at CMS

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This paper presents the implementation of the Timing, Trigger and Control (TTC) signal distribution tree in the Cathode Strip Chamber (CSC) sub-detector of the CMS Experiment at CERN. The key electronic component, the Clock and Control Board (CCB) is described in detail, as well as the transmission of TTC signals from the top of the CSC system down to the front-end boards.

Summary:

The Cathode Strip Chamber (CSC) sub-detector currently being commissioned at CERN comprises 468 six-layer multi-wire proportional chambers arranged in four stations in the Endcap regions of the CMS. The goal of the CSC system is to provide muon identification, triggering and momentum measurement. The CSC electronic system consists of: (1) on-chamber mounted anode and cathode front-end boards; (2) Trigger and DAQ boards in sixty 9U crates on the periphery of the return yoke of the CMS; and (3) one Track Finder (TF) and four Front-End Driver 9U crates located in the underground counting room. In total, the timing, trigger and command information must be distributed to more than 3500 electronic boards in the entire CSC system.

The top component of the TTC distribution tree within the CSC system is the Clock and Control Board (CCB). It resides in the middle of the peripheral and TF crates and carries the TTCrq mezzanine board with the TTCrx and QPLL ASICs. The TTC clock, Level 1 Trigger and synchronization commands are extracted

from the TTCrx ASIC. In local mode the CCB may generate these signals from its internal sources under the VME control. The 40MHz and 80MHz clocks from the QPLL ASIC are transmitted to other boards in the peripheral and TF crates over custom backplane using individual LVDS lines of the same length while the commands are distributed via GTLP bus. Further TTC signal distribution to on-chamber anode and cathode front-end boards is provided from the Trigger and Data Acquisition Motherboards using the LVDS links.

We describe in detail the CCB functionality and operating modes as well as

implementation of the TTC and Trigger Control transmission paths throughout the CSC system. Recent results of the slice and commissioning tests will also be presented

Poster session / 3

ALIBAVA : A PORTABLE READOUT SYSTEM FOR SILICON MICROSTRIP SENSORS

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A portable readout system for micro-strip silicon sensors has been developed. The system uses an analogue pipelined readout chip, which was developed for the LHC experiments. The system will be used to characterise the properties of both non-irradiated and irradiated micro-strip sensors. Heavily irradiated sensors will be operated at the Super LHC.
The system hardware has two main parts: a daughter board and a mother board. The daughter board contains two readout chips, analogue data buffering, power supply regulation and chip-to-sensor fan-in structures.. The mother board is intended to process the analogue data that comes from the readout chips and from external trigger signals, to control the whole system and to communicate with a PC via USB. There is provision for an external trigger input (e.g. scintillator trigger) and a synchronised trigger output for pulsing an external excitation source (e.g. laser system).
A prototype of the system will be presented as well as early measurements operating a silicon micro-strip sensor in a laser setup.

Parallel session B5 - ASICs 2 ILC / 4

Development of an ASIC for reading out CCDs at the vertex detector of the International Linear Collider

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The Linear Collider Flavour Identification Collaboration is developing sensors and readout electronics suitable for the International Linear Collider vertex detector. In order to achieve high data rates the proposed detector utilises column parallel CCDs, each read out by a custom designed ASIC. The prototype chip (CPR2) has 250 channels of electronics, each with a preamplifier, 5-bit flash ADC, data sparsification logic for identification of significant data clusters, and local memory for storage of data awaiting readout. CPR2 also has hierarchical 2-level data multiplexing and intermediate data memory, enabling readout of the sparsified data via the 5-bit data output bus.

Summary:

The ILC will bring into collision e+ and e- beams at centre-of-mass energies of initially 200 to 500GeV. The products of the resulting interactions will be recorded by two detectors. An important component of each of these is the vertex detector. This is designed to measure very precisely the tracks of charged particles close to the interaction point (IP), allowing the identification of those which originate from decay vertices displaced from the IP. Hence, particles containing b and c quarks and tau leptons can be efficiently detected.

To achieve the necessary precision, the vertex detector sensors must have a resolution < 5 microns and present a minimum of material to the particles which traverse them. The power consumption of the sensors and their associated readout systems must thus be small, allowing gas cooling. These requirements are fulfilled by CCDs, on which the LCFI Collaboration has concentrated its R&D efforts.

The high pair production backgrounds at the ILC require that the CCD pixel columns be read out in parallel at 50MHz if the occupancy is to be kept below the 1% desirable for pattern recognition. This requires a readout chip with a channel for each column of CCD pixels. The low occupancy makes on-chip data sparsification desirable. The CPR2 is a prototype which fulfils this requirement. The 250 channels of the chip are on the same 20microns pitch as the CCD columns. For test purposes, channels are divided into two types, half driven by charge preamplifiers directly coupled to the CCD outputs, the other half by voltage preamps connected to the CCD through source followers.

The amplified voltages are sampled and digitised at 50MHz. The 5-bit ADCs produce a modified Gray code which reduces the effect of single bit digitisation errors. This is fed to the cluster finding logic which computes the (6-bit) sums the data in two vertically separated pixels in the same column. This is added to the same sum produced by the channel to the right to produce the sum of a 2x2 group of pixels (7-bits). The result is compared with a 7-bit threshold. If the threshold is exceeded, nine 5-bit data words are stored in the channel buffer memory with a global, counter generated, 15 bit timestamp word (stored as three 5-bit words). The channel also triggers storage of the equivalent data for 3 neighbouring channels. Thus, the data for a matrix of 4x9 pixels is stored together with the associated timestamps. Since all channels perform the same operations, all possible 2x2 clusters are stored if the associated sum exceeds the threshold. Internal data storage is needed because the chip has only one (5-bit) output bus, the internal memories are continuously read out to the bus by a clock-driven multiplexer at 8 times the front end frequency.

Testing of CPR2 has confirmed its basic functionality. The next iteration (CPR2A) will incorporate improved digital functionality, with additional internal memory, to increase the efficiency of readout of clusters at occupancies of ~1% for an increased period of time.

Parallel session B1 - Trigger 1 Atlas / 5

The ATLAS Level1 Level2 Trigger Integration

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The ATLAS detector is designed to study the proton proton collision at the center of mass energy of 14 TeV with the bunch crossing rate of 40 MHz. In order to reduce this rate down to the level at which the events will be fully reconstructed, the multi-level trigger system is being deployed. The level 1 (LVL1) trigger reduces the rate down to 75 kHz via the custom-built electronics. The Region of Interest Builder (RoIB) delivers the Region of Interest (RoI) records to the level 2 (L2LV) trigger which runs the selection algorithms with the commodity processors and brings the rate further down to ~3 kHz. Finally the Event Filter (EF) reduces the rate down to ~200 Hz for permanent storage. The LVL1, LVL2 systems will be overviewed. The cosmic ray data taking in situ using partial detectors, the full trigger system and the DAQ system will be discussed. Results on system functionality, consistency in the full hardware and software chain based on the cosmic data will be presented. The trigger system performance will be shown with some critical quantities obtained by running preselected simulated events through the trigger and dataflow chains.

Summary:

The ATLAS LVL1 system identifies the basic signatures of interesting physics with high efficiency algorithms executed via custom electronics. It consists of three components, the Calorimeter Trigger, the Muon Trigger and the Central Trigger. The Central Trigger includes the Central Trigger Processor (CTP) and the Muon-to-CTP-Interface (MUCTPI). The MUCTPI obtains muon candidate information from the barrel and endcap muon trigger chambers, then produces muon multiplicities for six configurable transverse momentum (pT) thresholds. The Calorimeter Trigger system forms electron/photon, tau/hadron, and jet multiplicities as well as global event energy information. Based on these local trigger objects the CTP makes the trigger decision (L1A) with a configurable trigger menu. The L1A signal is distributed to all subdetectors to initiate readout of the triggered event. The LVL1 latency is required to be less than 2.5 us.

The ATLAS RoIB is a customized VME system. For each L1A it assembles a small amount of information of the objects identified at LVL1 (RoI fragments) from the LVL1 system into a full event record and passes it to the Level 2 Supervisors (L2SV). L2SVs distribute the records to the Level 2 processing farm which runs the high level trigger (HLT) algorithms. There event fragments are requested in fine granularity and a decision to accept or reject is made. Events accepted by LVL2 are fully assembled and formatted in the Event Builder (EB)'s destination nodes. Subsequently the complex selection algorithms are executed on complete events on the EF farms.

Integration tests of the LVL1 system, the LVL2 system and the DAQ system have been successfully performed by taking cosmic data with partial muon detector and calorimeter. Cosmic data have been recorded in situ and analyzed. The results show all subsystems function as expected and the full hardware and software chain installed at the experiment site works in a coherent and consistent way.

Integration and commissioning of the trigger and DAQ system at the experiment site are also being performed without the detector. Different tests have been done with preselected simulated proton proton events through the trigger and dataflow chains. The chain includes RoIB, LVL2, EB, EF and sometimes partial LVL1. The functionality and the stability have been scrutinized. Some critical quantities for the final system, such as the trigger rate and the event processing time, have been studied

using different trigger algorithms as well as different dataflow configurations.

Parallel session A1 - Systems, Installation and Commissioning 1 (DAQ, DCS, Cal) / 6

Infrastructures and installation of CMS DAQ

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At the time of this paper, all hardware elements of the CMS Data Acquisition System have been installed and commissioned both in the underground and surface areas. This paper describes in detail the infrastructures and the different steps that were necessary from the very beginning when the underground control room was only a building yard to a working system collecting data fragment from ~650 sources and sending them to surface for assembly and analysis.

Summary:

The data acquisition system for CMS is divided into an underground part and a surface part.

The underground part performs the following functions:
- Front End data collection over 650 sources and transmission to the surface on-line computing farm.
- Front End status collection and elaboration of a smart back pressure signal preventing the overflow of the Front End electronic.

The surface part performs the event building (640 event fragments assembled into a single event of ~1MB) and later-on, the on-line analysis to select the events to be stored for off-line analysis.

Year 2005 has been dedicated to the production/test of the custom made electronic boards and the procurement of the commercial items needed to operate the underground part of the Data Acquisition System of CMS.
The first half of 2006 has been spent to install the DAQ infrastructures in USC55 and to prepare the racks to receive the hardware elements.
The second half of 2006 was dedicated to the installation and cabling of the CMS DAQ elements in the underground control rooms.
Concurrently, the infrastructures in the surface building were installed and cabling of the computer room started early 2007.
The event builder PCs have been installed and commissioned this summer. They will act also as event analyzers as long as the data volume does not require dedicated PCs to run the high level trigger algorithms. It is foreseen to procure and install analyzer PCs in the second half of 2008.

Poster session / 7

Development of a Front-End Electronics for Pico-second Resolution TOF Detectors

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We have proposed using 2" by 2" micro-channel plates (MCP-PMTs) with a novel equal-time anode and with capacitive return path coupling to measure the time-of-flight of relativistic particles, with the goal of being able to construct large-area TOF detectors with a resolution of 1 psec.

The proposed front-end customer chip is a time stretcher with 1ps resolution, building with IBM 0.13um SiGe BiCMOS process. the preliminary designs and simulations for the front-end ASIC chip will be presented in this paper.

Summary:

The proposed readout electronics for each MCP-PMT unit consists of 4 identical front-end ASICs and one DAQ ASIC that digitizes the front-end outputs, distributes the system clock, and handles all digital traffic. The front-end ASIC chip is a 'time stretcher', converting the difference in times between start and stop pulses into a digital pulse with width proportional to the input time interval but stretched by a factor of 200. We are designing in the IBM 0.13um SiGe BiCMOS 8HP process, The circuitry includes a limiting amplifier and a constant-fraction discriminator. The DAQ chip then digitizes the stretched time interval. The preliminary design and detailed simulations of the front-end ASIC chip will be presented.

Poster session / 8

Status of the Optical Multiplexer Board 9U Prototype

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The Optical Multiplexer Board is one of the elements present in the Read Out chain of the Tile Calorimeter in ATLAS experiment. Due to radiation effects, two optical fibers with the same data are sent from the Front End Boards to this board, which has to decide in real time which one carries good data and pass them to Read Out Driver motherboard for processing.
The paper describes the design, tests and status of the first prototype, implemented as a 9U VME64x slave module, including both hardware and firmware aspects. In this last, algorithms for Cyclic Redundancy Code checking are used to make the decision. Besides, the board may be used as a data injector for testing purposes of the Read Out Driver motherboard.

Summary:

TileCal is the hadronic calorimeter of the ATLAS experiments. It consists, electronically speaking, of 10000 channels to be read each 25 ns. Data gathered from these channels are digitized and transmitted to the data acquisition system (DAQ) following the assertions of a three level trigger system.
The main component of the back-end electronics of the TileCal sub-detector is

the Read-Out Driver (ROD) which is placed between the first and the second level trigger level. The ROD has to pre-process and gather data coming from the Front End Boards (FEB) and send these data to the Read-Out Buffers (ROB) in the second level trigger.
To reduce data loss due to radiation effects, the TileCal collaboration decided to include data redundancy in the output links of the FrontEnd. This was accomplished using two optical fibres which transmit the same data. At ROD system level, data redundancy is used to discard the fibre with errors due to radiation.
The checking is based on rightness of the Cyclic Redundancy Codes (CRC) of the data packets on both fibres. This is also necessary as the ROD motherboard is expecting just one fibre per channel. For this purpose a new module, called Optical Multiplexer Board (OMB) was conceived. This board would be able to provide, in case of error in one link, the correct data to the ROD input by analyzing the Cyclic Redundancy Codes (CRC) of the data packets on both fibers coming from the FEB.
In the development of the work a new functionality for OMB was proposed. Because RODs should be tested in production stages and provided that in the first moments of LHC operation data may not always be available from front-end, it was suggested to include a “Data Injector Mode” to use the OMB like data pattern injector for ROD test and verification tasks.
The interest of this project was justified in February 2003, when a preliminary study appeared. This proposal shown a solution for OMB based on exhaustive on-line analysis of the data carried by both of the fibbers, using FPGAs for implementation.
The excellent results of the first OMB 6U prototype are described in this paper as well as the functional description and technical specifications of the final OMB 9U prototype. In this paper we show the status of this new OMB 9U Prototype.

Parallel session B3 - Trigger 3 / 9

The ALICE trigger electronics

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Summary:

The ALICE trigger system (TRG) consists of a Central Trigger Processor (CTP) and up to 24 Local Trigger Units (LTU) for each subdetector. CTP receives and processes trigger signals from trigger detectors and output from CTP are 3 levels of hardware triggers L0, L1 and L2. 24 trigger detectors are dynamically partitioned into up to 6 independent clusters. The trigger information is propagated through the LTUs to the Front-end electronics (FEE) of each subdetector via LVDS cable and optical fiber. The trigger information, which is sent from LTU to FEE can be monitored online for possible errors by the newly developed TTCit board.
After commissioning of TRG with each detector on surface, the ALICE trigger electronics has been installed and tested in the experimental cavern with appropriate ALICE experimental software. One setup is used for testing on the surface; the others are installed in experimental cavern.
This paper describes the current status of ALICE trigger electronics, online error trigger monitoring and appropriate software for this electronics.

The ALICE trigger system operates with interaction rates for nucleus-nucleus, proton-nucleus and proton-proton runs between about 8 kHz and 300 kHz. The main block of the ALICE trigger electronics is the Central Trigger Processor (CTP). The CTP is implemented using 6 different types of 6U VME board, together making up eleven active boards for the CTP. This block will receive and align up to 60 trigger inputs in parallel from the trigger detectors; it then processes trigger information inside cluster and generates result of processing. There are three different trigger levels (L0, L1 and L2) with latencies from 1.2 microseconds to 88 microseconds. The system allows dynamic partitioning in order to make optimum use of detector readout. The system provides a flexible past-future protection. The L0 trigger is sent as an LVDS signal or optionally via the Channel A of the TTC system. The L1 signal is sent on channel A of the TTC system and trigger data associated with level 1 are sent as a message on channel B of the TTC system. The L2 trigger is sent as a message on the TTC system after a delay, currently 88 microseconds, to allow for the longest required past-future protection interval.
Outputs from the CTP go to the LTUs of each subdetector. The LTU serves as an interface between the CTP and the subdetector readout electronics. The LTU is able to run also in the stand-alone mode of operation and the LTU fully emulates the CTP protocol and enables sub-detectors to carry out development, test and calibration tasks independently of the CTP. The timing of emulated trigger sequences is identical to the timing during the global run. The LTU can generate incomplete sequences or different types of errors can be introduced, either randomly or “on demand” (the option is available in both the global mode and the stand-alone emulation mode), all in order to verify the capability of the FEE to check the consistency of trigger information.
The trigger electronics is based on ALTERA Cyclone FPGAs (Field Programmable Logic Arrays), which provide flexibility to change the functionality of the trigger system by reprogramming FPGA. The system provides a range of monitoring and debugging options. Snap-shot memories enable detection of any system inconsistency and an identification of possible faults. Around 1200 counters, including many redundancies, are read in regular intervals (1 minute), which provides relevant physics information and also verify the consistency of the hardware operation.
In order to monitor and recognize possible errors in the trigger timing and the errors in trigger messages the TTCit board has been developed. The board can monitor the optical output of a trigger partition. In case of an error the information is displayed on the front panel. For detailed information and a precise identification of errors, a snap-shot memory can be read-out. The snap-shot memory contains information triggered by error in tree modes: pre-trigger, middle-trigger or post-trigger.
The ALICE Trigger system, including the Local Trigger Unit electronics, has been commissioned with all ALICE detectors on the surface and in the pit in parallel. Currently it is installed in the cavern where the full system is integrated with appropriate experimental software (Trigger - TRG, Experiment Control System - ECS, Data Acquisition System - DAQ and Detector Control System - DCS).

Poster session / **11**

A Trigger/Timing Logic Unit for ILC Test-beams

Author: David Cussans[1]

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ILC not a triggered experiment, but during detector development it may be useful to operate in a triggered mode. A Trigger/Tagging Logic Unit (TLU) is described which allows triggered operation, with option of smooth transition to triggerless, data-driven mode. The TLU is being

developed as part of the EUDET programme to develop test-beam infrastructure for ILC detector development.

Summary:

Introduction:

ILC not a triggered experiment, but during detector development it may be useful to operate in a triggered mode. A Trigger/Tagging Logic Unit (TLU) is described which allows triggered operation, with option of smooth transition to triggerless, data-driven mode. The TLU is being developed as part of the EUDET programme to develop test-beam infrastructure for ILC detector development.

At detectors with a pipe-lined trigger, for example the LHC and HERA experiments, the front-end links operate at a multiple of bx-clock to minimize latency for the first-level hardware trigger. Because the ILC detectors will not be triggered locking the link clock frequency need not be a multiple of the ILC bunch-crossing clock, allowing the use of COTs data-link technology. However, in data-driven operation a clock and control signals must still be distributed to the detectors to enable the data to be time-stamped where it modes from pipelined, fixed latency, to buffered data-driven.

Aims:

Because the ILC detectors will operate in a data-driven, triggerless mode any triggered test-beam operation for development of detectors should be as simple as possible - since it is not a “stepping stone” to the eventual system.

Simple and low cost enough to be widely distributed. Ideally, each group developing detectors should be able to have at least on TLU. It is hoped to place few *demands* on user whilst being as flexible as possible.

Description:

The TLU will be able to operate in two modes. Firstly a “classic” trigger/busy triggered mode with hand-shake. Secondly as a “Tagging” logic unit providing the time-stamp information needed for a data-driven system.

In the triggered mode, the TLU and each device has four signals connecting them: Trigger/Busy/Reset/DUT-Clock. Once a trigger has been sent from the TLU to a device and a busy signal sent from the device to the TLU the device can optionally clock out trigger information from the TLU on the trigger line.

In “tagging” (data driven) mode mode a separate low-jitter clock tree fans out a system-level clock to all test-beam devices. The TLU receives the system clock and produces a manchester encoded serial data stream which is fanned out to all system devices together with the system clock. The simple encoding, at the bit-rate equal to the system clock, allows the serial data to be decoded in an FPGA without the aid of an external clock recover unit. The serial data stream carries spill-on/spill-off (bunch train present) information and the spill(bunch-train) number.The TLU also keeps a record of time-stamps for incoming triggers.

Implementation:

Number of units is likely to be relatively low and the life-span is modest (~ 5 years). This suggests the use of a COTS FPGA module coupled to a custom motherboard and using off-the-shelf USB interface firmware and software drivers rather than totally custom hardware and firmware/software.

Cypress EZ-USB microcontroller with USB interface used to interface beween Xilinx Spartan xc3s1000 FPFGA and USB2.0.

Interface to the test-beam device under-test is via RJ45 connectors with LVDS levels. There are six DUT interfaces. Four 50-Ohm terminated coaxial connectors accept NIM,TTL or photo-muliplier level pulses and receive a trigger for each particle passing through the test-beam. The arrival of each trigger is time-stamped. In triggered mode the arrival of a trigger will cause a trigger to be issued to active DUTs, unless the DUT have indicated that they are busy.

The FPGA is configured via the USB interface. A memory-mapped interface is used for set up via the host interface and block transfer is used to transfer time-stamps from the TLU to the host computer.

Status:

An implemention of the TLU suitable for triggered mode already exists and is due to be used in test-beam this year. The low-jitter clock distribution system needed for operation in “tagging” mode has not yet been constructed.

Parallel session A4 - Systems, Installation and Commissioning 2 (TK and Pix) / **14**

The ALICE Silicon Pixel Detector system

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The ALICE silicon pixel detector (SPD) comprises the two innermost layers of the ALICE inner tracker system. The
SPD includes 120 half staves each consisting of 10 ALICE pixel chips bump bonded to two silicon sensors and one
multi-chip read-out module. Each pixel chip contains 8,192 active cells, so that the total number of pixel cells in the
SPD is ≈ 10^7. The on-detector read-out is based on a multi-chip-module containing 4 ASICs and an optical
transceiver module. The constraints on material budget detector module dimensions are very demanding. An
overview of the electronics integration, test results and test procedures are presented.

Summary:

1. SPD layout The ALICE silicon pixel detector (SPD) consists of two barrel layers at radii of 3.9cm and 7.6cm, respectively. The basic detector module is the half-stave, in which the active elements are two ladders glued to a multi-layer Al flexible flat cable carrying power and signal lines. Each half-stave consists of 10 pixel chips bump bonded to two silicon pixel sensors (70.7 x 16.8 mm2) and is read out by a multi-chip module. Each pixel chip contains a matrix of 8192 cells. The SPD contains 9.83 x 10^6 pixel cells in total. The half-staves are mounted on 10 light-weight carbon fiber sectors, each sector supporting 4 half-staves on the inner layer and 8 half-staves on the outer layer. The pseudorapidity coverage of the inner layer is $|\eta| < 1.95$.
2. SPD electronics 2.1. Electronics system architecture The pixel chips provide binary hit information, which is stored in a delay line during the L1 trigger latency. In case of a positive L1 decision the hit is stored in one out of four multi event buffers where the data wait for the L2 trigger decision to be read out or discarded. In each half-stave, a multi-chip module (MCM) initiates the read-out and performs the configuration process of the pixel chips. The connection to the control

room is established via three optical fibers. The MCM contains three ASICs and a custom developed 800 Mbit/s optical link for the data transfer between the detector and the control room. All on-detector ASICs have been implemented using a commercial 0.25μm CMOS process; radiation hardness is obtained by appropriate gate design rules and by redundancy in the critical nodes. In the control room FPGA-based electronics performs zero suppression, data formatting and sends the data to the ALICE data acquisition system.

2.2. Electronics integration
The compactness of the design sets severe constraints on the material budget and dimensions of the detector
elements and the interconnects.
The very small clearance between the SPD inner layer and the wall of the beam pipe requires that the overall
radial thickness of the half staves is less than 3 mm. The width of the half-staves is determined by the pixel chip
dimensions; the clearance between the edges of adjacent half-staves is down to ≈ 0.2mm and the width of the
MCM substrate is limited to 11mm in order to avoid interference with the other structural elements. In order to
keep the material budget within 1% X0 (each layer), the read-out chip and the sensors are 200 μm thick and the
pixel chips are thinned down to 150 μm. The interconnection between the pixel chips and the read-out MCM is
established via an multi-layer flexible bus in which aluminium layers are used as conductor to even further reduce
the material budget.

2.3. Full system and production tests
Full system tests in beam setups and in the laboratory of the entire detector system including the sensors, pixel
read-out chips, the multi-chip module, the optical links, the off-detector electronics, the ALICE trigger system and
the ALICE data acquisition system have been performed.
2.4. Summary
The tight material budget and the limitation in physical dimensions required by the detector design introduce new
challenges for the integration of the on-detector electronics. The full system as well as an overview of the
integration of the on-detector electronics are presented.

Parallel session B6 - ASICs 3 future / 15

Development of SEU-robust, radiation-tolerant and industry-compatible programmable logic components

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Most of the microelectronics components developed for the first generation in LHC experiments have been defined and designed with very precise experiment specific goals and are hardly adaptable to other applications. In an effort to cover the needs for generic programmable components often needed in the real world, an industry-compatible Programmable Logic Device (PLD) and an industry-compatible Field-Programmable Gate Array (FPGA) are now under development.

This effort is targeted to small volume applications or to the cases where small programmable functions are required to fix a system application. The PLD is a fuse-based, 10-input, 8-I/O general architecture device compatible with a popular commercial part. The FPGA under development is instead a 32×32 logic block array, equivalent to ~25k gates, in 0.13 micron CMOS. SEU-robust registers are employed for configuration registers as well as for user data flip-flops. Test results for both chips will be presented.

Summary:

The harsh radiation environment present in the vicinity of high-intensity-beam particle accelerators, necessary for High Energy Physics (HEP) experiments like the LHC, requires so far the utilization of custom-designed Application-Specific Integrated Circuits (ASICs), and forbids instead the exploitation of standard commercial programmable logic components. Future experiment and upgrades would benefit from the flexibility of programmable logic covering the need for small volume applications or where simple logic functions are necessary. Within this perspective, two industry-compatible radiation-tolerant devices are under development, respectively a Programmable Logic Device (PLD) and a Field-Programmable Gate Array (FPGA), targeting two different types of applications. Studies performed on the radiation effects on most commercial programmable logic parts have proved them to be often sensitive to both Total-Ionizing Dose (TID) and Single-Event Upsets (SEUs). SEUs can occur in the user logic and, in case of SRAM-based devices, also in the configuration registers. When such a register is corrupted, the user logic can end up being modified, therefore the functionality can be affected and compromised.
This work focuses on the development of programmable logic designed to be SEU-robust and TID-tolerant. Our final aim is the creation of an FPGA and a PLD where SEU insensitivity is built-in, thus not requiring the user to exploit special technique for SEU protection.
SEU-hardening circuit and layout techniques were employed for the design of a robust register based on the Dual-Interlocked Cell (DICE). The sensitivity of the SEU-robust register topology was assessed on a test chip fabricated in a 0.25 micron technology. The circuit proved to be insensitive up to an LET of 79.6 cm2MeV/mg showing minimal sensitivity at higher LETs. The structure of the register will be described in this paper.
The SEU register was exploited also for the development of a fuse-based PLD. The configuration fuses are intrinsically hard to SEUs while the user logic is protected by the SEU-hardened structure. The PLD is a 10-input 8-I/O general architecture device compatible with most commercial parts. The PLD structure will be described.
The target FPGA device is an SRAM-based 32×32 logic block matrix which uses the SEU-robust register for both configuration and user data in order to attain maximum reprogrammability together with SEU hardness. The FPGA could be used as a stand-alone chip or as an IP-core. The FPGA fabric under development will be described.
Both devices can easily be programmed using the same development tools available for the corresponding commercial parts and adapted to our specific implementation by a simple post-processing tool. Device programming considerations will be discussed.

Parallel session A1 - Systems, Installation and Commissioning 1 (DAQ, DCS, Cal) / 16

Performance Study of the CMS Ecal Electronics using electrons from 15 GeV to 250 GeV

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The experimental conditions and physics goals of LHC experiments set challenging specifications for detectors and their readout electronics. The CMS Electromagnetic Calorimeter (Ecal) is an example of a complex system in which every component needs to be understood in detail in order to ensure the quality of the physics results.
In 2006 9 ECAL supermodules were exposed to an electron test beam in the energy range from 15 GeV and 250 GeV. Many aspects of the calorimeter response have been studied in detail.
We will describe the results of these studies, with emphasis on the contribution of the electronics to linearity, resolution and noise of the system.

Parallel session A4 - Systems, Installation and Commissioning 2 (TK and Pix) / 17

Test and commissioning of the CARLOS control boards for the ALICE Silicon Drift Detectors

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Co-authors: Alessandro Bruno [2]; Alexandre Rashevsky [3]; Angelo Rivetti [4]; Davide Falchieri [1]; Enzo Gandolfi [1]; Filippo Costa [1]; Flavio Tosello [4]; Gianni Mazza [4]; Giuseppe Giraudo [4]; Jiri Kràl [5]; Lodovico Riccati [4]; Luca Toscano [4]; Massimo Masetti [1]; Paolo De Remigis [4]; Paolo Giubellino [4]; Richard Wheadon [4]; Serhiy Senyukov [2]; Silvia Coli [4]; Stefania Beolè [2]

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The paper presents the test strategy and its results during the installation of the CARLOS end ladder board. This board is able to compress data coming from one Silicon Drift Detector (SDD) front-end electronics and to send them towards the data concentrator card CARLOSrx in counting room via a 800 MBit/s optical link.
The paper describes the integration of the CARLOS end ladder boards, including its cooling system, mechanical supports, the low voltage distribution, various signal cables and optical fiber patch panels. The complexity and installation sequence require tests at each step of the installation.

Summary:

The Inner Tracking System (ITS) of the ALICE experiment contains six coaxial cylindrical layers. Layers 3 contains 14 ladders each one hosting 6 SDDs (Silicon Drift Detectors), while layer 4 contains 22 ladders each one hosting 8 SDDs. The CARLOS end ladder board is placed on both sides of each ladder with the purpose of acquiring and compressing data coming from each SDD before sending them towards the data concentrator card CARLOSrx in counting room through optical fibers. The board contains the compression chip CARLOS that performs a bi-dimensional compression of the data coming from the SDD front-end electronics (called SDD module). CARLOS 16-bit output bus is encoded with 8B/10B Ethernet protocol and sent to a 800 MBit/s single mode optical fiber using a 1310 nm optical laser.
The CARLOS end ladder board receives the trigger signals and the configuration parameters through a 40 MBit/s serial signal coming from CARLOSrx through an optical fiber and converted using a photodiode.
An other photodiode is used for receiving the 40.08 MHz clock coming from the TTC system. The QPLL ASIC on the end ladder board allows to obtain a clock with a peak-to-peak jitter lower than 50 ps that is used both for the serializer (ASIC GOL) of the board and for the front-end electronics.
A special control unit has been developed with the purpose of monitoring parameters such as voltage, current and temperature related to the whole readout chain. The

control unit is remotely controlled from the DCS (Detector Control System) board through the I2C bus. The CARLOS end ladder board also provides power for the analog and digital voltages of the front-end boards under the control of the DCS system. Each ladder has been tested with the use of the complete readout electronics system, developed for ALICE SDD experiment, including its cooling system. The same test was repeated when the ladder was assembled in cylindrical layers (layer 3 and 4) and, in particular, the noise level due to different ladders working at the same time was observed. The system was successfully tested, especially for what concerns data transmission and reception of information via optical links (780 Optical Links are used to process signals from the SDD-detectors and to send the results to the off-detector electronics). Moreover the low voltage distribution and the DCS feature were fully tested and the results confirm the efficiency of the readout electronics, chosen for ALICE SDD experiments, which is integrated in the CARLOS end ladder board.

Poster session / 18

CARLOSrx: an on line Data Acquisition system for ALICE ITS SDD

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Co-authors: Davide Falchieri [1]; Enzo Gandolfi [1]; Massimo Masetti [1]; Samuele Antinori [1]

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The data concentrator card CARLOSrx is a readout board developed for the ALICE ITS Silicon Drift Detector (SDD) experiment held at CERN.
CARLOSrx is a 9Ux400 mm VME board, containing 4 FPGAs with the purpose of processing data coming from 12 SDD detectors and sending them to a computer running the DATE software. Twentyfour boards are installed for SDD. We have implemented and tested a new firmware version of CARLOSrx able to communicate with 12 SDD detectors, trigger system and DAQ software.
The paper presents the results of these tests.

Summary:

Each CARLOSrx is a board of remarkable dimension, 9U x 400 mm VME, which will be inserted in a VME crate situated in a counting room during the run of ALICE experiment.The most important tasks of CARLOSrx are to receive data from SDD detectors and send them to ALICE Local Data Concentrator (LDC) for the correct reconstruction of the acquired events.
Each CARLOSrx communicates with the front end electronics via single mode optical fibers, in particular way the hardware configuration is able to download the configuration, clock and to receive the events for 12 SDDs detectors through 36 optical. To do that on the CARLOSrx board is mounted the CERN SIU board of the Detector Date Link (DDL) developed for the ALICE experiment. In the same time the board includes the CERN TTCrq mezzanine card that is used for trigger information, clock and busy management with ALICE Local Trigger Unit (LTU). The power supply and firmware configuration for this board is provide by VME bus.
CARLOSrx is composed principally of 4FPGAs (three process the data coming from detector and one handle the VME bus) and 4 FIFO hardware (256 Kword x 32 bits) that buffer the data during the operations of board.
The CARLOSrx firmware has been tested first in Bologna and Torino and now at CERN for long time and is able to send JTAG instructions and clock to all front end electronics, receive data coming from 12 modules (one module is composed by one detector and the front end electronic needed to digitalize and send data to CARLOSrx), pack and label data and finally send them to a LDC.
Each CARLOSrx was connected to 6, 8, or 12 modules, and it was able in every situations to send data correctly to LDC; the trigger rate with 12 modules connected to the board was 90 Hz producing a throughput of 160 MB/s, without compression. Every

single event acquired was checked and no error was found.
Now it is under test a new firmware where has been implemented new features like, modularity with granularity 1, so CARLOSrx is able to receive data coming from one or more modules at the same time (this important feature permits CARLOSrx to eliminate a module with problem and continue to acquire data), error management. In this way CARLOSrx is able to reject events: this command is sent from the trigger system. Moreover a RS232 interface has been developed to debug the board during data acquisition (a custom software takes the control of RS232 port of PC in this way is able to send some commands to CARLOSrx and check the value of some registers and signals during the run).
A custom software has been developed to analyze the data produced by CARLOSrx. This software is completely automatized and it is able to find eventual errors caused by a wrong behavior of CARLOSrx and or front end electronics.

Parallel session A6 - Systems, Installation and Commissioning 4 (Lumi, MU) / 19

Time calibration of the LHCb Muon System

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The LHCb Muon System consists of about 122,000 readout channels. It plays a basic role in the first trigger level. The trigger requires 95% efficiency in Muon tracks detection. It is then necessary to reach a system time alignment at the level of about 2 ns. This alignment must be monitored against possible fluctuations due to changes in the detector operating conditions. We describe the custom instrumentation implemented at system level for time calibration, the strategy adopted, the procedure to be followed both for system alignment and monitoring, the control program realized for this purpose. We also illustrate first results obtained during the detector commissioning in the LHCb pit.

Summary:

The LHCb Muon detector plays a crucial role in the first trigger level. It is realized by means of Multi-Wire-Proportional-Chambers and Gas-Electron-Multipliers and consists of about 122,000 front-end channels.
High efficiency is necessary both at detector and front-end level to satisfy the trigger requirement of 5 hits per 5 Muon stations (layers of detectors) with an overall efficiency of 95%. This corresponds to having a single front-end channel detection efficiency of 99% within a time window of 20 ns and poses the problem of an accurate time calibration of the whole detector.
The Muon trigger processes the binary information coming from the Muon detectors according to a pipelined architecture, starting to process a new event every 25 ns (Bunch Crossing – BX). The Muon trigger expects Muon data being tagged with an identifier of the specific BX they originate from. However, considering the width of time distributions due to the intrinsic detector resolution, in order to reach the requested trigger efficiency, it is necessary to calibrate the internal system delays at the level of about 2-3 ns.
Starting from the above requirements, the Muon System has been conceived and realized containing specific tools for time calibration at the channel level. Several reasons cause the system channels to be naturally misaligned in time: time of flight of particles through detectors, different cable lengths, different number of electronics stages to be crossed.
The basic strategy for system time calibration is to measure the hit time of arrival at the ODE board level, just before the hits are dispatched to the muon trigger.
Inside the SYNC chip, placed on the ODE, time spectra can be built on each input channel. SYNC is a custom chip, containing eight Time-to-Digital-

Converters, one per channel. Two kinds of time spectra can be built: a coarse-time histogram, based on the current BX number, and a fine-time histogram, based on the hit phase with respect to the rising system clock edge. The first histograms have bins of 25 ns, while the second ones have bins of 1.5 ns. Also the fine-time histograms must be centered to reach the requested detector efficiency. Two different adjustments are possible:
• The SYNC BX counters, which allow moving time in steps of 25 ns clock cycles;
• The programmable delays, placed on the front-end boards (DIALOG chip), which allow moving time in 32 steps of 1.6 ns.
A first rough system alignment can be obtained using a system pulsing network, which we have embedded in our electronics. However, an accurate System calibration is possible only by measuring the time of arrival of detected particles coming from beam interactions and building time histograms with significant statistics.
The information gathered on the SYNC histograms is the basis for a system-wide analysis aimed at finding the general alignment of the detector. The alignment procedure of all the 122000 front-end channels is the basis for a System Control Program aimed at system time calibration, which is presently being used during system and detector commissioning.

Parallel session A5 - Systems, Installation and Commissioning 3 (TK and Pix, Lumi) / 20

Status of the ATLAS Pixel Detector

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The ATLAS silicon pixel detector is nearing completion for operation at the Large Hadron Collider at CERN. The ATLAS pixel detector contains approximately 80 million channels and 1744 detector modules. Electronics and module fabrication and testing is complete, as well as system integration of major elements of the pixel detector.
The overall status of the ATLAS pixel detector will be presented, emphasizing systems issues and lessons learned in fabricating this new type of detector for hadron collider experiments.

Poster session / 21

System test for the ATLAS Pixel Detector data acquisition

Author: Clara Troncon[1]

[1] *Univ. + INFN*

The ATLAS Pixel Detector is an 80 M channels silicon tracking system designed to detect charged tracks and secondary vertices with very high precision. To verify that the integrated assembly will perform as expected subsequent to installation into the experimental area, a fraction (10%) of the detector and the requisite ancillary services has been assembled and operated in a laboratory setting. We refer to this as system testing, and results from these tests will be presented.
The talk will illustrate all the aspects of the system test, including the detector control and safety system, the monitoring system and the DAQ system, the data base technologies used to store the configuration

and condition data, the techniques for calibrating the detector and the analysis of noise tests and cosmic data.

Parallel session B3 - Trigger 3 / 22

Data transmission and selection for the L0 calorimeter trigger of LHCb.

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This report describes the Selection Crate, designed by INFN for the L0 calorimeter trigger of the LHCb experiment.
The Selection Crate is a modular system which consists in 8 Selection Boards (SB) used to select the most energetic clusters detected by the electromagnetic and hadron calorimeters, as well to evaluate other global trigger variables.
A SB is equipped with 28 x 1.6 Gbps optical inputs and 3 x 1.6 Gbps optical outputs.
The slow control is achieved by using a onboard diskless ethernet-booting CreditCard PC with a related GlueCard bus converter, while a TTCrq board provides the fast control TFC signals of the LHC TTC system.
Each SB receives data from the front-end through 3 MPO ribbon connectors and sends data to the trigger decision unit through single channel optical links.
All the optical links are suited for multimode, 1.6 Gbps, 850 nm fiber with sync patterns and 8B/10B coding. The optical transmitters used throughout the calorimeter have been designed by INFN Bologna. The optical transmitter boards are capable of sending on a single fiber up to 8 x 32bit at the LHCb clock of 40.08 MHz.

Poster session / 23

Results and Consequences of Magnet Test and Cosmic Challenge for the CMS Barrel Muon Alignment System

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In the last year – as part of the CMS test called Magnet Test and Cosmic Challenge (MTCC) - about 25% of the full CMS Barrel Muon Alignment System was built and operated. The configuration enabled us to test all the elements of the system and its function under real conditions. In the paper the setup –including the read-out and control- is described and the first preliminary results are presented. The correct operation of the system has been demonstrated. About 500 full measurement cycles have been recorded and evaluated.

Summary:

In the past years the development of the CMS Barrel Muon Alignment system has been reported in regular papers presented at LECC conferences. In the last year – as part of the CMS test called Magnet Test and Cosmic Challenge (MTCC) – two sectors of the CMS Barrel Muon detector was equipped with the elements of the Barrel Muon Position Monitoring (Alignment) system. It consisted of 42 muon chambers, 10 rigid mechanical structures called MABs and 2 z-bars. These elements were holding 1800 LED light sources and 100 video-cameras connected to 10 PC/104 computers (called Board PC). This setup represented about the 25% of the final position monitoring system. All the elements had been calibrated according to the calibration scheme reported earlier. During the MTCC 14 muon chambers were operated as active muon detectors. For these chambers the LED light sources were controlled thorough the chamber control system as it is foreseen for the final CMS operation. For the others special LED control units called PIConNETs have been developed and used.
The global control and readout was performed using a dedicated Ethernet network consisting of a central measurement controller PC, 10 Board PCs and 28 PIConNET units. There were several goals of the tests during the MTCC. One group is related to the operation of the system. The other group of tasks was related to the observation of the deformations and movements of the CMS barrel and the barrel muon chambers during the operation, especially the effects related to the magnetic field.
During the two phases of the MTCC the system was operated regularly, in the second phase (Oct 2007) continuously. More than 500 measurement cycles have been completed. The results can be summarized as follows:
- The system worked correctly and provided results that could be interpreted.
- The dynamic running scheme has proved to be very efficient leading to fully parallel operation of the board PCs.
- A full cycle lasted about 100 minutes. This is already acceptable for future CMS operation, however, significant improvements are possible in the future.
- Control of the operating muon chambers through the chamber DCS system went smoothly even at the maximum load of this channel.
- A separate test has been made during the MTCC to check the operation of commercial Ethernet switch units in magnetic field. This test was also successful.
- The resolution of the system in the most important phi-direction is ~20 micrometer, well below the specification. This enabled us to detect even thermal deformations due to the daily cycle.
- The irreversible deformation (shrinkage) of the full barrel yoke during the first magnet operation as well as the elastic deformation under field during the changes of the magnetic field have been observed and the result is in good agreement with the preliminary finite-element calculations.

Parallel session B4 - ASICs 1 FE chips / 24

Development of a small-scale prototype of the GOSSIP chip in the 0.13um CMOS technology.

Authors: Ruud Kluit[1]; Vladimir Gromov[1]

Co-author: Harry van der Graaf [1]

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Abstract.
The GOSSIP (Gas On Slimmed Silicon Pixel) detector is a candidate to be a good alternative for silicon based pixel detectors. The Gossip chip is being developed to serve as a read-out array for such a gas-filled detector. Thanks to the very low capacitance at the preamplifier input, the front-end of the chip demonstrates low-noise performance in combination with a fast peaking time and low analog power dissipation. Measurement of the drift time of every primary electron enables 3D reconstruction of the particle's track. For this purpose Time-to-Digital converter must be placed in each pixel.
A small-scale prototype of the GOSSIP chip has been developed in the 0.13µm CMOS

technology. The prototype includes a 16 by 16 pixel array. Each pixel is equipped with the front-end circuit, threshold DAC, and a high resolution 4-bit TDC. The chip will be available for testing in May 2007 and after initial tests it will be processed to build a prototype detector.

Summary:

Summary.
The GOSSIP (Gas On Slimmed Silicon Pixel) chip is a CMOS pixel array with a fine grid (e.g. micromegas) placed at a distance of 50μm on top of it by means of wafer post-processing technology. One mm above this grid the cathode foil is placed. The cathode foil and the grid are put at -800V and -400V, respectively, and the pixel array surface is at ground potential. The volume between the drift foil and the pixel array is filled with a suitable gas mixture. When a minimum ionizing (MIP) particle passes the drift gap, about 10-50 electron-ion pairs will be created along the track. Driven by the electric field the electrons will drift towards the pixels. In the grid-to-pixel gap an avalanche multiplication occurs making the sufficient charge to activate an on-pixel integrated circuit. The activated pixels are a projection of the track on the array surface. Moreover, the drift time measurements at the activated pixels will allow 3D track reconstruction.
A number of features make the GOSSIP chip advantageous for future particle detectors. It has no thick silicon sensor bulk, but a gas volume instead. Therefore it has a low material budget and it is free from the radiation damage effects in the depletion layer of the silicon sensor. The on-pixel circuitry will be radiation hard due to the internal properties of the up-to-date deep-submicron CMOS technology.
In the first prototype [1] we designed a front-end for a pixel as small as 55μm by 55μm. The low value of the parasitic capacitance at the input of the preamplifier let us design a low-noise (ENC=60e rms) and the same time very fast (40 ns peaking time) and low power (2μW per channel) front-end circuit including a CMOS comparator. The low power aspect is of primary importance since any additional cooling system involves an increase of the material budget. The chip demonstrated low sensitivity for digital crosstalk and the new design with a TDC in each pixel cell should validate this. This requires careful layout of the input traces in combination with common usage of the isolated NFETs and an increased amount of substrate contacts throughout in the circuit.
The main goal of the present prototype of the GOSSIP chip is to build a real small-scale detector capable of the particle track reconstruction. For this purpose we have designed a 16 by 16 pixels array. The total sensitive area is 0.88 mm2 with a pixel size of 55μm by 55μm. To compensate the channel-to-channel threshold spread a 4-bit DAC is added in each pixel cell.
In order to measure drift time each pixel cell contains a TDC. Its function is to digitize the time interval between the moment when the pixel has been hit and the end of the 40 MHz clock signal (LHC bunch cycle). This value gives the time that a particle has passed through the detector. The TDC is made of a pulse controlled local oscillator on the basis of a 2-input NAND gate with a chain of inverters in feedback. The circuit starts oscillating on the positive edge of the output signal of the comparator (hit signal) and stops at the positive edge of the clock signal. The oscillator is followed by a 4-bit pulse counter in the form of a linear feedback shift register. This circuit counts the number of pulses at the output of the oscillator. The resulting value is the digital code of the drift time. Time resolution of the TDC (1.6 ns) is determined by the delay in the feedback of the oscillator. Quality of this type of TDC is set by the temperature stability of the chain of inverters together with its sensitivity to the drift of the power supply voltage. Simulations show that the error is lower than LSB when the TDC operates within the temperature range 30 degrees and the power supply range 60 mV.
In a test situation the trigger signal comes much later than the particle. The hit time slice will be defined with the help of a 4-bit latency counter. It gives a number of full 40 MHz clock cycles between the hit signal and the trigger signal. If the trigger signal does not show up within 15 clock cycles both the latency counter and the drift time counter will be reset.
After receiving the trigger signal all 256 pixels of the array will be sequentially read-out.
For better testability we are able to feed the test signal to each pixel separately and mask bad pixels. A serial link is used to load the data to the registers controlling the corresponding analog switches of the threshold DAC, the pixel mask

circuit and the test signal circuit.
[1] V.Gromov, R.Kluit, H. van der Graaf, "Prototype of the Front-end Circuit for the GOSSIP (Gas On Slimmed Silicon Pixel) Chip in 0.13 μm CMOS Technology ", 12th Workshop on Electronics for LHC and Future Experiments, pp. 253-257, Valencia, Spain, 25-29 September 2007.

Poster session / 25

MAPS in 130 nm and 90 nm triple well CMOS technologies for HEP applications

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In this work deep N-well CMOS monolithic active pixel sensors (DNW-MAPS) are presented as an alternative approach to signal processing in high energy physics experiments. Based on different resolution constraints, some prototype MAPS, suitable for applications requiring different detector pitch, have been developed and fabricated in 90 nm and 130 nm triple well CMOS technologies. Experimental results from the characterization of the test structures with different features will be presented together with TCAD and Monte Carlo simulations intended to study the device substrate properties in terms of charge diffusion and charge sharing among pixels.

Summary:

Recently, monolithic active pixel sensors (MAPS) properties have been intensely investigated by several research teams involved in the development of detectors for particle physics experiments. Their monolithic structure, featuring a few μm thick superficial active volume, makes them interesting for applications to experiments at the future high luminosity colliders. In particular, deep N-well (DNW) MAPS make use of a buried N-type layer, available in modern triple-well deep submicron CMOS processes, as the charge collecting electrode and, instead of the classical three transistor readout scheme, employes a charge sensitive amplifier to perform signal amplification. The use of a DNW as the collecting electrode makes it possible to layout all of the N-channel transistors belonging to the front-end electronics over the sensor area, therefore reducing the impact of the electronics itself on the detector fill factor. In order to fully exploit the potential of complementary MOSFET processes and include also PMOS transistors (which need to be integrated in standard N-wells) in the design of the pixel level electronics, the sensitive element has to take up a significant fraction of the elementary cell surface. The above described approach results in an increased functional density which may be exploited to add a filtering stage and some simple logic blocks to the charge preamplifier. These guidelines have been followed in the design of different prototype chips fabricated in 90 nm and 130 nm epitaxial, triple well CMOS processes provided by STMicroelectronics. A set of test chips, called Apsel (active pixel sensor electronics) and including single pixel structures and MAPS matrices, has been designed both in 130 nm and 90 nm CMOS technologies. Pixel-level front-end electronics in the Apsel2 family chips takes advantage of a typical readout channel for capacitive detectors including a charge preamplifier and a shaping stage and is suitable for the design of detectors with a pitch in the 50 μm range. A different readout topology, lacking the shaper, has been integrated in the SDR0 prototype chip which includes single pixel structures, an 8X8 matrix and a 16X16 pixel matrix featuring sparsified data readout and a 25 μm pitch. Noise and charge sensitivity properties of the front-end electronics

will be measured by means of charge injection in some dedicated structures. Functionality tests of the sparsified digital readout architecture will be carried out in the SDR0 chip. A laser source will be used for the experimental characterization of the device properties in terms of charge diffusion in the substrate, charge collection and charge sharing among the pixels. Such results will be compared to results from the simulations performed with ISE-TCAD tools by Synopsys and with Monte Carlo techniques specifically developed to simulate random walk of minority carriers in an undepleted detector substrate.

Parallel session B5 - ASICs 2 ILC / 26

MAROC: Multi Anode Readout Chip

Author: Sylvie BLIN[1]

Co-authors: Christophe DE LA TAILLE [1]; Gisèle MARTIN-CHASSARD [1]; Nathalie SEGUIN-MOREAU [1]; Patrick PUZO [1]; Pierre BARRILLON [1]

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MAROC is the readout chip designed for the ATLAS luminometer made of Roman pots. This ASIC has been realised in SiGe 0.35µm technology and is an evolution of the OPERA_ROC ASIC developed and installed on the OPERA experiment to auto-trigger and readout 64 channels Hamamatsu multi anode PMTs.
Its main features are a 100% trigger rate for signal greater than 1/3 photoelectron, a charge measurement up to 30 photoelectrons with a linearity of 2% or better and a crosstalk less than 1%. A 12-bit Wilkinson ADC has been embedded to digitalise charge measurement.
In order to check the functionalities of MAROC, laboratory tests have been performed and have showed a good global behaviour of the chip, which allows using it for beam tests of a complete Roman Pot at CERN during autumn 2007.

Poster session / 27

Digital part of SiPM Integrated Read Out Chip ASIC for ILC hadronic calorimeter

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Co-authors: Christophe DE LA TAILLE [1]; Gisele MARTIN CHASSARD [1]; Julien FLEURY [1]; Ludovic RAUX [1]; Michel BOUCHEL [1]

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SPIROC (SiPM Integrated Read Out Chip) is the Very Front End ASIC that reads ILC hadronic calorimeter SiPM. It integrates a very complex digital part which performs many functions and manages Acquisition, A/D Conversion and data Read-out.

The Acquisition module manages Switched Capacitor Array in which charge and time are stored. This is done by an asynchronous module to meet time requirements. This part manages 36 channels with a depth of 16 for each.
The conversion step permits to convert analogue data into digital data by driving an integrated Wilkinson ADC. Data are stored into an integrated 4K bytes memory.
The read out step handles the communication between chips and sendout of data. ASIC are daisy chained to minimize lines between boards.

Parallel session B4 - ASICs 1 FE chips / **28**

Steering and Readout Chips for DEPFET Sensor Matrices

Authors: Ivan Peric[1]; Peter Fischer[1]

Co-authors: Christian Kreidl [1]; Florian Giesen [1]

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The ASICs required to operate DEPFET matrices - a fast analog switch and a drain current readout chip - are presented.

Summary:

DEPFET Pixel sensor matrices consist of regular arrangements of DEPFETs. They are read out sequentially by enabling individual gate rows so that the currents in the drain columns reflect the pixel charge. Specialized chips are required to apply voltage steps of up to 10V to gate- and clear rows. The radiation tolerant switcher3 chip has been developed for that purpose. It contains 128 channels, a flexible sequencer and relies on bump bonding. A prototype for the latest drain readout architecture is also presented.

Poster session / **29**

SPIROC (SiPM Integrated Read Out Chip): Dedicated very front-end electronics for an ILC prototype hadronic calorimeter with SiPM readout.

Author: Ludovic Raux[1]

Co-authors: Christophe de La Taille [1]; Frédéric Dulucq [1]; Gisèle Martin-Chassard [1]; Julien Fleury [1]; Michel Bouchel [1]

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SPIROC is a dedicated very front-end electronics for an ILC prototype hadronic calorimeter with SiPM readout. It has been realized in 0.35m SiGe technology. It has been developed to match the requirements of large dynamic range, low noise, low consumption, high precision and large number of readout channels needed.

SPIROC is an auto-triggered, bi-gain, 36-channel ASIC which allows to measure on each channel the charge from one photoelectron to 2000 and the time with a 100ps accurate TDC.
An analog memory array with a depth of 16 for each is used to store the time information and the charge measurement. A 12-bit Wilkinson ADC has been embedded to digitize the analog memory contents (time and charge on 2 gains). The data are then stored in a 4kbytes RAM. A very complex digital part has been integrated to manage all theses features and to transfer the data to the DAQ.

Parallel session B5 - ASICs 2 ILC / **30**

HARDROC, HAdronic Rpc Detector ReadOut Chip

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Co-authors: Christophe de LA TAILLE [1]; Clement JAUFFRET [2]; Gisele MARTIN-CHASSARD [1]; Herve MATHEZ [3]; Imad LAKTINEH [3]; Jean-Claude BRIENT [2]; Michel BOUCHEL [1]; Renaud GAGLIONE [3]

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HARDROC is a complete readout chip in SiGe 0.35µm of the RPCs or GEMs foreseen for a Digital HAdronic CALorimeter (DHCAL) at the ILC. The ASIC integrates 64 channels of
• fast low impedance preamplifier with 6bits variable gain (tunable between 0 and 4)
• variable shaper (50-150ns) and Track and Hold to provide a multiplexed analog charge output up to 10pC.
• variable gain fast shaper (15ns) followed by two low offset discriminators to autotrigg down to10 fC. The thresholds are loaded by two internal 10 bit- DACs.
• A 128 deep digital memory to store the 2*64 discriminator outputs and bunch crossing identification coded over 24 bits counter.
The design and measured performance of the chip will be presented.

Parallel session B7 - Systems, Installation and Commissioning 7 / 31

Electronic developments for HADES RPC wall: overview and progress

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This contribution presents the actual status and progress of the electronics developed for the Resistive Plate Chamber detector of HADES. This new detector for the Time of Flight detection system will contain 1000 RPC modules, covering a total active area of around 7 m2. The Front-End electronics consist of custom-made boards that exploit the benefit of the use of commercial components to achieve time resolutions below 100ps. The readout electronics, also custom-made, is a multipurpose board providing a 128-channel Time to Digital Converter (TDC) based on the HPTDC chip.

Summary:

New advances on RPCs (Resistive Plate Chambers) show that only since a few years ago it is possible to use RPCs for precise time of flight measurements at normal conditions of pressure and temperature with inexpensive materials. These detectors are becoming widely used because their excellent TOF capabilities and reduced cost, facing in some applications the well assessed technology of plastic scintillators. The RPC detectors that will be installed in the low angle region of HADES (High Acceptance DiElecton Spectrometer) are used for both, particle identification and triggering. 1024 double-sided readout detectors will be distributed in an active area of about 7 squared-meters, distributed in 6 sectors, covering a polar angle between 18 and 85 deg. with 2pi azimuthal acceptance.

The electronic systems involved in the RPC system are: the Front-End that digitizes the signals from the RPC cells, the Readout that label and pack the digital signals from the Front-End and the power supply and slow-control system. All of them are based on custom-made boards.

The Front-End electronics of the HADES RPC consists of two different boards. The Daughterboard provides the specific signal processing for timing and charge measurement. This digital conversion converts the fast analog RPC signals into time-window signals where the rising edge provides information about the timing and the width codifies the charge. The digitized signals are converted to LVDS and transmitted through the Motherboard which also provides stable supply voltages and programmable threshold DACs for the discriminators.

A general-purpose trigger and readout board with on-board DAQ functionality is currently being developed. Its primary application was to be a 128-channel Time to Digital Converter (TDC) electronics based on the HPTDC (achieving 40 ps resolution) to read out the HADES RPC detector, but the new version has been designed in a way to be detector independent and thus may serve for any high speed data acquisition by using a flexible add-on board concept.

Custom power supply boards provide the required voltages to the Front-End electronics: +5V, -5V and +3.3V. This power supply boards are based on commercial switching DC/DC modules that have been conveniently filtered (common and differential modes) to obtain clean power supply voltages. This supply boards will also contain sensing capabilities to implement the low voltage monitoring system, based on Linux computers-on-chip that runs Epics in a distributed system over the Ethernet.

HADES is currently installed at GSI Darmstadt (Germany), and has as main goal the detection of electron pairs produced in relativistic pion-nucleus and nucleus-nucleus collisions, with high invariant-mass resolution and high acceptance, to obtain information about the modification of the properties of vector mesons in nuclear matter, both normal and hot and compressed. HADES consists of several sub-detectors providing triggering, and particle identification and discrimination capabilities. Among these sub-detectors the RPC detectors covers the TOF system at low angles, where the particle rate where particle rates reach their maxima, whereas plastic scintillator rods read by photo-multiplier tubes are set up for large angles. The new RPC detector will increase the granularity and time resolution to levels that will allow extending the range of possible collisions in HADES from C-C to Au-Au.

Parallel session A1 - Systems, Installation and Commissioning 1 (DAQ, DCS, Cal) / 32

New DAQ and Digitizing systems of CMD-3 Detector.

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The CMD-3 Cryogenic Magnet Detector for VEPP-2000 Collider is under construction now. This paper describes hardware part of new DAQ system. The unique features of this system is low EMI, low power and high speed. This is serial-backplane LVDS – media based system. The DAQ system is easy scalable and low-cost due to output to commercially available Fast Ethernet. Special attention is devoted to how DAQ interact with Trigger and Digitizing subsystems. As example the "T2Q" Readout and Signal Processing Board for Drift Chamber of CMD-3 detector are presented. This Board includes 16 wire processing channels which performs double-end wire readout for charge division measurements and time measurement. Each wire processing channel supplied with a micro-trigger

to operate in Common-Stop CMD-3 Trigger environment. The unique features of this Board are very high dynamic range to ensure good dEdx and high accuracy time measurement. Low size and low power consumptions are achieved utilizing commercially available components only. It is shown specially designed low EMI high-speed serial backplane DAQ has virtually no pick-ups and allows on-board preamplifier and on-board ground decoupling.

Summary:

Modern Academic Research activity requires DAQ that combine high speed of data with high density of hardware. Also it will be cost-effective, easy scalable and low EMI. The DAQ system described is satisfactory approach of that task. Since it is built with commercially available components only it is cost-effective for small and medium size systems. Using of LVDS transceivers allows small power consumption and good EMI compatibility. In order to communicate with DAQ and Trigger each Digitizing Board are equipped with programmable First Level Trigger Preprocessor and DAQ Preprocessor. Current status is finishing of production.

Poster session / 34

FPGA based Readout Logic of the Front-end Electronics of the Absolute Luminosity Monitor

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Readout of the front-end electronics of the Absolute Luminosity Monitor is controlled by programmable devices. AlfaR is a local readout controller which reads digitized data with LHC clock and keeps them until validation of the first level trigger. Once validated, data are moved via serial bus to further part of the readout chain supervised by AlfaM chip. This global readout controller manages 23 AlfaR devices and provides a platform for communication with a higher level system. For each accepted event, a block of data from all 23 AlraR controllers is sent from AlfaM over serial optical link.

There are 8 such readout systems in whole Absolute Luminosity Monitor.

Summary:

The Absolute Luminosity Monitor consists of 8 Roman Pots, each of them containing identical readout architecture. A single Roman Pot consists of a 5 x 5 matrix of small structures called PMF.

Each PMF hosts 64 channel Maroc front-end chip and associated with it AlfaR local readout controller. The latter one provides storage resources, a data management and a serial communication interface between local and global systems.

At each LHC clock, 64 bit wide data are made available on the output of Maroc. Such data word is stored in 64 bit wide internal pipeline storage of AlfaR along 40 MHz LHC clock. Before being written, each bit of the input data word is ANDed with respective bit of a mask register to allow for disabling of faulty input channels. Depth of the pipeline is parameterized to allow for tuning of the trigger latency to up to 256 clock cycles.

Each word is kept in the pipeline until is rejected or accepted by the first level trigger. Upon decision, data are dropped or moved to another storage buffer - an output derandomizer. To allow for checking of data alignment across local readout systems, subset of the local bunch crossing and event counters' states

are added to the accepted event data. This way, each data word written to the derandomizer is extended to 71 bits.

The depth of the derandomizer is fixed and equals to 256 slots – sufficiently enough to accommodate expected number of back-to-back positive decisions of the first level trigger.

Event from the derandomizer is requested by the readout supervising chip AlfaM as soon as a positive trigger decision is received. The corresponding data word from the derandomizer is then serialized and sent to AlfaM via a dedicated copper link.

AlfaM – the global readout controlled - is located on the motherboard card, having connection to the global system as well as to 23 AlfaR chips belonging to the PMF of a single Roman Pot. Once requested, the data transfers from all underlying AlfaR controllers take place in the same time along centrally distributed 40 MHz clock. After a fixed time interval, all data words from AlfaR chips are de-serialized internally in input registers of AlfaM. Then subsequently they are multiplexed and moved to the output data link buffer to form a data block of particular event. Such block is sent over the gigabit optical output link as soon as the link is free. Length of the message is fixed and for each event it is ~2 Kbits.

Only when all input registers have been multiplexed and moved the output buffer, AlfaM can request a new event data from the AlfaR controllers. Thus, in order to make sure that none of back-to-back positive decisions of the first level trigger is lost, they are buffered in the trigger FIFO of AlfaM. The depth of this buffer is set to 256 slots – to match the depth of the derandomizing buffers in the AlfaR controllers.

Apart from supervising the data flow, AlfaM provides a base for communication between underlying AlfaR chips and the global system. Such communication is realized using a simple SPI interface ran from the global system through ELMB controller. This way one can read or write internal registers of AlfaM, AlraR or Maroc chips or control operability of this system.

Parallel session A5 - Systems, Installation and Commissioning 3 (TK and Pix, Lumi) / 35

System Design of the ATLAS Absolute Luminosity Monitor

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Co-authors: Bjorn Lundberg [2]; francis anghinolfi [1]; sebastien franz [1]; wieslaw iwanski [1]

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The ATLAS absolute luminosity monitor is composed of 8 roman pots symmetrically located in the LHC tunnel. Each pot contains 23 multi anode photomultiplier tubes, and each one of those is fitted with a front-end assembly called PMF. A PMF provides the high voltage biasing of the tube, the front-end chip and the local readout controller in a very compact arrangement. The 23 PMFs contained in one roman pot are connected to a motherboard used as an interface to the back-end electronics. The system allows to configure the front-end electronics from the ATLAS detector control system and to transmit the luminosity data over optical link.

Summary:

Introduction.

The ATLAS detector will be provided with an absolute luminosity monitor composed of eight roman pots symmetrically located in the LHC tunnel at 240 meters from the interaction point. Each of these pots houses a scintillating fiber tracker (ALFA) whose light is detected by 23 multi anode photomultiplier tubes. Each MAPMT is coupled to a front-end assembly (PMF).

Front-end assembly.

Each MAPMT is biased by a high voltage divider board that is plugged straight on the tube high voltage pins using pin feed through contacts. The matrix of 64 signal pins of the tube passes through the high voltage board and reaches an adaptor board underneath, where it is then redistributed on edge connectors. This arrangement allows to plug a third board underneath the adaptor, that holds the front-end ASIC (MAROC) used to preamplify and to discriminate the pulses. The MAROC chip is directly bonded to the board and it is directly coupled to the readout FPGA that faces the ASIC on the back side of the board. This front-end assembly provides a very compact front-end block on the MAPMT area of 30 mm by 30 mm, in a total stack up of less than 40 mm (tube included). The blocks are arranged on a matrix of 5 by 5 slots provided with low voltage, high voltage and FPGA readout interfaces.

Motherboard and data link.

The PMF assemblies deliver each a serial data stream formatted by the front-end FPGA (ALFA-R). The data streams are driven at the LHC clock rate and are collected by a readout FPGA (ALFA-M) interface located on a motherboard. The 25 streams are bundled together to form a front-end packet that is transmitted to the back-end through an optical gigabit link. The link is implemented with a GOL ASIC configured in G-Link mode. The timing information is handled by a TTCrx chip on the motherboard; the system clock is stabilised with a QPLL.

The motherboard houses all the necessary low voltage radiation hard regulators that it needs and also that are needed by the PMFs.

The motherboard is equipped with a carefully designed reset logic chain that allows to handle the startup sequence during a cold startup, or when a local or a remote reset are requested. The status of the PMFs and of the motherboard circuitry is made available in the form of a status word that can be read asynchrounously by the configuration and control system.

Configuration and Control.

The motherboard and the PMFs are controlled by an independent link built with a standard ELMB. The ELMB is self powered from the back end and it allows to drive remote reset signals to the various motherboard circuits. The embedded SPI interface of the ELMB is used to communicate with the motherboard and with the PMF logic circuits. Because the SPI interface is driven at a clock rate controlled by the ELMB, the status of all the system can be monitored in all circunstances, and in particular when the GOL or TTC links are down. The SPI interface allows also to download the configuration data of the MAROC chips on the PMFs at the CANBus speed.

Parallel session A6 - Systems, Installation and Commissioning 4 (Lumi, MU) / 36

CMS DT Chambers Read-Out Electronics

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Being close to completion of CMS installation, the three levels of the final read-out system of the Drift Tube (DT) chambers is presented. Firstly, the Read Out Boards (ROB), responsible for time digitalization of the signals generated by a charged particle track. Secondly, the Read Out Server (ROS) boards receive data from 25 ROB channels through a 240 Mbps copper link and perform data merging for further transmission through a 800 Mbps optical link.
Finally, the Detector Dependent Unit (DDU) merge data from 12 ROS to build an event fragment and send it to the global CMS DAQ through a S-LINK64 output at 320 MB/s. DDU also receives synchronization commands from the TTC system (Timing, Trigger and Control), perform errors detection on data and send a fast feedback to the TTS (Trigger Throttling System).
Functionality of these electronics has been validated in laboratory and in several test-beams, including the Magnet Test and Cosmic Challenge exercise that demonstrated proper operation and integration within the final CMS framework.

Summary:

The CMS (Compact Muon Solenoid) detector is one of the four large experiments that will be installed in the new accelerator LHC (Large Hadron Collider) that is being built at CERN. A key point of CMS is its ability to trigger on and reconstruct muon tracks at high luminosities, as this will allow deeper exploring into matter, probing the Higgs mechanisms and other aspects of the Standard Model [1]. This task is performed by the various CMS sub detectors, among them, the Drift Tube chambers (DT), that provide muon identification and precise momentum measurement.

The read-out electronics of the CMS DT chambers is designed to perform time digitization of the signals generated by charged particle tracks and to do further data merging in order to achieve a read-out of the full detector (172,200 channels) at a Level 1 trigger rate of 100 kHz. The system is divided in three levels. First, the 1500 ROB (Read-Out Boards), placed inside the so-called Minicrates [2] attached to the DT chambers. Second, 60 ROS (Read-Out Server) boards located inside the CMS cavern in the balconies on both sides of the CMS wheels. And finally, 5 DDU (Detector Dependend Unit) boards which will operate in the underground counting room.

ROBs are built around an HPTDC (High Performance Time to Digital Converter) [3] ASIC developed by the CERN/EP MIC group. Inside each ROB, four HPTDC´s are connected in a token ring scheme for digitization of up to 128 chamber channels with a time resolution of 781 ps and further data transmission to the ROS through a 240 Mbps serial copper link.

ROS boards perform a data merging of 25 input ROB channels, reducing data overhead to achieve ~ 8 kbytes per event in the whole detector. Data is serialized and transmitted to the DDU through an optical link at 800 Mbps. ROS boards also perform main tasks of data quality monitoring and event synchronization.

Each DDU merges data from 12 ROS in order to build an event fragment at the Level 1 trigger rate (up to 100 kHz) and send it to the global CMS DAQ through an S-LINK64 [4] output at 320 MB/s. One of the main tasks of the DDU is keeping synchronization with the whole detector. In order to do this, the DDU receives synchronization commands from the TTC system (Timing, Trigger and Control [5]), performs errors detection on data and sends a fast feedback to the trigger system through the TTS output (Trigger Throttling System [6]) to slow down the trigger rate or stop data acquisition in case of failures. In total the 5 DDU boards can manage event sizes up to ~15 kbytes, at the trigger rate of 100 kHz, about the double of requirements.

In summary, the chosen architecture, as well as the dimension of the memories, links bandwidths, pooling mechanisms, failure detection circuitry, etc, fulfils the experiment requirements of trigger and data rate, radiation tolerance, limited supervision and power consumption.

The complete functionality of these electronics has been validated in laboratory and in several test-beams [7]. Moreover, Magnet Test and Cosmic Challenge exercise, has demonstrated full operation of the readout chain and integration within the final CMS framework. Right now, the read-out system is being installed and commissioned for CMS start up by fall 2007.

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Poster session / **37**

Proposal, development and test of an analog front-end electronic board for the Nemo telescope.

Author: Filippo Maria Giorgi[1]

Co-authors: Alessandro Gabrielli [1]; Domenico Lo Presti [2]; Enzo Gandolfi [1]; Luigi Caponetto [3]; Nunzio Randazzo [3]

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Development, realization and test of an electronic data acquisition-board for the NEMO (NEutrino Mediterranean Observatory) collaboration are described in this work. The collaboration is involved in R&D for the construction of a deep underwater km^3 scale Cherenkov neutrino telescope in the Mediterranean sea. Thousands of optical modules are equipped with a photo multiplier tube and an electronic circuit for data acquisition and transmission. This work shows a possible solution for the front-end board compatible with an analog sampling chip; this data acquisition system has been developed to be fully compliant with the data transmission system of the Nemo Phase-1 apparatus.

Summary:

The data acquisition board described in this work is a prototypal front-end for the Cerenkov neutrino telescope Nemo. The detector involves thousands of Optical Modules (hereafter OM) spread over a volume of 1 Km^3 and supported by a three-dimensional structure. Each OM is equipped by a photo multiplier tube (PMT) for Cerenkov light detection and an electronic circuit for data acquisition and transmission (DAQ-Board). The proposed structure of the detector is made up of a 9x9 towers grid; a tower is a mechanical support made of 18 superimposed floors hosting 4 OMs each. The spacing between the towers and the width of the floors will grant the coverage of the entire one Km^3 volume. The Italian proposed site for the telescope is the southern Ionian Sea near the coast of Capo Passero, Sicily.

Nowadays a test apparatus called Nemo Phase-1 is running. This structure involves a single tower made up of 4 floors only and it has been deployed few kilometers away from the coast of Catania.
The data acquisition board proposed works with a full custom ASIC called LIRA (acronym from the Italian for "Analog Delay Line"), used for the PMT waveform analog sampling. The aim of this project is to develop a front-end board integrating the analog sampling technology over the present data transmission system; even the layout of the board meets the mechanical constraints imposed by the Phase-1 OM specifications. The main components of the proposed solution are: the chip for the analog sampling, a pipelined ADC for samples conversion at 20 MHz, and a programmable logic device for the acquisition process control and data transmission to a floor data-concentrator (Floor Control Module).
The low power analog sampler supports rates up to 200MS/s and embeds an over-threshold trigger and signal classifier. This chip, in normal operating condition, consumes 150 mW for a 50 KHz event rate. The sampler stores each photo-electron signal into two parallel FIFOs, one acquiring the PMT anode and the other acquiring the last dynode signal to grant a higher dynamic extension. Once the sampler FIFO is full, data can be read and converted at 20MHz by the pipelined ADC. The real time classification of the signal permits to choose properly the analog channel that should be digitized: a high dynamic pulse will be read from the low-gain dynode channel; on the opposite, a low signal will be read from the anodic FIFO sampler. Digital samples are then temporarily stored inside an FPGA: a programmable digital logic device responsible for controlling the sampling process, transferring data and executing remote commands.
The board has then been tested simulating a PMT signal with an arbitrary function generator and acquiring the sampled digital waveform on a PC using a logic state analyzer. The firmware for the interface towards the FCM has been simulated on a PC while the hardware line transceivers have been tested on board to inspect signal integrity. Nowadays we are setting up a more exhaustive test bench on the actual data acquisition system.

Parallel session A1 - Systems, Installation and Commissioning 1 (DAQ, DCS, Cal) / 38

Implementation and performance of the Detector Control System for the electromagnetic calorimeter of the CMS experiment

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In this presentation we describe the main design objectives, the detailed specifications and the final layout of the Detector Control System (DCS) for the electromagnetic calorimeter (ECAL) of the CMS experiment. Emphasis is put on the system implementation and specific hardware and software solutions in each of its sub-systems. The latest results from the tests of final prototypes of these subsystems during the 2006 ECAL test-beam programme, as well as the installation and commissioning of the whole DCS at the CMS experimental construction site are also discussed.

Poster session / 39

A complete set of firmware for the TileCal Read-Out Driver.

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TileCal is the hadronic tile calorimeter of the ATLAS experiment at LHC/CERN. The Read-Out Driver (ROD) is the main component of the TileCal back-end electronics. The ROD is a VME 64x 9u board with multiple programmable devices which requires a complete set of firmware. This paper describes the firmware and functionalities of all these programmable devices, especially the DSP Processing Units daughterboards where the data processing takes place. Finally, some results obtained during the TileCal commissioning phase are presented.

Summary:

TileCal is the hadronic tile calorimeter of the ATLAS experiment at LHC/CERN. The central element of the back-end system of the TileCal detector is the Read-Out Driver (ROD). The TileCal ROD motherboard based on a common design for ATLAS calorimeters and it includes multiple programmable devices and two Processing Units daughterboards. These devices are programmed with a complete set of firmware code which is, in some cases, also common for both ATLAS calorimeters RODs. Both, the common and the TileCal specific firmware are described in this paper emphasizing on the Processing Units reconstruction algorithms.
The input data coming from front-end is received in the ROD through 8 Optical Receivers and transmitted to 4 Field Programmable Gate Arrays (FPGAs) (called StagingFPGAs). The StagingFPGA is the ROD input data distributor and transmits the received data to the Processing Units daughterboards. Two InputFPGAs receive, check and transmit the data in the PU towards two Digital Signal Processors (DSPs).The DSPs are the main component of the ROD since they are responsible for data reconstruction in real time at the ATLAS first level trigger rate. Besides, the DSP code also includes Timing, Trigger and Control (TTC) synchronization, Muon Tagging and Missing Et algorithms, histogramming, and real time behaviour information. In addition, the Output FPGA implements the interface between the PU and the VME bus and TTC system. The DSPs process and send the data to the ROD motherboard Output Controller FPGA (OC_FPGA). Finally, the OC_FPGA is the output data distributor and is responsible of data transmission to the Read-Out System (ROS) through the Transition Module (TM).
Two more FPGAs provide the interface with the VME bus (VME_FPGA) and with the TTC system (TTC_FPGA). Besides, some extra functionalities and recent firmware upgrades are also presented in this paper. Finally, some results obtained during the TileCal commissioning phase are also presented. During this phase the basic firmware and the recent upgrades are being tested as well as the DSP reconstruction algorithms.

Poster session / 40

Proposal of a readout technique for low-pitch pixel devices

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The up-to-date pixel detectors applied to HEP in LHC experiments implement 2D matrixes of sensitive elements that are basically readout via token-based techniques, according to external trigger signals. As the readout time is one of the drawbacks of large matrix devices, because it implies long detector dead times, here it is described a novel readout architecture of pixel devices, which exploits the features of deep-submicron CMOS technologies and should be considered for low-pitch pixel devices. This allows for future applications not only on general pixel detectors but also on trackers and trigger systems, wherever an on-chip data reduction/sparsification is considered.

Summary:

The readout electronics exploited for to-date pixel detectors mainly implement token-based techniques to readout the hits. The number of pixels per chip of the LHC experiments is of the order of some thousands. These pixels are designed with bidimensional rectangular matrixes and arranged in rows and columns. It can be affirmed that the more is the number of pixels, the longer is the dead time because the longer is the readout phase. In fact, the more is the number of wires routed among the rows and the columns of the matrix in the chip layout, the larger is the pixel's pitch. This latter plays a significant role in the spatial resolution of the pixel detector. As the number of wires used by the readout architecture specifies how the information of the hits is sent to the output, this number cannot be scaled under a given minimum threshold. This point has been in-depth investigated and simulated and the paper presents a novel digital readout scheme to extract the time and position information of the hits, wherever they are spread out over the pixels' area, via a non-token based technique. This solution may be implemented in hardware by exploiting the up-to-date CAD tools to project digital circuits and, in conjunction with the full-custom design of the sensitive pixel cells, it may lead to the production of mixed-mode ASICS with fast readout logic. The idea is to not use point-to-point wires from the border of the matrix to the single pixels or groups of pixels at all. All the pixels are driven via global wired-or nets and are readout via other row wires shared over the whole matrix. This work aims at simplifying the internal routing of pixels and moves outside the matrix, on the digital readout part, the sparsification logic. This leads to a matrix wire-density and to a pixel's pitch independent to the number of pixels and allows for future bigger detectors with respect to those recently used. As the pixels do not own internal registers and there are no dedicated wires to freeze single pixels, to avoid data overlap of adjacent bunches the hits are frozen and set free, column by column (or row by row), at any read clock cycle. Let's give a brief functional description. At a given time, for example when a bunch-crossing signal is given, the columns that own at least one hit are seen via wired-or nets and frozen. The coordinates of these columns are associated with a time-stamp, whose buffers are located outside the matrix. Then, one at a time, the columns are enabled and the pixels' out write the horizontal bus. In one period a full column of pixels is readout and set free. Then the process moves to another column. The proposed approach could match the requirements of future low-pitch pixel detectors that need robust on-chip digital sparsification and that may be also used in first level triggers on tracks in vertex detectors.

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Design of on-chip data sparsification for a mixed-mode MAPS device

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The device described in the paper is built up of a bidimensional matrix of MAPS, already designed and fabricated in the past by the SLIM5 Collaboration, and of an off-pixel digital readout sparsification. The readout logic is based on std-cells and implements an optimised token-like technique. It is aimed at overcoming the readout speed limit of future large-matrix pixel detectors for particle tracking, by matching the requirements of future HEP experiments. In particular, the readout architecture extends the flexibility of the MAPS devices to be also used in first level triggers on tracks in vertex detectors.

Summary:

The paper describes the design of a mixed-mode ASIC that implements a matrix of MAPS cells along with a digital readout sparsification circuit. The design has been carried out within the SLIM5 Collaboration and it is aimed at overcoming the readout speed limit of future large-matrix pixel detectors for particle tracking, by matching the requirements of future HEP experiments. In particular, the readout architecture extends the flexibility of the MAPS devices to be also used in first level triggers on tracks in vertex detectors. The MAPS cells have been fabricated and tested in the past years with different layout flavours and now this ASIC includes readout capabilities. Plus, the mixed-mode design approach extends the performance of the chip as both the matrix and the readout logic have been developed separately and, lately, integrated together. In particular the matrix of MAPS has been described with a VHDL-Verilog model and used as a macro-cell block within a bigger digital design. The global place-and-route has been also digitally designed. The design is implemented via the STM 0.13mm CMOS digital technology. Let's give a brief functional description of the readout logic. The matrix of pixels is grouped into regions of 16 pixels (macro-pixels). Each region is activated and frozen via dedicated wires while the reset and readout phases are carried out via wires that are shared over the whole matrix. The dedicated wires may also be masked, one by one, in case they would be too noisy or burned, to avoid reading not-significant hits at any readout phase. At a given time, for example when a bunch-crossing signal is provided, the columns of macro-pixels that own at least one hit are seen via fast-or wires and frozen. The coordinates of these columns are associated with a time-stamp, whose buffers are located outside the matrix. Then, one at a time, the columns are enabled and the macro-pixels' output data are written on a readout bus. Once the column of pixels has been readout it is set free. Then the process moves to another column. The readout phase involves one column of macro-pixels at a time and this leaves the rest of the matrix free and capable of detecting new hits. Thus, the matrix may own hits, along with their personal time-stamps, belonging to different bunch-crossings. During the readout phase the matrix is swept and all the hits belonging to a given bunch are readout, reset and set free. The process continues till all the macro-pixels have been readout. All these capabilities have been designed into a single die composed of a large full-custom matrix of pixels that is readout via a standard-cell based digital circuit.

Poster session / **42**

Calibration and performance tests of the Very-Front-End electronics for the CMS electromagnetic calorimeter

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The Very-Front-End electronics processing signal from photodetectors of the CMS electromagnetic calorimeter, have been put through extensive test program to guarantee functionality and reliability. The final characteristics of the VFE boards designed for the calorimeter barrel and endcaps are resented. The results, which have been also verified during test beam at CERN, confirm the high quality of the boards production and show that the CMS detector specifications are reached.

Summary:

On detector electronics of the CMS electromagnetic calorimeter (ECAL), which consist of 75,848 radiation hard scintillating crystals PbWO4, contain almost 16,000 Very-Front-End (VFE) boards that process signals from Avalanche Photodiodes (APDs) in the central barrel region and Vacuum Phototriodes (VPTs) in the forward endcaps regions, respectively. The VFE board was designed in two types: covering a dynamic range up to 50 pC corresponding to incident particle energy of ~1.7 TeV for barrel and 16 pC for energy up to ~3 TeV for the endcaps. Both types comprises five identical and independent read-out channels. Each channel, processing the signal from one crystal, consists of a Multi-Gain Pre-Amplifier (MGPA), a multi-channel ADC, and two level adapters LVDS-RX. The MGPA contains a pre-amplifier and three parallel gain stages with nominal gains 1, 6, and 12 that shape and amplify the photodetector signal. The three analogue output signals of the MGPA are then digitized in parallel by the multi-channel 40 MHz 12-bit ADC (AD41240). An ADC internal logic determines whether a gain is saturated and then outputs the data from the highest non-saturated channel. In addition, the barrel VFE board also incorporates a Detector Control Unit (DCU) chip for measuring the APD leakage current and the crystal temperature.

All the VFE boards have to pass an extensive quality and assurance program to guarantee their functionality and reliability. The program includes an optical inspection by the manufacturer, a power-on test - the first electrical test that measures voltages, currents and performs a functional test, a burn-in for 72 hours at a temperature of 60℃, which is followed by a complete calibration and characterization of each channel. The calibration procedure covers an absolute calibration of each channel for the three gain stages in ADC counts per pC, channel-to-channel relative calibration, and gain ratios and linearity studies. Moreover, other relevant tests, such as a simulation of leakage current of the APDs, a test of temperature read-out channel on its complete dynamic range are also performed. Results are registered in a database and are used for a first intercalibration of the ECAL. To date, the test program for all the 12,800 barrel and the ~3,000 endcap VFE boards has been completed. The dispersion in the gains is found to be small (~ 1%) complying with the CMS detector specifications. Only around 2% of them failed the test criteria and have been rejected, the rest have been assembled into barrel supermodules and endcap supercrystals. The results obtained during the Q&A program have been verified in summers 2006 and 2007, when several fully equipped supermodules and supercrystals were tested and calibrated with high energy electrons.

Poster session / **43**

Optimization of amplifiers for MAPS

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High precision particle tracking and imaging applications require position sensitive detectors with high granularity, good radiation tolerance, low material budget, fast read-out and low power dissipation. Monolithic Active Pixel Sensors (MAPS) fabricated in a standard microelectronic technology provide an attractive solution for these demanding applications. The signal-to-noise ratio of MAPS can be increased by using in-pixel amplifiers. The compromise between speed, noise, gain and power consumption has to be achieved in the design of the amplifier. The charge collection efficiency and total capacitance at the amplifier input is influenced by the size of charge collecting diode. Therefore, in order to achieve better MAPS performances, both the geometry of the charge collecting diode and the amplifier design

have to be considered in the optimization process.
In this work different amplifier designs and geometries of the charge collecting diode are proposed. The characterization measurements of the amplifiers fabricated in AMS 0.35 um OPTO technology will be presented. The electronic properties of the amplifiers calculated with Spectre circuit simulator and the charge collection efficiency simulated with ISE-TCAD package will be compared with the measurements. The advantages and drawbacks of the implemented designs will be discussed.

Parallel session A6 - Systems, Installation and Commissioning 4 (Lumi, MU) / 44

The 1st Result of Global Commissioning of the ATLAS Endcap Muon Trigger System in ATLAS Cavern

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We will report on the ATLAS commissioning run from the view point of the Thin Gap Chamber (TGC), which is the ATLAS end cap muon trigger detector. So far, a half of TGC chambers with on-detector electronics have been already installed to the ATLAS cavern. To integrate all sub-detectors before the physics run starting from early 2008, the global commissioning run together with other sub-detectors has been performed from June 2007. We have evaluated the performance of the complete trigger chain of the TGC electronics and provide the trigger signal using cosmic-ray to the sub-systems in the global run environment.

Summary:

Before starting a physics run from early 2008, all sub-detectors including their front-end electronics should be installed and tested synthetically in-situ.
The thin gap chamber (TGC) is used for the muon-endcap trigger system. The muon-endcap system covers the both endcaps of the detector (1.05<abs(eta)<2.4) to detect isolated muons and give the level-1 muon trigger signal with two ranges of the transverse momentum (pt) of low-pt > 6 GeV/c and high-pt > 20 GeV/c.
As at least three measurement points per track is necessary to identify a muon with even such coarse momentum estimation, there are three TGC wheels per endcap (one has three layers with triplet chambers, and the other two wheels have two layers each with doublet chambers).
Each wheel has the radius of about 10 meter, for example pivot doublet wheel has the radius of 11m, and due to this huge detector size, the number of channels become about 320,000 in total. Every wheel has commonly twelve sectors. This 1/12 sector is a construction unit for the trigger muon-endcap system for both the chambers and electronics. The sector is also the unit for the trigger and readout system.
The analog signals from the detector are fed into the ASD (Amplifier-Shaper-Discriminator) ASIC. There are three chains for the TGC electronics system. The first chain is the level-1 trigger decision logic. Candidate signals of more than 6GeV/c muon are selected by three modules (timing adjustment, bunch ID and coincidence ASICs). These modules are mounted on the sector. The muon candidates with more than 20GeV/c are classified by high-pt decision ASIC mounted nearby the sector.

The r-phi coincidence and the 6 classifications of pt information are performed by the FPGA mounted in the ATLAS counting room. The resulting trigger information is sent to the Muon Central Trigger Processor Interface (MUCTPI) in a standard format. The second chain is for the data readout. It consists of the pipeline buffers, derandomizers and parallel/serial converters ICs. The third chain is used for the initialization, monitoring and controlling of the modules. The functionality of all on-detector modules and their cablings has been inspected at the surface building before installing to the ATLAS cavern. So far, a half of TGC chambers with on-detector electronics have been already installed to the cavern.
In order to integrate all sub-detectors before the physics run starting from early 2008, the ATLAS commissioning run will be performed from June 2007. The main goal of the global commissioning run from the view point of Level-1 Endcap Muon Trigger System is to confirm the functionality of the complete chain of the TGC trigger electronics. Before the commissioning run, the trigger signal of the events with cosmic ray will be generated by using standalone TGC system itself, and then provided to the sub-systems during the ATLAS commissioning run.
The scope of this presentation is the result of the global commissioning run, especially from the viewpoint of TGC system.

Parallel session A6 - Systems, Installation and Commissioning 4 (Lumi, MU) / 45

CSC Data Acquisition System for CMS

Author: Jianhui Gu[1]

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Details of the Cathode Strip Chamber (CSC) Data Acquisition (DAQ) system for the CMS experiment at the LHC will be described. The CSC system is large, consisting of 218K cathode channels and 183K anode channels. This leads to a substantial data rate of ~1.5GByte/s at LHC design luminosity (1034cm-2s-1) and the CMS first level trigger (L1A) rate of 100KHz. The DAQ system consists of three parts. The first part is on-chamber Cathode Front End Boards (CFEB), which amplify, shape, store and digitize chamber cathode signals, and Anode Front End Boards (AFEB), which amplify, shape and discriminate chamber anode signals. The second part is the on-detector Data Acquisition Motherboards (DAQMB), which control the on-chamber electronics and the readout of the chamber. The third part is the off-detector DAQ interface boards, which perform real time error checking, electronics reset requests and data concentration. It passes the resulting data to a CSC local DAQ farm, as well as CMS main DAQ. All electronics in the system employ FPGAs allowing programmability. In addition, several high-speed serial interface technologies are employed.

Summary:

The Cathode Strip Chamber (CSC) system is one of the major components of the Compact Muon Solenoid (CMS) experiment at Large Hadron Collider (LHC) at CERN. The system is large, consisting of 468 chamber modules, forming eight disks to cover the three magnetic yoke iron stations at each end of the detector. Designed to work at high rates in a high magnetic field and moderate radiation field, the CSCs provide hit position precision measurements of accuracy ~100μm in the bending coordinate, and timing to better than a single beam crossing (25ns). The electronics system for the CSC is large, consisting of 218K cathode channels and 183K anode channels. The CSC DAQ system reads out data in response to CMS First Level Trigger (L1A) at an event rate of 100KHz. The data enters the CMS main DAQ system through an SLINK64 data path, which builds and filters the events, and writes the data to tape at an event rate of 100Hz.
The CSC DAQ system is naturally divided into three parts. The first part consists of the Cathode Front End Board (CFEB) and Anode Front End Board

(AFEB) mounted directly on the chambers. The second part is the Data Acquisition Motherboard (DAQMB) situated in VME crates (Peripheral Crates) on the periphery of the magnetic yoke iron. The third part is the Front End Driver (FED) crates and a CSC local DAQ farm situated in CMS counting rooms. The CSC DAQ system is asynchronous. Events are marked with L1A numbers. Custom parallel Cyclic Redundancy Check (CRC) is heavily used throughout the system to assure data integrity.

The CFEBs amplify, shape and digitize CSC chamber cathode charge signals. Each CFEB services 96 cathode strip channels. Five or four CFEBs are mounted on each chamber, with a total of 2268 boards in the system. A hit in the chamber produces induced charge on cathode strip that is amplified and shaped by BUCKEYE ASIC chips. The output voltage is sampled every 50 ns, and stored in a 96 cell/channel Switch Capacitor Array (SCA) ASIC chips. The chamber electronics is self-triggering. Voltages are stored in the capacitor and digitized only if the CFEB receives a local charge track trigger in coincidence with the L1A. The CFEB utilize commercial 12 bit ADCs. The resulting digital data from the 96 channels are multiplexed at 40MHz, and sent through Channel link via skew-clear cables (6 to 14.5 meters) to the DAQMB in the crates located on the iron disk periphery.

The Data Acquisition Mother Board (DAQMB) controls the on-chamber electronics and the readout of a single chamber. This includes collecting data from CFEB and AFEB, as well as the local CSC trigger information. The DAQMB also serves as the controller performing slow control, calibration, and CFEB monitoring. The DAQMB is built around seven FIFOs, which upon receipt of L1A, receive data from five CFEBs, one Trigger Mother Board (TMB), and one Anode Local Charge Track Board (ALCT). The DAQMB concentrates the data from the seven FIFO's, assigns header and trailer words containing error information, a CRC check, and a unique L1A number. The data is sent at 1.6Gbit/s using Texas Instruments TI2501 serializer through optical fibers to the FED crates in the counting room. Since each DAQMB services one chamber there are 468 DAQMB in the system.

The CSC Front End Driver (FED) electronics assembles the data from the 468 DAQMBs for transfer to CMS main DAQ via SLINK64. The FED also performs real time error checking, electronics reset requests and data concentration. Lastly, a fraction of the data is sent to a local computer farm for real time monitoring of the CSC system.

The four FED crates include 36 Detector Dependent Units (DDU) and 4 Data Concentrator Cards (DCC). Each crate contains a high speed custom designed backplane. Each DDU receives data from 13 DAQMBs that are channeled through Xilinx FPGA's RocketIO. Data from the 13 input fibers are concatenated with header and trailer words added. As the events are assembled, the DDU checks the data for hardware error flags, CRC words, DAQMB/CFEB status, and the L1A number and beam crossing number synchronization. In all, over 150 checks are made on each event received. Thus detector hardware problems can be recognized within 100μsec of their onset. The DDU outputs its data via FPGA RocketIO communication with two 3.1Gbit/s links on a custom backplane to a Data Concentrator Card (DCC). A fraction of the data is also sent via a custom designed gigabit Ethernet interface to the CSC local DAQ farm.

The main function for the DCC is to further concentrate the data. There is a single DCC in each of the four FED crates. Each DCC receives the data from 9 DDU in the crate through eighteen serial links with 3.1Gbit/s each. The DCC outputs the data to CMS main DAQ via two SLINK64. The DCC also receives (via a TTCrx chip) and distributes the LHC clock and CMS control to its FED crate via the custom backplane. This allows simulation of the clock and control for debugging purposes if the LHC clock is not available.

The CSC local DAQ farm consists of ten computers. Nine of them are served as the data acquisition computers, each equipped with two PCI-express dual-port optical gigabit Ethernet interface cards. One computer serves as the manager and data storage. The farm is used for CSC data monitoring and checking during normal LHC data taking, and is also used as the main system for CSC calibration.

The CSC DAQ system had been extensively tested. It performed successfully during last year's MTCC test. The system is currently being commissioned for the LHC run at CERN.

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Foundation.

Poster session / 46

Final Test at the Surface of the ATLAS Endcap Muon Trigger Chamber Electronics

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For the detector commissioning planned in 2007, a sector assembly of the ATLAS muon-endcap chamber and final test at the surface for the assembled electronics are progressed in CERN intensively. For the test, we built up the DAQ system using test pulse of two types and cosmic ray pulse. So far, 60% of all 320,000 channels have been already tested and most of them were installed into the ATLAS pit.
In this presentation, we will describe the DAQ systems and mass-test procedure in detail, and report the result of electronics test with some actual experiences.

Summary:

For the detector commissioning planned in 2007, a sector assembly of the ATLAS muon-endcap chamber and final test at the surface for the assembled electronics are progressed in CERN intensively.
The thin gap chamber (TGC) is used for the muon-endcap trigger system. The muon-endcap system covers the both endcaps of the detector (1.05<abs(eta)<2.4) to detect isolated muons and give the level-1 muon trigger signal with two ranges of the transverse momentum (pt) of low-pt > 6 GeV/c and high-pt > 20 GeV/c.
As at least three measurement points per track is necessary to identify a muon with even such coarse momentum estimation, there are three TGC discs per endcap (one has three layers with triplet chambers, and the other two discs have two layers each with doublet chambers).

Each disc has the radius of about 10 meters, for example pivot doublet disc has the radius of 11m, and due to this huge detector size, the number of channels become about 320,000 in total. Every disc has commonly twelve sectors. This 1/12 sector is a construction unit for the trigger muon-endcap system for both the chambers and electronics. The sector is also the unit for the trigger and readout system. The electronics systems mounted on a sector are the front-end ASD (Amplifier-Shaper-Discriminator), readout chain (pipeline buffers, derandomizers and parallel/serial converter), trigger decision logic (timing adjustment, bunch ID, coincidence) for the level-1 low-pt muon candidate signals, miscellaneous control and test circuits and Detector Control System (DCS). We also mount modules for high-pt decision logic as well as readout data concentrator nearby the sector, but these are not directly mounted on it.
Once the sector is installed in the whole ATLAS detector system in the cavern, one cannot access easily its electronics as well as cables. We have to test the electronics system after completion of the sector and fix or repair quickly if we find incomplete connection of cables or damage of electronics components.
In order to check all the functionalities, it is necessary to do almost full DAQ operation to the sector. So DAQ systems of two types are built up with being fully compiled with the ATLAS online software framework. First one is using test pulse of two types which our electronics can provide intrinsically, and one can find out dead channels of electronics, incomplete connection between ASD and readout chain with this system. Second one is using cosmic ray pulse. To build up this system, a module called Commissioning Trigger Module (CTM) which can provide cosmic ray trigger with coincidence of trigger decision logic is developed. With this system, one can find out dead channels of a chamber, cable swapping of HV and readout line. We think this cosmic ray trigger will play a very important role at the detector commissioning stage. So far, 60% of all 320,000 channels have been already tested with only few tens remaining dead channels.
In this presentation, we will describe the DAQ systems and mass-test procedure in detail, and report the result of electronics test with some actual experiences.

Parallel session B6 - ASICs 3 future / 47

A circuit topology suitable for the readout of ultra thin pixel detectors at SLHC and elsewhere

Author: Michael Campbell[1]

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Hybrid pixel detectors provide unrivalled pattern recognition capabilities at LHC vertex detectors. Further reducing the material budget is of crucial importance among the many challenges which must be addressed by the vertex systems at SLHC. We propose a two stage front-end pixel readout architecture whereby the discrimination is performed on the sum of the total charge deposited in four neighbouring pixels prior to readout of the analog or binary hit information per pixel. In this way it may be possible to reduce the detector thickness from some 100um to 50um while maintaining a high separation of signal, threshold and noise.

Summary:

Hybrid pixel detectors provide unrivalled pattern recognition capabilities at the LHC vertex detectors. Further reducing the material budget is of crucial importance among the many challenges which must be addressed by the vertex systems at the SLHC. On the detector side a compromise must be found between providing a sufficiently large and prompt signal to permit clean, in-time discrimination and minimising material. The task is complicated by the distortion

of the MIP (Landau) spectrum by charge sharing between pixels - even if charge sharing contributes to enhanced spatial resolution. This issue is akin to the charge sharing which limits the spectral resolution of single photon counting systems.

Here we propose a two stage front-end readout architecture whereby the discrimination is performed on the sum of the total charge deposited in a number of pixels prior to readout of the analog or binary hit information per pixel. The architecture is very similar to that proposed for the Medipix3 development [1]. Each pixel provides four identical currents which are proportional to its input charge to summing circuits located at the pixel corners. Discriminators are connected to the output of each summing circuit. The discriminators communicate with each other event-by-event permitting only one pixel corner to claim a given hit. This implies that the discrimination is performed on the full MIP spectrum allowing the threshold to be placed at around ½ of the Landau peak - as opposed to between ¼ and 1/8th of the peak in existing systems. Although the front-end noise is effectively increased by a factor of 2 due to summing the uncorrelated contributions of 4 front-ends there is still a significant improvement in the separation of signal, threshold and noise. In this way it may be possible to reduce the detector thickness from a few 100 um to around 50 um while working with a threshold of 1 000 e- to 2 000 e-. The approach can be applied to planar or 3D sensors which, being only 50 um thick, are depleted easily even after high radiation doses. Moreover, the new system avoids hits occurring just above the threshold which would be wrongly allocated in time because of discriminator timewalk.

Further material budget reductions can be expected from thinning the readout wafer to an absolute minimum. Also the use of wafer bonding techniques together with deep via interconnect may simplify the mechanical construction of the detector avoiding bump bonding while at the same time allowing thin single chip tiles to be produced.

The paper will focus on simulations of the new circuit architecture using planar sensors and outline some technology options which may in future permit the construction of ultra thin pixel sensors.

[1] R. Ballabriga, M. Campbell, E. H. M. Heijne, X. Llopart, L. Tlustos, “The Medipix3 Prototype, a Pixel Readout Chip Working in Single Photon Counting Mode with Improved Spectrometric Performance,” proceedings of Nuclear Science Symposium IEEE 2006, October 2006, San Diego, USA, published on CDROM

Topical 3: Detector Power Supply and Distribution 3 / 48

Inductor based switching DC-DC converter for low voltage power distribution in SLHC

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In view of a power distribution scheme compatible with the requirements of future trackers in SLHC, we are evaluating the feasibility of on-board inductor based DC-DC step-down conversion. Such converter should be integrated and capable of operating in radiation environments and magnetic field. We present results concerning the choice of the CMOS technology for the integrated circuit, the research of magnetic

components properly working in presence of high magnetic field, calculations of the expected efficiency and EM noise emission.

Summary:

The distribution of power in future LHC experiments represents a difficult engineering challenge, given the global requirements in terms of power needs, available cooling capacity and limited material budget. The harsh radiation environment (up to several Mrd in Total ionizing Dose) requires all the electronics to be radiation tolerant and the intense magnetic field (up to 4T) makes conventional switching converters unusable in many locations.
In view of LHC upgrades where front-end circuits might require even larger supply currents, it is necessary to evaluate an alternative power distribution scheme. This could be based on the distribution of higher voltage (24 -48V) from external power supplies to converters installed locally inside the detectors that have to convert the power to the low voltage and high current required by the front-end circuits. Due to the vicinity of the switching converter to the sensitive detector elements, EM noise has to be carefully studied.
We are evaluating a solution involving an inductor based switching DC-DC step-down converter. A preliminary analysis is in progress in order to understand the feasibility and availability of the different components of the converter that match the above requirements.
We have selected a 0.35 um CMOS technology usually employed in automotive applications. This technology can stand up to 80V and it can be made radiation tolerant with some modification to the layout. Irradiation results on leakage current and threshold voltage shift up to 80 Mrad will be shown.
As regular ferromagnetic inductor cores saturate in such high magnetic field we are evaluating different air core inductor designs. To avoid EM noise we studied the emitted magnetic field from differently shaped air core inductors (solenoidal and toroidal). Inductors of 500nH made by 32 turns with a volume of 340mm^3 were simulated with a 3D finite element program with a current of 1A. The results illustrating the residual magnetic field for different geometries will be shown.
A simulation program was written to evaluate the efficiency of this converter, taking into account the parameters and parasitic values of the CMOS technology, inductor and capacitor and using different values of input voltage, output current and voltage. We will show that an efficiency above 80% could be achieved. In the nominal case of input voltage equal to 24V, output voltage 2.5V, output current 1A, switches on-resistance 110mOhm, inductance 500nH and at a frequency of 1Mhz, the efficiency is 89%.

Parallel session B5 - ASICs 2 ILC / 49

A 130nm CMOS Evaluation Digitizer Chip for Silicon Strips Read-out at the ILC.

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A CMOS 130nm evaluation chip intended to read Silicon strip detectors at the ILC has been designed and successfully tested. Optimized for a detector capacitance of 10 pF, it includes four channels of charge integration, pulse shaping, a 16 deep-analog sampler triggered on input analogue sums, and parallel analog to digital conversion. Tests results of the full chain are reported,

demonstrating the behavior and performance of the full sampling process and analog to digital conversion. Each channel dissipates less than one milliwatt static power.

Summary:

Deep Sub-Micron integrated technologies allow implementing readout chips at low power operation, low material budget, high channel count, and last but not least, fair radiation hardness.

A first 180nm CMOS readout chip for Silicon strips detector has been designed and tested in 2006, and a 130nm improved version has been received and successfully tested recently, taking benefits of the first chip experience.

The 130nm circuit comprises a low-noise charge amplifier with 20mV/MIP gain, a pulse shaper operating between 0.5 and 2 microseconds in order to match various detector lengths and operation conditions, a 16-deep analogue sampler at speeds up to 20 MHz triggered by a sparsifying analogue section, and a 12-bit parallel analogue to digital converter. This structure fits conveniently the ILC timing where data taking occurs for one millisecond, followed by a 200 millisecond time for digitization and readout.

The preamplifier is a folded-cascode structure where the PMOS input transistor is biased at 70 microamperes, providing enough gain to ensure an input stage noise less than 625 + 9e-/pF at 2 microseconds shaping time. The shaper is a CR-RC active filter. Power dissipation is 510 microwatts for the preamplifier and shaper that can be switched up and down in less than 1 millisecond.

The sparsifier block has been designed, setting a threshold over the analogue sum of three adjacent channels. In this way, only channels reacting to this selection are sampled in a circular analogue sampler clocked to store sixteen samples of the shapers outputs, including pedestals. Therefore, digitization of relevant data only is achieved in parallel on 12 bits after data taking using a ramping shared ADC.

A single channel including the analogue sampler fits in a 100 x 800 square micrometers area.

Tests results are reported for all blocks, as well.as Signal to Noise ratio when the chip is wire-bonded to an actual Silicon strips detector and stimulated with actual high energy particles.

Parallel session A4 - Systems, Installation and Commissioning 2 (TK and Pix) / 52

Production and Testing of the LHCb Outer Tracker Front End Readout Electronics

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The LHCb Outer Tracker is a straw drift detector with a modular design and a total of 55 000 readout channels distributed over a sensitive area of 12 double layers of 6x5 m^2 each.
The main electronics readout requirement is the precise (~0.5 ns) drift time measurement at an occupancy of ~4% and 1 MHz readout.
A total of 128 channels are read out by one Front-End box.

About 450 FE-Boxes have been built. Quality Assurance during the production has been performed on single FE-Box components.

The assembled FE-Box is finally commissioned using a special FE-Tester.
The FE-Tester is a programmable pulser with a time resolution of 150 ps capable to simulate all the functionality of the readout mimicking the real detector.

Consequently, problems have been found and solved resulting in good overall performance.

Summary:

The FE-Box readout has a modular structure. Four different type of boards are used, each with its own funcionality, dedicated to a specific stage in the input signal processing.

At first, charge signals from the straw detector are decoupled from the HV (HV board) and amplified, shaped and discriminated by the ATLAS ASDBLR chips (ASDBLR board). Once the signal has been digitized, drift-times are determined and stored in the OTIS TDC (OTIS board) and sent out to the GOL serializer at
L0 accept (GOL board). Optical fibres carry the data 90 meters far from the detector to the TELL1 acquisition board at the L0 output rate of 1.1 MHz, in order to be filtered and finally stored for off-line processing.

The electronics readout requirements is the precise (~0.5 ns) and efficient drift time measurement at an occupancy of ~4% to ensure single hit resolution (200 micron) and efficient charged particle reconstruction.
To achieve the desired performance, several steps of quality assurance during the production have been applied, using dedicated test setups for each type of board.
The tested boards have been finally assembled on an alluminium chassis.
The assembled FE-Box is commissioned using a special FE-Tester.

The FE-Tester is based on the test setup build for the Alice Alcapone tester. The heart of the setup is a PCB with an Altera programmable logic chip. Most of the electronics needed for the tests is built on the controller board to interface the FE-Box howewer, a specific connection board is developed (Flipper Box) with the additional required electronics.

The logic in the Altera is controlled by a LabView program on a PC. The connection between them is a JTAG interface through the parallel port. For the communication with the FE-Box the I2C bus is used.

The FE-Tester consist of a programmable pulser with a time resolution of 150 ps capable to provide all the functionality of the readout (slow and fast controls) mimicking the real detector.

The following tests have been performed on assembled FE-Boxes:
- Timing. Measurement of the time conversion linearity and the global resolution of the OTIS board.

- Threshold Characteristics. A threshold scan is done and the measurement of the half-efficiency-point is carried out for a fixed input charge.
  The relative variation of the half-efficiency-point must be for less than 40 mV all 128 channels as required during the original ASDBLR chip selection.
  The test is performed using two test pulse signals (low and high) generated in the ASDBLR chip. Moreover, an amplitude scan is done and the uniformity the half-efficiency-point for a fixed threshold is measured.

- Noise. Measurement of the noise is studied as a function of the threshold. In the threshold range foresee at operation, the noise is required to be less than 40 kHz.
- Synchronization. Four 8 bit TDC are inside a single FE-Box. Tuning the time difference between test pulse signal and the generated L0, a precision latency scan is done and therefore the synchronization between channels is verified.

The FE-Setup has been used during the R&D phase of the Outer Tracker electronics. Its usefullness was proven by finding problems at an early stage and finally it helped to improve the overall performance. Secondly, the Fe-Tester was used during mass production of the FE-Boxes, and commissioned each FE-Box before delivery to CERN for the installation on the Outer Tracker.

Parallel session B1 - Trigger 1 Atlas / **53**

First Measurements with the ATLAS Level-1 Calorimeter Trigger Preprocessor System

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The level-1 calorimeter trigger is a hardware-based system with the goal of identifying high-pt objects within an overall latency of 2.5us. It is composed of a preprocessor system which digitises 7200 analogue input channels, determines the bunch-crossing of the interaction and provides a fine timing and energy calibration; and two subsequent digital
processors.

The Preprocessor plays a central role during integration of the system as it provides digitisation and readout of calorimeter signals and serves as a digital signal source for the
subsequent processors.

Results of data taken with cosmic muons are shown, and the experience gathered during the system integration is described.

Summary:

The high luminosity and bunch-crossing rate of the LHC pose a particular challenge to the trigger.

The ATLAS level-1 calorimeter trigger has to process 7200 trigger towers within an overall latency of 2.5us. reducing the event rate from 40 MHz to below 100 kHz. It is realised completely in hardware, including ASICs and FPGAs, in a VME-based system.

The Preprocesor of the ATLAS Level-1 calorimeter trigger is a compact system which digitises the detector signals, determines the bunch-crossing number of the interaction and provides a fine timing and energy calibration. The result is sent to two digital
processors, the Cluster Processor and the Jet-Energy Processor. The Cluster Processor identifies electrons/photons and taus. The Jet-Energy Processor identifies jets and computes missing and total transverse energy. Both digital processors provide their information
to the Central Trigger Processor which generates the level-1 decision.

The Preprocessor is a highly modular system consisting of eight crates hosting a total of 124
Preprocessor modules. Each of these modules processes 64 channels in parallel, with the main signal processing performed in the custom-built Preprocessor ASICs located in 16 four-channel Multichip Modules.

The location of the Preprocessor within the trigger system, combined with the fact that it
provides its own DAQ readout path leads it to play a central role when it comes to integrating the trigger with the detectors. It is the only place where digital readout of all trigger towers in parallel is possible. Tasks that are addressed include channel-mapping connectivity tests, timing measurements and signal quality tests.

This talk gives an introduction to the tasks of the level-1 calorimeter trigger with focus on the Preprocessor system. Data taken with cosmic muons are shown in addition to results from the system integration.

Plenary session P4 / 54

DT Sector Collector electronics design and construction

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The CMS detector is equipped with Drift Tubes chambers for muon detection in the barrel region. The Sector Collector modules collect the track segments reconstructed by on-chamber trigger electronics. Data from different chambers are aligned in time and sent to the subsequent reconstruction processors via optical links. Several FPGA devices performing the processing of the data were designed in VHDL, including spy features to monitor the trigger data flow. Prototypes of the boards were operated in the CMS “cosmic challenge”. A test jig was set up with custom hardware and software in order to fully validate final production boards. First experience with installation and running in CMS will be shown.

Summary:

The CMS detector at LHC is equipped with Drift Tubes (DT) chambers for muon detection in the barrel region. Local Trigger electronics, installed on the chambers, processes the hits and reconstructs local track segments within a fixed latency time. Local trigger data, comprising position, impact angle and reconstruction quality, is routed out and collected by Trigger Sector Collector (SC) modules, installed on the towers near to the detector.
Each SC board handles redundant links from the DT chambers of a 30 degrees sector of

the detector, performing reduction and synchronization of the data. The correct synchronization of data from different chambers is crucial in order to allow the track segments to be further correlated by the following stage of the trigger system (Track Finder). Spy features on the SC modules allow the status of the links and the trigger data flow to be monitored, both through local access to the board (VME interface) and through the injection of part of the trigger data into the DAQ stream. Each SC module can also return a "sector trigger", generated as a Boolean function of the local segments, to the chambers of the sector and to the corresponding readout module. Thus, a sector-level trigger and readout system devoted to commissioning and system debugging is implemented.
The SC modules are built by several units: a VME 9U motherboard, hosting a board controller device that provides the VME interface, the interconnection with the readout modules and the sector trigger generation; four mezzanine cards, receiving data from the chambers of the sector, performing data reduction and spying; and a fifth mezzanine card, hosting serializers (GOL chips at 1.6 Gbit/s) and optical drivers for the fiber connection to the counting room, where optical-receiver modules deliver trigger data to the Track Finder boards.
The hardware implementation of the system profits of custom processors implemented on FPGA devices using VHDL programming. The modules installed on towers near to the detector are based on flash-FPGAs, ensuring high fault immunity in a moderate radiation environment. The optical receiver modules are operated in the underground counting room, with no radiation issues, thus they are built with sram-FPGAs that provide embedded gigabit-deserializers and more computational resources. Prototypes of the boards were installed and operated during CMS Magnet Test and Cosmic Challenge: three sectors of the DT detector were synchronized and provided cosmic triggers to the global DAQ. The magnet test allowed also the fringe field to be measured in the tower racks to estimate the required magnetic field tolerance of critical components used in the modules. The components were further tested in a controlled field to optimize their design before launching the final production. In order to validate each board before installation, a test jig was set up using VME custom general purpose I/O modules (Pattern Units). The custom test software accesses the VME bus and it allows patterns to be injected and outputs to be read out at 40 MHz, while checking the status and the spy registers of the board under test.

Topical 1: Detector Power Supply and Distribution 1 / 55

Radiation-Tolerant Custom Made Low Voltage Power Supply System for ATLAS/TileCal Detector

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The Tile Calorimeter front-end electronics of the ATLAS detector is powered by 256 custom-made low voltage power supplies (LVPS) called LVBOX. Each LVBOX contains eight 150W DC/DC single-output modules transforming 200VDC input into various independent low voltage outputs (+3.3V, +/-5V, +/-15V). A local control and communication board using ELMB permits to monitor behavioral parameters (temperatures, Iin, Iout, Vin, Vout, sense lines reading) and trim Vout of each DC/DC module (Brick) using CAN Bus communication. The

power supply is water cooled, is capable to survive a total integrated radiation dose of 40krad, and can work in external magnetic field higher than 0.02 Tesla. The LVPS is now manufactured in 256 production units.The 200VDC input voltage for these LVBOXes are delivered from 22 bulk power supplies HPS1 located in USA15 control room. Sixty-four auxiliary control and power supply boards (AUX Board) in the same control room are required to give power for the LVBOX monitoring and control circuits. Four LVPS Interlock Boards are capable to switch off all LVPS and HPS1 supplies in case of water cooling system leak or general switch off of the Tile detector.

Summary:

LVBOX

The power supply, called LVBOX, is mounted in the vicinity of Tile Calorimeter detector modules (drawers) inside so called FINGERS [1]. Each LVBOX contains eight independent DC/DC converters - bricks (3.3VDIG, +5VMB, -5VMB, +5VDIG, +15VMB, +5VHV, +15VHV, and -15VHV), so called ELMB Motherboard, ELMB plug-in board [2], 200VDC distribution Fuse-Board, internal cable set, and chassis and water cooled heatsink. The ELMB Motherboard and ELMB module are connected to DC/DC converters and permit remote PC monitoring of their behavioral parameters (temperatures, Iin, Iout, Vin, Vout, DIG and MB side sense line voltages) and set trimming of Vout. Start-up sequence of LVBOX is carried out in 3 groups of bricks[5]. HV or DIG side brick group shutdowns are triggered by most critical power lines: -5VMB, +15VMB, and -15VHV. The LVBOX is exposed to radiation and magnetic field in the ATLAS cavern. The Tile LVPS system is computer managed by the Detector Control System (DCS) software through a CAN Bus line that communicates with the local ELMB of each power supply. The LVBOX of each Tile detector module has to deliver average power of 300W. Production of final 256 units started at CERN in January 2007.

DC/DC SWITCHING POWER SUPPLY MODULE - “BRICK”

The key component of the LVBOX is a small size (80 x 80 x 30mm), radiation and magnetic field tolerant, single output DC/DC dual transistor synchronous forward converter based on LT1681 chip[6]. Full custom design using only COTS (Commercial Off The Shelf) components and the universal printed circuit board design enabled to select three brick versions of various outputs (+3.3V, +5V, or 15V) by means of only several components change. Brick input voltage is +200VDC due to the radiation derating. The maximum output power from the brick is 150W. The DC/DC converter design enables high efficiency of energy conversion: 72% for 3.3V @10A Iout, 85% for 5V version @10A, and 82 % for 15V version @6A, respectively[3]. Switcher uses the current mode control and has fixed switching frequency of 300kHz. The brick frequency can be synchronized with other DC/DC modules inside LVBOX. In order to start, the brick needs a remote auxiliary Start-Up voltage of +15V coming from the AUX Board in USA15 control room. Important brick features are active Overcurrent and Overvoltage protection circuitry[5]. Innovative technology of brick cooling (especially of the switching FET power transistors, power inductors and high frequency transformer) was applied by means of custom made Al2O3 ceramic spacers. 2048 bricks plus spares are needed for the LVBOX production.

Brick has integrated remote control and measurement circuitry for both input (Iin/Vin) and output (Iout/Vout) parameters. Moreover, three temperature sensors are also present to control brick cooling. The Vout voltage can be trimmed in range of 15%. This feature enables a remote correction of Vout voltage during radiation degradation of output voltage of LVPS. The trimming, sensing and remote control of the brick are carried out by the ELMB module [2].

Extensive irradiation test campaigns of COTS components and of the brick prototype were performed at PSI, Villigen, CH (protons 2002, 2003, 2004), at CERN (neutron P2B 2004, TCC2 SPS tunnel 2002, 2003 campaigns), Saclay (Co60 gamma test 2003) and at INT Portugal NIEL tests in 2003[3].

Experimental results demonstrated that bricks and ELMB motherboards could work together without problems up to 20krad TID, and survive up to 2.15E+12 n/cm^2 neutron fluency. Bricks radiation tolerance is even higher reaching 35-38krads. Bricks are also designed to be operational in external DC magnetic field without damage. Magnetic field decreases efficiency caused by DC magnetization of the HF transformer ferrite core. Decrease of the DC/DC converter efficiency measured at CERN magnet with external B at 200 Gauss (TILECAL nominal level) was max -1.5%, and at 500 Gauss was -3%.

200VDC BULK POWER SUPPLIES

The input for the Tile power system is 200V DC voltage that is converted from three phase mains 3x230V~. For this purpose 22 custom made bulk power supplies HPS1 are needed. One HPS1 unit contains three 1.7kW power channels delivering 200VDC/8.5A [4], and can power 12 LVBOX power supplies. HPS1 are not radiation tolerant and therefore are deployed in USA15 control room of the ATLAS cavern. They were developed at TESLA Company, Prague, CZ.

AUX BOARD

The Auxiliary (AUX) Board is 6U sized pcb board and generates all auxiliary signals and power voltages for one cluster of 4 LVBOXes. The board consists of 3 x 4 isolated power supplies for the ELMB motherboard (trimmed between 6.8 - 14.5V), for ELMB chip (6.8 - 14.5V) and Start-up signal (15 - 25V) for LVPS bricks. It also contains current sources for LVBOX HV/DIG side remote on/off current loop controls and an interlock circuitry. The board is controlled via ELMB module hosting custom made version of ELMB software. So all AUX boards are creating another CAN bus network and theirs control is embedded into the overall remote control system. The distance between 64 AUX Boards or 22 HPS1 supplies in USA15 room and 256 LVBOXes in the ATLAS cavern varies from 60 to 100 meters depending on the position of particular power supply.

LVPS INTERLOCK BOARD

The LVPS interlock board receives ATLAS DSS cooling interlock signals. In case of interrupted water cooling to the Tile Calorimeter, one LVPS Interlock Board will disable functioning of 64 LVBOXes. It is hardwired together with 16 channels of 200VDC HPS1 bulk power supplies and 16 AUX Boards.

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Parallel session B6 - ASICs 3 future / 56

a low power and low signal 4 bit 50MS/s double sampling pipelined ADC for Monolithic Active Pixels Sensor

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For CMOS monolithic active pixels sensor readout, we developed a 4 bit very low power analog to digital converter using a double sampling pipelined architecture. The converter consists of a non-resetting sample and hold stage followed by a 2.5 bit sub-ADC and a 2 bit flash. This prototype consists of 4 ADC double-channels; each one is sampling at 50MS/s and dissipates only 2.3mW at 3.3V supply voltage. It includes a fast power down input. The size for the layout is 80µm*0.9mm. This corresponds to the pitch of 4 pixel columns, each one is 20µm wide.

Summary:

SUMMARY:
CMOS Monolithic Active Pixel Sensors (MAPS) provide many well-known advantages for vertex detectors, high precision beam telescopes etc… Granularity, radiation tolerance, random access and high speed read-out are the most appealing characteristics. However, there are several constraints on the design of the associated readout electronics:
· The process is chosen first according to its particle detection performances.
· The minimum readable signal is very low (»1 mV).
· The layout dimensions must fit with the narrow pixel pitch.
· The power dissipation is a critical issue.
The design presented here is a 4 bit double sampling pipelined Analog to Digital Converter (ADC). According to the power dissipation and the layout size, it is an improved version in comparison with the results we published last year (San Diego IEEE NSS 2006). This design is one of the candidates to equip the pixels array designed at IPHC-Strasbourg in collaboration with DAPNIA-Saclay for the future International Linear Collider (ILC) Vertex Detector.
The converter consists of a sample and hold amplifier (SHA) stage followed by a double sampling pipelined stages.

A) The Sample and Hold Amplifier (SHA):

It amplifies the small incoming signal by 4 and compensates the amplifier's offset effect and the input common mode voltage fluctuations.
A charge redistribution architecture is used. Four non overlapping clock signals control the sampling and the hold phases. During the sampling phase, the input signal is stored onto the sampling capacitor (400 fF). During the hold phase, the charges are transferred onto the feedback hold capacitor (100 fF).

B) Double sampling pipelined ADC:

The pipeline architecture provides the best deal between speed, consumption and area required for the MAPS. A 2.5 bit pipelined stage followed by 2 bit flash stage is used in this ADC. A digital error correction stage is added to leave room for the comparators' offsets.
Two successive stages of the ADC are always in opposite clock phases. Therefore the amplifier and the comparators are shared between two adjacent parallel ADC channels. The full logic part is also shared. Due to the critical input signal, each ADC channel has its own SHA stage. By using double sampling switched capacitor method, the equivalent sampling rate is doubled, the power is reduced almost by 40% and the surface is significantly reduced compared to the simple pipelined architecture. In contrast, the complexity of the pipelined stage is increased; more switches and more different clock phases are needed. Two important side effects are caused by sharing the amplifiers. First, the load

capacitance of the amplifier is increased and that affects its bandwidth requirements. Second, the amplifier offset is never reset; this can be tolerated by an adequate amplifier open loop DC-gain.
For the ILC case, the beam duty cycle is 1/200. A bias pulsing stage is integrated in the circuit. Therefore, the analog part is switched OFF or ON in less than 1µs.
We have already designed and successfully tested two first prototypes of 5 bit simple pipelined ADC. The design presented here introduces several improvements and theses results will be presented.

Poster session / **57**

SKIROC : A FRONT-END CHIP TO READ OUT THE IMAGING SILICON-TUNGSTEN CALORIMETER FOR ILC

Author: Julien Fleury[1]

Co-authors: Christophe de La Taille [2]; Gisele Martin Chassard [2]; Ludovic Raux [2]; Michel Bouchel [2]

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This abstract describes the new front end ASIC designed for the silicon tungsten electromagnetic calorimeter called SKIROC.
This new chip embeds the main features required for the ILC final detector.

Summary:

Integration and low-power consumption of the read-out ASIC for the International Linear Collider (ILC) 82-million-channel W-Si calorimeter must reach an unprecedented level as it will be embedded inside the detector. Uniformity and dynamic range performance has to reach the accuracy to achieve calorimetric measurement. A first step towards this goal has been a 10,000-channel physics prototype of 18*18 cm which is currently in test beam in CERN.
A new version of a full integrated read out chip (SKIROC) has been designed to equip the technologic prototype to be built for 2009. Based on the running physics prototype ASIC (FLC_PHY3), it embeds most of the required features expected for the final detector.
The dynamic range has been improved from 500 to 2000 MIP. An auto-trigger capability has been added allowing built-in zero suppress. The number of channel has been doubled reaching 36 to fit smaller silicon pads and the low-noise charge preamplifier now accepts both AC and DC coupled detectors. After an exhaustive description, the measurement results of that new front-end chip will be presented. The results on the technological R&D concurrently conducted on the ultra-thin PCB hosting both the front-end electronic and the silicon detectors will also be described.

Topical 3: Detector Power Supply and Distribution 3 / **58**

High Radiation Resistant DC-DC Converter Regulators for use in Magnetic fields for LHC High Luminosity Silicon Tracker

Author: Satish Dhawan[1]

Co-authors: David Lynn [2]; James Kierstead [2]; Oliver Keith Baker [1]; Paul Tipton [1]

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We have found at least one commercial Buck regulator with integrated inductor fabricated with 0.25μm CMOS technology. This device was exposed to a Cobalt 60 source at BNL; there was negligible effect to 100 mega rad dosage (when the exposure was terminated). System implementation issues are being evaluated.

Summary:

At the "12th Workshop on Electronics for LHC and Future Experiments" held in Valencia, Spain 25-29 September, 2006, we presented some results showing operations using air core coils.

Our focus is to investigate the possibility of using DC-DC converters for the powering of the silicon Tracker for the high luminosity ATLAS upgrade. Our objective is to locate these regulators on the same PCB as the silicon readout chips.

CMOS at small feature size (0.25um or less) shows promise for radiation environments. We recently found out that at a company had designed a Buck regulator using 0.25um CMOS technology. A device mounted on an evaluation board with an output of 4 amps @ 1.8 Volts was exposed to Cobalt 60 source. There was no noticeable effect even with an accumulated dosage of 100 mega rads when the exposure was stopped (after 3 weeks of exposure). This chip is a multichip module with a silicon die and a ferrite rod inductor. For our application (high radiation, high magnetic field), this inductor will be replaced by an air core coil.

We are investigating
1. Switching noise of the Buck into the silicon strip detector and its readout chip.
2. Antenna affect, the charge from the input capacitors is transferred to the output capacitors at a frequency of 5 MHz with a duty cycle given by output voltage = Output voltage /Input voltage. Traces on the PC board become part of the antenna. One solution is to bury these traces in the inner layers of the PCB.
3. Are other vendors working on 0.25um CMOS technology Buck regulators operating at higher frequencies?
4. More radiation testing

Figure: Power conversion Efficiency vs Output current before and after 100 Mrad Gamma exposures.

At the conference, we shall report on the results of our research.

Poster session / **59**

Software environment for controlling and re-configuration of Xilinx Virtex FPGAs

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Co-authors: Benjamin Schockert [2]; Carmen Gonzalez Gutierrez [3]; Dag Larsen [1]; Dieter Röhrich [1]; Håvard Helstrup [4]; Johan Alme [1]; Ketil Røed [4]; Kjetil Ullaland [1]; Luciano Musa [3]; Matthias Richter [1]; Ralf Keidel [2]; Roberto Campagnolo [3]; Sebastian Bablok [1]; Thomas Beierlein [5]; Tobias Krawutschke [6]; Torsten Alt [7]; Volker Lindenstruth [7]

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The Time Projection Chamber (TPC) is one of the sub-detectors of the ALICE detector that is currently being commissioned as a part of the Large Hadron Collider (LHC) at CERN. The Detector Control System (DCS) is used for control and monitoring of the system. For the TPC Front End Electronics (FEE) the control node is a Readout Control Unit (RCU) that communicates to higher layers via Ethernet, using the standard framework DIM (Distributed Information Management). The RCU is equipped with commercial SRAM based FPGAs that will experience errors due to the radiation environment they are operating in. This article will present the implemeted hardware solution for error correction and will focus on the software environment for configuration and controlling of the system.

Summary:

In this article the implementation of the DCS for FPGA configuration and error correction in the TPC Front End Electronics (FEE) is introduced. In the field layer the DCS consists of an RCU (ReadOut Control Unit) motherboard with DCS (Detector Control System) board and several Front-End-Cards (FECs) attached. On the RCU an SRAM based Xilinx Virtex-II Pro FPGA is essential for the read-out chain. Since the Front-End-Electronics operates in a radiation environment single event upsets can occur. The Xilinx Virtex-II supports a feature called Active Partial Reconfiguration. This allows for reconfiguration of the FPGA without interrupting operation. There is also radiation tolerant 8 MB of Flash memory and a Flash based Actel FPGA on the RCU motherboard. The Actel FPGA communicates with the DCS Board, the Flash Memory and the configuration memory of the Xilinx Virtex-II. This hardware solution has three different modes of operation: initial configuration, scrubbing (continously overwriting the configuration memory) and frame by frame readback verification and error correction. The last mode reads back every frame one by one and if an error is found this one frame is overwritten in the configuration memory. It is also possible to count the number of errors that occured using this mode.
The DCS board drives a Linux Operating system which provides a communication system called the FeeServer (Front-End-Electronics Server). The FeeServer is in charge of publishing values and status information as well as receiving commands from the upper layers. To provide a remote way for configuring the Xilinx a Linux device driver is used and functions in the FeeServer have been implemented to access the Xilinx device through the standard communication channels. The FeeServer consists of a device independent core and the so called ControlEngine (CE) to support the use in different detectors. Finite State Machines (FSM) for each mode of operation have been introduced in the Control Engine of the FeeServer. In case of a frame by frame readback verification and error correction it is also possible to publish the number of occurred errors to the higher layers.
Configuration files are stored in the Configuration Database and are transported by the DCS communication software to the FeeServer. Since error tolerance and robustness are mandatory checksums are used to check the data integrity. This article focuses on the software part of the configuration and error correction modes.
Although the presented remote configuration functionality was developed for the RCU and the Virtex-II, it is possible to use this solution in other parts of the detector as well. In these parts the devices to be configured are Xilinx Virtex-4s, which are also supported by the device driver.

Parallel session A4 - Systems, Installation and Commissioning 2 (TK and Pix) / 60

Towards the final ATLAS Pixel Detector Control System

Author: Susanne Kersten[1]

Co-authors: Dirk Hoffmann [2]; Jennifer Boek [3]; Jens Weingarten [4]; Joachim Schultes [3]; Kerstin Lantzsch [3]; Markus Keil [5]; Olivier Pisano [2]; Peter Kind [3]; Peter Maettig [3]; Sebastian Weber ; Tobias Henss [3]

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The innermost part of the ATLAS experiment is a pixel detector, built by around 1750 individual detector modules. To operate the modules, readout electronics and other detector components, a complex power supply and detector control system (DCS) is necessary. This includes a large number of crates, which house the different hardware components as well as a PC net, where the different control projects are running. To test the final detector after its assembly before it is installed in the ATLAS cavern a large test system was setup at CERN, which allows to operate ca. 10 % of the detector in parallel. Since autumn 2006 this system is in permanent operation. As nearly everywhere the final control hardware is used, its reliability and the performance of the control software could be investigated. An overview on our DCS hard- and software is given and we report on the experience with the control system.

Susanne Kersten 'on behalf of Atlas Pixel Detector Collaboration'

Parallel session B2 - Trigger 2 CMS and Atlas / 61

Modular Trigger Processing, The GCT Muon and Quiet Bit System

Author: Matthew Stettler[1]

Co-authors: Gregory Iles [1]; John Jones [2]; Kostantinos Fountas [2]; Magnus Hansen [1]

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The CMS Global Calorimeter Trigger system's HCAL Muon and Quiet bit function is being implemented with a novel processing architecture. This architecture utilizes micro TCA, a modern modular communications standard based on high speed serial links, to implement a processing matrix. This matrix is configurable in both logical functionality and data flow, allowing far greater flexibility than current trigger processing systems. In addition, the modular nature of this architecture allows flexibility in scale unmatched by traditional approaches. The Muon and Quiet bit system consists of two major components, a custom micro TCA backplane and processing module based. These components are based on Xilinx Virtex5 and Mindspeed crosspoint switch devices, bringing together state of the art FPGA based processing and Telcom switching technologies.

Summary:

A secondary function of the CMS Global Calorimeter Trigger system (GCT) is to provide reordered HCAL Muon and Quiet bit data to the Global Trigger. This function is being implemented utilizing a multi-gigabit switched serial mesh based processing topology. It represents an evolution of the current GCT architecture, taking advantage of the lessons learned implementing the optical data transmission and concentration between

the Regional Calorimeter Trigger racks and the GCT. This topology is realizable in the micro TCA communications equipment standard, with a custom (though spec compliant) backplane.

Traditional detector triggering systems have always been large hardware designs that pushed the state of the art in both speed and density. Due to their optimization for throughput, they have tended to be fully custom one-off systems, complex and difficult to modify, and generally lacking in clean internal interfaces.

A more desirable architecture would support fine grained modularity, and be based on a suitably flexible commercial standard, while supporting the extreme data rates required of current trigger systems. Recent advancements in FPGA and data switching technology, as well as the emergence of the Advanced Telecommunications Architecture, have made it practical to consider a modular, commercial standards based architecture for future triggering systems.

The GCT HCAL Muon and Quiet bit functionality entails the reorganization of the data as collected by the 18 Regional Calorimeter Trigger crates, and transfer to the Global Trigger (GT). In addition, the serial encoding of the data needs to be changed to provide compatibility with the GT. While computationally fairly straightforward, the number of channels (18, 1.6Gbit in, 24, 1.2Gbit out) is significant. This communication intensive design is a good fit for an initial implementation of a micro TCA based modular processing system.

The design is based on two main modules, a custom micro TCA backplane and a processing module. The custom backplane is an intelligent micro TCA implementation embedding hub functionality in the backplane. This allows the inclusion of large crosspoint switches (Mindspeed M21161), creating a high performance data routing fabric. A large FPGA (Xilinx V5LX110T) forms the basis of the processing modules, which receive and reformat the data.

Poster session / 62

Installation and Commissioning of the CMS Timing, Trigger and Control Distribution System

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Co-authors: Andre Holzner [1]; Tim Christiansen [1]

[1] *CERN*

The Timing, Trigger and Control (TTC) distribution system must ensure high-quality clocking of the CMS experiment to allow the physics potential of the LHC machine to be fully exploited. This key system provides the synchronization tools – bunch clock, first level Triggers and fast commands – that enable all sub-detector systems to take data for the same LHC collision. The challenges of its installation are described, along with the tools used to commission the system and verify that its design goals are met.

Summary:

The Compact Muon Solenoid (CMS) detector is currently being assembled at the CERN Large Hadron Collider (LHC), due to start operation in 2007. The LHC will collide bunches of protons with a bunch crossing frequency of 40.0789MHz at an energy of 7TeV/beam. Given the high target luminosity of 10^34/cm2/s it is of paramount importance that data coming from all parts of the CMS detector be assigned to the correct (same) collision. The Timing, Trigger and Control (TTC) distribution system that provides all front-end and back-end components in CMS with the bunch clock is thus a key component in the overall system without which all others cannot take

beam-synchronous data. There are over 10 million individual detector channels spread over 10 sub-detectors systems that rely on the TTC distribution system. The CMS TTC system is based upon a common LHC-wide development that has been adapted to the specific needs of the CMS experiment. The TTC system distributes the bunch clock, First-level Trigger (L1A) and fast control signals from a central location in the CMS underground counting room to the sub-detector electronics located in both the counting room and on the CMS detector itself. Fast control signals are used to synchronize the sub-detector systems with one another and with the LHC machine – an example signal is the "Orbit" pulse which marks the start of a turn in the machine every 3564 clocks and is a fundamental tool for synchronization to the LHC machine's bunch structure.
The installed TTC system must be able to transmit the bunch clock of the LHC that is expected to be 40.0789MHz with a tolerance of at least ±3kHz to allow for beam path variations. Requirements on the Jitter of the clock signal come from two major sources: the timing accuracy intrinsic to the various sub-detectors of CMS and the requirements of high-speed serial links that are widely used in the readout systems. For the detector types used in CMS, the former requirement is rather loose – of the order of 1ns. It is the requirement placed on the reference clocks for synchronous high-speed serial links that read-out data at speeds above 1Gb/s across many sub-detector systems in CMS which provides the most stringent constraint of maximum jitter of 350ps pk-pk. While care has been taken during the design and testing of the electronic ASICs and modules that make up the system to ensure that these requirements are met, the installation and commissioning of the TTC system provide the final in-situ verification.
The top of the CMS TTC distribution system is installed over two 52U-high racks in ten 6U VME crates. These racks are located approximately 100m below the surface in the CMS underground counting room in a central position to minimize the signal path for time-critical signals such as the L1A Trigger. Nine of the ten VME crates house the distribution electronics for the sub-detectors of CMS while electronics in the tenth receives the beam timing signals (Clock and Orbit) from the LHC RF systems and fans those signals out to the sub-detector TTC crates. Each sub-detector crate holds one Local Trigger Controller (LTC) VME module, up to six TTC CMS Interface (TTCci) modules and up to six TTC Encoder and Transmitter (TTCex) modules. The LTC is used by sub-detectors to provide the sequences of Triggers and Fast Commands necessary for testing and commissioning in the absence of a Central (Global) Trigger system. These sequences are translated by the TTCci module into the commands specific to that sub-detector system and these commands are then encoded and sent to the sub-detector over single-mode optical fiber by the TTCex modules. Fibers are installed within the counting room to reach the racks used by the individual sub-detectors, from where the signals are split optically and further distributed to the on-detector electronics.
Once installed, the correct functioning of the system must be verified.
Commissioning of the TTC distribution in CMS will proceed in two phases: verification of signal integrity on installed lines that is carried out before hand-over to each sub-detector; followed by a period of signal verification and synchronization testing that is carried out with the sub-detectors. Software tools based on CMS-wide Data Acquisition framework XDAQ have been put in place to allow the installers to rapidly check the quality of the connections that are made. These are augmented by detailed measurements of the time stability of the central system in the first instance, followed by measurements of the signals received at the ends of the distribution system. Once the system is sufficiently stable the integration of sub-detector systems with the central systems is done one system at time. In this phase the synchronization of the entire system is built up step by step at the end of which the whole of CMS will be ready to sample the LHC beams when they turn on. The overall synchronization scheme will be described in detail for the individual systems and then the bringing together of all the systems to form a coherent whole. Once CMS is in this state a global phase shift of the master clock will be all that will be required to bring the detector sampling into phase with the actual particle crossings in the LHC.

Parallel session B4 - ASICs 1 FE chips / 63

VFAT2 : A front-end system on chip providing fast trigger information, digitized data storage and formatting for the charge sensitive readout of multi-channel silicon and gas particle detectors.

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Co-authors: Giovanni Anelli [1]; Herve Mugnier [2]; Jan Kaplon [1]; Kostas Kloukinas [1]; Pierre Chalmet [2]; Walter Snoeys [1]

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The architecture, key design parameters and results for a highly integrated front-end readout system fabricated as a single ASIC is presented. The chip (VFAT2) comprises complex analog and digital functions traditionally designed as separate components. VFAT2 contains very low noise 128 channel front-end amplification with programmable internal calibration, intelligent "fast OR" trigger building outputs, digital data tagging and storage, data formatting and data packet transmission with error protection. VFAT2 is designed to work in the demanding radiation environments posed by modern H.E.P. experiments and in particular the TOTEM experiment of the LHC.

Measured results are presented demonstrating full functionality and excellent analog performance despite intensive digital activity on the same piece of silicon.

Summary:

VFAT2 is a "trigger and tracking" front-end ASIC, designed primarily for the readout of sensors in the TOTEM experiment of LHC.

The VFAT2 chip has been designed in quarter micron technology and has two basic functions. The first (Trigger) is to provide programmable "fast OR" information based on the region of the sensor hit. This can be used for the creation of a trigger and in CMS it provides input to the first level trigger (LV1A). The second function (Tracking) is for providing precise spatial hit information for a given triggered event.

TOTEM itself comprises three operating regions each employing a different sensor technology to detect charge from traversing minimum ionising particles (MIPs). Silicon strips, Gas Electron Multipliers (GEM) and Cathode Strip Chambers (CSC) are the technologies used each having different electrical characteristics. VFAT2 has been designed to provide the charge readout and low noise MIP discrimination for all 3 sensor technologies.

VFAT2 has 128 low noise input channels which after discrimination provide binary "hit" information which is stored until a trigger is received. The storage capacity enables trigger latencies of up to 6.4us (< 256 clock periods at 40 MHz), simultaneously store data for up to 128 triggered events and enable continuous dead time free operation with up to 100kHz Poisson distributed trigger rates. Time and event tags are added to the triggered data which are then read from the chip in the form of digitized data packets at 40 Mbps.

VFAT2 has many programmable functions controlled through an I2C interface. These include : internal biasing of analog blocks via 8 bit DACs, individual channel calibration via an internal test pulse with 8 bit programmable amplitude, calibration test pulse phase control, operate with positive or negative detector charge, 8 bit global threshold plus a 5 bit trim DAC threshold adjust on each channel, multiple possibilities for channel grouping for the "Fast OR" outputs, variable latency, various test modes plus an automatic self test of the digital memories. Chip status information including occupancy and SEU rates can be read via I2C.

For robustness against single event upsets (SEU), the digital parts of VFAT2 have been designed with hamming encoding for the SRAMs and triplication logic for the I2C interface and control logic. All analog circuitry employs layout techniques that reduce threshold voltage shifts under ionising radiation.

A major design challenge was to integrate the multitude of digital functions without having a significant impact on the analog performance. Stringent design techniques to "deafen the listener" and "silence the

talker" have been employed to all analog and digital modules.

Measurements from the chip show all modules to be 100% functionally correct. The shaper has a peaking time of 22ns. The expected front-end noise performance of approximately 500e + 50e/pF is maintained. The total power consumption is 572mW.

VFAT2 has successfully integrated complex analog and digital functions into a single ASIC without compromising noise performance. This paves the way to future (post LHC) designs which will require further integration still.

Parallel session A1 - Systems, Installation and Commissioning 1 (DAQ, DCS, Cal) / 64

A MAPS-based readout for Tera-Pixel electromagnetic calorimeter at the ILC

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For the ILC physics program, the detectors will need an unprecedented jet energy resolution. For the electromagnetic calorimeter, the use of a highly granular silicon-tungsten calorimeter has been proposed. The status of a silicon readout option, which uses Monolithic Active Pixel Sensors (MAPS), will be presented. This novel design provides extremely fine granularity with integrated binary readout. This leads to a "Tera-Pixel" electromagnetic calorimeter system. A overview of the MAPS concept will be given along with the advantages of this design. We present first results of the prototype sensor together with simulation results showing the expected detector performance.

Summary:

For the readout of such a highly granular Silicon-Tungsten calorimeter, there are several options available. From detailed simulation of the Tera-Pixel ECAL we know, that most pixels are only hit once per event, if one chooses a pixel size of 50 x 50 μm. We can employ a simple binary readout using a comparator instead of an analog readout, which simplifies the pixel layout. We have then designed and fabricated a CMOS Monolithic Active Pixel Sensor (MAPS) in the novel INMAPS process. The INMAPS process is a standard 0.18 micron CMOS image-sensor technology with a high energy "deep-Pwell" implant located beneath the active circuits. A conventional MAPS design will experience charge sharing between the sense-node(s) and any PMOS active devices in the pixel which can dramatically reduce the efficiency of the pixel. By implanting the "deep-Pwell" in the pixel regions containing active circuits, charge deposited in the epitaxial layer is reflected and conserved for collection at only the exposed collection diode nodes. The pixels contain four N-well diodes for charge-collection; analog front-end circuits for signal pulse shaping; comparator for threshold discrimination; digital logic for threshold trim adjustment and pixel masking. Pixels are served by shared row-logic which stores the location and time-stamp of pixel hits in local SRAM, at the target 150ns beam bunch crossing rate of the ILC. The sparse hit data is read out from the columns of logic in the quiet time between bunch trains. A prototype sensor consisting of 8 units of 42x84 pixels with 6 million transistors in total has been produced. The data acquisition requirements for such a system with 10^12 readout channels are driven by the noise. Even with a noise level of 10^-6, there will be 1 million hits per event and the occupancy is entirely noise driven. Therefore the required DAQ bandwidth is around 500 Gbit/s. Another system

issue is the power consumption. For a MAPS detector with a 1 % duty cycle we obtain a power consumption of 40 μW/mm^2. The test sensor will allow us to explore options to further reduce this. A clear advantage of the MAPS approach is the fact, that it can be manufactured in a industry standard process and will be cheaper to produce than the combination of high resistivity silicon sensor and a readout chip. Parallel to the design work on the sensor itself, we have worked extensively on the physics simulation of a MAPS-based ECAL. For an accurate sensor simulation the Sentaurus package was used for optimizing the design layout and to study the charge spread within the MAPS pixels. To study the physics performance, the MAPS based calorimeter was implemented in the MOKKA detector simulation, which is based on GEANT4. The simulation output has been used to test Particle Flow Algorithms and some first results of using Particle Flow with a highly granular MAPS-based ECAL are presented.

Parallel session B1 - Trigger 1 Atlas / **65**

The ATLAS Barrel Level-1 Muon Trigger Sector-Logic/Rx off-detector trigger and acquisition board

Author: Federico Spila[1]

Co-authors: Alberto Aloisio [2]; Andrea Salamon [3]; Emilio Petrolo [1]; Ettore Gennari [1]; Francesca Pastore [1]; Riccardo Vari [1]; Stefano Veneziano [1]

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The ATLAS experiment uses a system of three concentric Resistive Plate Chambers (RPC) detector layers for the level-1 muon trigger in the air-core barrel toroid region. The algorithm looks for hit coincidences within different detector layers inside the programmed geometrical road which defines the transverse momentum cut. The on-detector electronics that provides the trigger and detector readout functionalities collects input signals coming from the RPC front-end.
Trigger and readout data from on-detector electronics are sent via optical fibres to the off-detector electronics. Six or seven optical fibres from one of the 64 trigger sectors go to one VME Sector-Logic/RX module, that latter elaborates the collected trigger and readout data, and sends readout and trigger data respectively to the Read-Out Driver modules and to the Central Level-1 Trigger.
We present the functionality and the implementation of the VME Sector-Logic/RX module, and results from the first cosmic ray run data collected using this module.

Summary:

The ATLAS experiment uses a system of three concentric Resistive Plate Chambers detectors layers for the level-1
muon trigger in the air-core barrel toroid region. The trigger classifies muons within different programmable
transverse momentum ranges, and tags the identified tracks with the corresponding bunch crossing number.
The algorithm looks for hit coincidences within different detector layers inside the programmed geometrical road
which defines the transverse momentum cut.
The full experiment is divided in 64 trigger sector. One sector side is composed by three planes of RPC detectors
(inner, middle-pivot and outer), each plane being composed normally of six or seven adjacent RPC detectors. A
trigger tower is composed by three half RPC detectors (inner, pivot and outer) belonging to the same trigger
sector, so that there are six or seven trigger towers per trigger sector.
For every Trigger Tower, trigger and readout data, coming from on-detector electronics, are sent via

optical fibres
to the off-detector part of the trigger. Six or seven optical fibres (one per Tower), coming from one trigger sector
go to one VME Sector-Logic/RX module (from now “Sector Logic”), which elaborates the collected trigger and
readout data, and sends readout and trigger data respectively to the Read-out Driver (ROD) module and to the
Muon-Central Trigger Processor Interface (MUCTPI) module.
Sector Logic modules are mounted on VME Crates in USA 15, far form the detector. There are 16 VME Crates,
each with 4 Sector Logic (for a total of 64 Sector Login, one per ATLAS Trigger Sector).
Data communication from SL to others modules are made using the ROD-BUS (a custom VME Backpanel that
enables adjacent slot in the same VME crate to share a custom data-bus.
Every Crate has two “5-slot ROD-BUS”, on which modules are mounted in this order: 1 Muctpi Interface module;
1 SL module; 1 ROD module; 1 SL module; 1 Muctpi Interface module.
Muctpi Interface is a module that receives trigger data from SL and drives a parallel LVDS bus to reach the
MUCTPI module mounted in USA 15 at a 10m distance.
Every SL receives data from 8 Optical link from the Trigger Towers elaborates, and send data to 1 Muctpi Interface on 1 side and one ROD on the other side:
• 8-bit trigger data per link are processed in a pipe-line 3 clock periods long, that produce a 32 bit word with
information about the 2 highest pT muon candidate, and the Bunch Crossing value.
Trigger data so generated are sent to MUCTPII Interface.
• Up to 8 16-bit word wide read-out “Pad Fragment”, are temporary stored using internal FIFOs, and are processed to generate the 32 bit “SL Fragment” (that contains all the Pad fragments of the same Trigger event).
SL Fragments are sent to ROD Module via a Serializer chip, which provides LVDS data transmission at 1280 Mbps
speed-rate.

The Sector Logic processor core is based on two Xilinx FPGA, one dedicated to VME Communications and to other
services (JTAG, I2C, etc...). The other FPGA is dedicated to the trigger and read-out logic.
The first Sector Logic modules are mounted in USA 15 together with some ROD and MUCTPI modules, and will be
used to collect data of the first ATLAS Cosmic Ray Run. The result of this run will be presented.

Parallel session A5 - Systems, Installation and Commissioning 3 (TK and Pix, Lumi) / 66

SCT and TRT Performance from Cosmic Ray Runs

Author: Heidi Sandaker[1]

[1] *CERN*

The Barrel and Endcap SCT detectors have been integrated into the barrel and Endcap TRT detectors. There have been cosmic ray runs for the Barrel and Endcaps in the surface building (SR1) and after installation in the ATLAS cavern. This talk will focus on the most recent results. The procedure for timing in the SCT and TRT for Cosmic runs will be described as well as the procedures to ensure that the readout of the two detectors remained synchronous. Several tests were performed to see if the operation of the SCT (TRT) induced any noise in the TRT (SCT). The cosmic ray data are used to evaluate the SCT module and TRT straw efficiencies for MIPs and to verify that the noise occupancies are as low as expected from the calibration scans and from similar measurements in a controlled environment. This provides a critical test of the large-scale system performance of the

integrated barrel SCT/TRT and end-cap SCT/TRT detectors The cosmic ray data also provide key data for initial alignment studies with tracks, and the most recent results are summarised.

Summary:

TheBarrel and Endcap SCT detectors have been integrated into the barrel and Endcap TRT detectors in the CERN SR1 building. A large sample of cosmic ray data was acquired in SR1 and this was invaluable for understanding the system performance of these detectors. This also provided the opportunity for synchronous operation of the SCT and TRT and was therefore a critical test of the ATLAS DAQ system. A brief summary of the analysis of the SR1 cosmic ray data will be presented.

This talk will focus on the results of the first noise tests and cosmic ray data from the combined SCT and TRT runs after installation in the ATLAS cavern. These results provide the first determination for the noise performance of the SCT and TRT in-situ with the final electrical grounding scheme implemented. These results will be compared with data taken at earlier stages of detector integration. Several tests of the grounding scheme will also be discussed. Some tests were also performed to see if the SCT (TRT) operation induced any excess noise in the TRT(SCT).

The best indication of the performance of the SCT and TRT during ATLAS operation will come from the cosmic ray runs in the ATLAS cavern. A cosmic ray trigger will be provided by the ATLA S muon trigger system. A critical issue in a pipelined system is to time all the detectors in correctly. The procedures used for the SCT and the TRT will be reviewed and the results of timing scans used to verify the calculations will be discussed. Another critical issue for a pipelined system is to ensure that different detectors remain synchronized during a run and the tests used to check this will be presented. The cosmic ray muons will allow for the determination of the SCT module and the TRT straw efficiency for MIPs. At the same time this data will check that the noise occupancies in real operation is as low as that expected from the electronic calibration runs. This will therefore provide a critical system test for the operation of the full SCT/TRT systems.

The cosmic ray data will also be invaluable for the first alignment of the SCT and TRT detectors. The analysis of the SR1 cosmic ray data gave very encouraging results. More detailed studies will be possible with the new cavern cosmic ray data and since the detector is installed in its final location, any distortions measured will be representative of the operational system. As the muons will traverse the full SCT and TRT detectors, the alignment analysis will allow for the determination of some low frequency spatial modes of the detector which will not be constrained by pp data, such as sagitta distortions.

Parallel session A5 - Systems, Installation and Commissioning 3 (TK and Pix, Lumi) / 67

SCT Commissioning

Authors: Anthony Weidberg[1]; Maiike Limper[2]

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[2] *NIKHEF*

The Barrel and EndCap SCT detectors are installed in the ATLAS cavern. This talk will focus on the installation and first tests of the SCT in-situ. The thermal, electrical and optical services will be reviewed and some of the problems that were encountered during installation will be discussed. The first tests of the SCT in-situ will be described using the calibration scans.. The performance of the SCT will be described, with particular emphasis on the fraction of working channels and the noise performance. The effects of different grounding options have been studied. The noise occupancy has been studied in calibration and “physics” runs and the effects of the operation of the TRT have been evaluated.

Summary:

The barrel and EndCap SCT detectors have been installed in the ATLAS cavern. The electrical, optical and cooling services have been connected and an extensive programme of detector commissioning is underway. The first tests to be performed were the checks of the continuity of the electrical and optical

connections as well as the reliability of the cooling system. The module cooling is based on an evaporative system using C3F8 to remove up to 40 kW of heat. Any liquid in the exhaust pipes must be evaporated and raised above the cavern due point to avoid condensation, therefore heaters are installed in these exhaust lines. A vulnerability to moisture ingress was identified in these heaters during the first commissioning tests and the heaters have all been modified to fix this. The performance of the cooling system will be reviewed.

The access to the electrical and optical patch panels will become increasingly difficult during the course of the final stages of ATLAS assembly, so it was vital to make full tests and repairs while access was straightforward. A simple electrical test system was used to check the continuity of all electrical connections from the patch panels to the modules. A few cases of broken tracks on the Al Low Mass Tapes (LMTs) were discovered and all the critical faults were successfully repaired in-situ. All cases of connector problems and shorted wires were also fixed. The optical connections at the patch panels near the detector, were also fully tested. The continuity for the fibreTTC links were tested by measuring the currents in the p-i-n diodes in the on-detector opto-packages. The continuity of the fibre data links was verified by performing digital scans of the receiver threshold in the Back of Carte (BOC). A few non-functional links were recovered by cleaning the MT-12 connectors to remove dust. Many TTC links were operating at very low p-i-n currents which is not satisfactory for long-term operation, so a programme to produce better coupled VCSEL arrays is underway.

After the functionality of the services had been verified, the performance of the modules was studied. Firstly the parameters for the optical services were optimised to ensure reliable communication to the modules. Then simple digital tests were carried out to verify the functionality of the modules. Finally more detailed analogue scans were performed to measure the noise performance of the system. Threshold scans of the front-end discriminator were performed for different values of the injected charge. These could then be used to determine the gain of the front-end amplifier and the input noise. After setting the threshold DACs to values corresponding to 1 fC threshold, the noise occupancy in calibration mode and physics mode was measured. These results will be compared with similar data taken during macro assembly at Oxford, NIKHEF and CERN SR1. Various tests of the grounding system and effects of the simultaneous operation of the TRT will also be discussed.

The first results from cosmic ray tests of the SCT in the ATLAS cavern will be discussed. This work will be used to give a summary of the in-situ performance of the SCT.

Parallel session B1 - Trigger 1 Atlas / 69

The ATLAS Level-1 Central Trigger

Authors: Andrea Messina[None]; Attila KRASZNAHORKAY[1]; Christian Ohm[2]; David Berge[2]; Georges Schuler[2]; Herman Pessoa Lima Jr.[3]; Jose de Seixas[3]; Marcelo Perantoni[3]; Nick Ellis[2]; Per Gallno[2]; Per Klofver[2]; Philippe Farthouat[2]; Ralf Spiwoks[2]; Stefan Ask[2]; Stefan Haas[2]; Thilo Pauly[2]; Thorsten Wengler[4]

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The ATLAS Level-1 Central Trigger consists of the Muon-to-Central-Trigger-Processor Interface (MUCTPI), the Central Trigger Processor (CTP), and the Timing, Trigger and Control (TTC) partitions of the sub-detectors. The MUCTPI connects the output of the muon trigger system to the CTP. At every bunch crossing it receives information on muon candidates from each of the 208 muon trigger sectors and calculates the total multiplicity for each of six pT thresholds. The CTP combines information from calorimeter and the MUCTPI and makes the final Level-1 Accept (L1A) decision on the basis of lists of selection criteria (trigger menus). The MUCTPI and the CTP provide trigger summary information to the data acquisition system (DAQ) and the Level-2

trigger for every event selected at the Level-1. They further provide accumulated and, for the CTP, bunch-by-bunch scaler data for monitoring of the trigger, detector and beam conditions. The TTC partitions send timing, trigger and control signals from the CTP to the sub-detectors and receive busy signals which can throttle the generation of L1As. The Local Trigger Processors (LTPs) normally receive the TTC signals from the CTP but can also generate them locally. The LTP interface (LTPIF) modules allow to connect several LTPs for combined local running.

The MUCTPI, the CTP and most of the TTC partitions of the ATLAS sub-detectors have been installed in the ATLAS experiment and are being used for commissioning tests with the trigger processors on the input and several sub-detectors as well as DAQ and Level-2 trigger on the output. Results of operating the Central Trigger in the experiment using trigger information from trigger processors connected to sub-detectors observing cosmic rays will be shown.

Poster session / **70**

The ATLAS Level-1 Muon to Central Trigger Processor Interface

Authors: Attila Krasznahorkay[1]; David Berge[1]; Georges Schuler[1]; Nick Ellis[1]; Per Klofver[1]; Philippe Farthouat[1]; Ralf Spiwoks[1]; Stefan Haas[1]; Thilo Pauly[1]; Thorsten Wengler[1]

[1] *CERN*

The Muon to Central Trigger Processor Interface (MUCTPI) is part of the ATLAS Level-1 trigger system and connects the output of muon trigger system to the Central Trigger Processor (CTP). At every bunch crossing, the MUCTPI receives information on muon candidates from each of the 208 muon trigger sectors and calculates the total multiplicity for each of six pT thresholds. This multiplicity value is then sent to the CTP, where it is used together with the input from the Calorimeter trigger to take the final Level-1 decision. In addition the MUCTPI provides data to the Level-2 trigger and to the data acquisition (DAQ) system for events selected at Level-1. This information is used to define regions of interest (RoIs) that drive the Level-2 muon-trigger processing.
The MUCTPI system consists of a 9U VME64x chassis with a special backplane and 18 custom designed modules. Each of the 16 octant modules (MIOCT) receives and processes the muon candidate data from 13 sectors of the muon trigger detectors. It calculates the local muon candidate multiplicities and avoids double counting of muon tracks detected in overlapping sectors of an octant. The MIBAK backplane sums the multiplicity values of all MIOCT modules and also provides for readout data transfer and distribution of timing and trigger signals to all the modules in the chassis. The MICTP receives the external timing and triggers signals and sends the final multiplicity value to the CTP. The MIROD module collects information from the MICTP and the MIOCT modules and sends this data after formatting to the Level-2 trigger and the DAQ system via an optical S-LINK interface. The design of the modules is based on state-of-the-art FPGA devices and special attention was paid to low-latency in the data transmission and processing.
We present the design and implementation of the final version of the MUCTPI. Results from integration testing with the CTP, the muon trigger system as well as the DAQ and Level-2 systems including data from cosmic ray runs will also be shown.

Parallel session B6 - ASICs 3 future / **71**

The GBT, a Proposed Architecture for Multi-Gbps Data Transmission in High Energy Physics

Authors: Alessandro Marchioro[1]; Federico Faccio[1]; Jorgen Christiansen[1]; Ken Wyllie[1]; Kostas Kloukinas[1]; Paulo Moreira[1]; Sophie Baron[1]

[1] *CERN*

The future upgrade of the LHC accelerator, the SLHC, will increase the beam luminosity by a factor of ten leading to a corresponding growth of the amounts of data to be treated by the data transmission and acquisition systems. The development of the GBT ASIC addresses this issue providing a means to increase the bandwidth available to transmit the data to and from the counting room. The GBT architecture will provide the support to transmit simultaneously the three types of data required to run an experiment in a hostile radiation environment over a multipurpose link. This paper will describe the GBT architecture and some aspects of its detailed implementation.

Summary:

With the installation of LHC and its associated experiments approaching completion, CERN and its collaborating institutes are now considering an upgrade of the accelerator to achieve higher beam luminosity, the SLHC. Higher luminosity will bring the benefit of improving the statistical accuracy of the measurements but, it will also impose more stringent requirements on the performance of the data acquisition systems as well as on their radiation tolerant characteristics. Some of the systems and their components will have thus to be redesigned to cope with higher data rates and higher radiation levels. In particular the data transmission links will have to be upgraded to wider bandwidths in order to cope with the larger amounts of physics data being produced by the detectors. To increase the bandwidth without paying a penalty on the detector's mass budget it is necessary to use fewer optical links at higher data rates rather than simply increasing the number of links. The GBT ASIC architecture was developed under this perspective. It is target at high speed (~4 Gbps) data transmission between the detectors and the counting room and it aims at providing simultaneous transmission of physics, trigger and experiment control data over the same link. The GBT will act thus simultaneously as a data-link and as a TTC transmitter and receiver incorporating many of the functions that traditionally have been separated physically and functionally in data-acquisition, timing, trigger and slow control links. The GBT will implement point-to-point duplex links allowing bidirectional data transmission between the counting room and the detectors.

In other to simplify the development and maintenance of the links the GBT interface will adopt commercial standards like the Gbit-Ethernet. Moreover, the communications protocol to be adopted is constrained so that it will be possible to develop compatible firmware in most standard FPGAs existing today in the market.

Due to the beam luminosity increase, the total dose radiation levels that the on detector electronics will be exposed to are expected to increase in the same proportion reaching the 100 Mrad level for some of the inner detectors. These high levels of radiation will pose long term reliability problems due to total dose effects which can be minimized by using advanced CMOS commercial technologies and following special layout techniques previously developed for the LHC ASICs. The GBT IC will be thus fabricated in a commercial 130 nm technology which will ensure the required radiation tolerance as well as the capability to implement large bandwidth transmission circuits (~4 Gbps). The higher luminosity will also be linked to an increase of the Single Event Upset rates. SEUs are a major impairment to error free data transmission at high data rates. To deal with this situation the GBT adopts a robust error correction scheme that will allow to correct burst of errors cased by SEUs.

The paper will describe in detail the proposed architecture, the communications protocol and the forward error correction code used. The paper will also discuss some of the GBT circuits and in particular will describe the techniques used to deal with SEU in the high speed circuitry as well as the de-serializer and clock recovery circuits.

Poster session / **72**

The CMS Pixel FED

Author: Manfred Pernicka[1]

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The innermost detector of the CMS Experiment consists of 60 million silicon pixels. The hit data has to be read out and must be digitized, synchronized, formatted and transferred over the S-Link to the final CMS DAQ. The amount of data can only be handled because the readout chip (ROC) delivers zero-suppressed data above an adjustable threshold for every pixel.
The Pixel FED 9U VME module receives an optical analogue signal, which is subsequently digitized and processed. The position of the pixel on a module is transmitted with 5 symbols coded in 6 pulse height steps each. The data of 36 inputs from one event build a final event data block. The main challenge is that the information which arrives on the different inputs at the same time can be from different events and can differ up to 16 events depending on the number of hit pixels in past. That is possible because the ROC has a multi event memory and the input data length can be very different. Finally the information will be transferred over the S-Link to the CMS DAQ. Each module must be able to process more than 100 kHz trigger rate or if in trouble to send an alarm signal. The number of inputs is limited by the maximum data transmission rate of the S-Link (640 MB/s) for the expected high luminosity of LHC.
The data flow on the module is continuously controlled. Errors are written in an error memory, included in the data stream and if critical sent to the general CMS readout control.

Summary:

The signal of the pixel detector has to pass several steps before the arrival at the Front End Driver (FED). Initially it is a 40 MHz differential analogue signal. Inside the pixel detector it is transferred over cables and PCB traces to the optohybrid. The main intention was to keep material budget as small as possible, to include a cooling system for the hybrids and to have a minimum of signal reflections. Using a single-mode fiber, the signal is finally transferred to the FED. On the way it passes several connectors where uncontrolled signal attenuation occurs.
The pixel readout system consists of 40 PX-FEDs with 36 inputs each. The optical input signal is converted to electrical on the board. Adjustable current sources in the optical receiver are used to tune the output range. Furthermore a DC-DAC signal for every input allows optimal offset adjustment in the 10 bit range of the ADC. A fast DAC can create arbitrary input pattern for test purposes. We do not expect that the input signals are in phase to the clock, hence every input has its own clock, where the clock phase can be adjusted to the main clock in steps of 1.6 ns to select the optimum digitization sampling point for each input.
The data processing is done on Altera FPGAs, four at the front and one for final data block building as well as multi event storage. Each front Altera handles nine inputs. The first task is to synchronize the ADC data to the main clock and automatically adjust the pedestal of the incoming signals to a predefined value. This is absolute necessary, because the optical transmission system is strongly influenced by temperature. Each input has its own data processor. The data arrive at different times and have different length. A Readout Chip (ROC) at the front end can store up to 16 events. An average of 20 hits is expected with high beam intensities. The result is an event data block with primary header and trailer and stored in the first FIFO-1. If the data size is too big, the data stream is truncated and closed with a trailer. If the FIFO-1 is nearly full the data length is drastically reduced. A busy is sent to the general control system and an error message stored. A possible reason for such a condition could be problems with the pixel data threshold. A trigger signal together with an event number starts a readout process of one event, stored in the 36 FIFO-1.On the way to the next FIFO-2, where the data from 4 or 5 inputs are stored, the data are checked if the input event number correlates with that of the TTC system, once all data from each input has arrived after a certain time. A column histogram shows the distribution of the column numbers. All the errors are stored in a special error memory with some more information like input and event numbers. The error message is also transferred as error data to the event data and if absolutely critical, the error information is also sent over the TTS system to the general control system. With two data buses, each 64+4 bits wide, the event information of the eight FIFO-2 is collected in the final FIFO-3. On this path several spy FIFOs are included. Finally, the data are transferred to the CMS DAQ over the S-Link at 80 MHz.
The Pixel-FED board also includes two 32 bit bus systems controlled by VME. One has a length of approximately 65 cm and was a critical part because of crosstalk to the input signals and to each other because of the fast rise time of the drivers.
The VME data on board are clock synchronized and all logic blocks need a clock for proper functioning except the reset signal which is asynchronous. The inputs for the two data strobes, address and data and read/write decision have a digital filter for protection against noise and spikes.
No hang-up of the processing und storage system should be possible. The data transfer is as fast as the highest S-Link speed. The module was tested with 300 kHz trigger rate and short events. The BUSY signal was used to reduce the trigger rate when the S-Link was at the limit and the FIFOs nearly full. At

full luminosity, about 100 events of average size can be stored on board.
The module is composed of a mother board, nine ADC and five Altera daughter boards. Thus, the number of layers for the main board could be reduced to ten. The general design rule for fast signals was that one output drives one input (point to point connection). Most signal lines are serially terminated, which reduces the drive power significantly considering the wide parallel buses.

Parallel session A4 - Systems, Installation and Commissioning 2 (TK and Pix) / 73

Electronics and Trigger developments for the Diffractive Physics Proposal at 220m from LHC-ATLAS

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The instrumentation consists of two sets of Roman Pots installed respectively at 216 and 224m on both sides from the ATLAS IP to measure with precision the position (<10 micrometers) and the timing (< 5 picoseconds) of the two back to back diffracted protons tracks.
Each Roman Pot is equipped with several plans of edgeless silicon strip detectors read-out by a new version of the ATLAS SCT ABC chip with a longer latency (6.4 microseconds) and fast OR outputs defining a track segment.
These inputs are to be combined in time with the ATLASLVL1 trigger ACCEPT signal. In addition these tracks are time filtered with a very fast timing detector (MCP-PMT) allowing to constraint further at LVL2 the position of the IP within one millimeter precision. The description of the electronics and trigger system as well as the various technical issues associated with such challenging experiment (clocks, cabling, cooling, time monitoring) will be presented. Preliminary test results of the position and timing devices will be given.

Summary:

This should be done within the L1 CTP latency of about 2 microseconds leaving around 500 nanoseconds for the full digital logic, taking into account the particles flight path and transit cables from the roman pots stations. These information will be combined with two jets with a large Pt >20 Gev/c to make the L1 diffractive trigger. The implementation of the various electronics functional blocks and cables as well as the associated timing and data flow will be presented. At LEVEL 2, the full digitized information of all the silicon strips planes will allow a precise reconstruction of each track hits with a precision of 5 micrometers. In addition the timing information can be then fully used in order to insulate the relevant vertex with a precision of the millimeter or better.
We propose to measure also very precisely the time of flight of diffracted protons produced at the collision IP in specific devices placed in each roman pot. using these new micro-channel-plate photomultipliers in which the particles product Cherenkov light while traversing the window of one element in an array of area (e.g. 2,5 cm x 2,5 cm) .Recently, there has been a substantial improvement in the time resolution of MCP's, which have now achieved a 10 picoseconds transit-time spread (FWHM) for a single photon and 6 picoseconds for multiple photoelectrons. The basic principle of such detector is the following. A relativistic particle produces Cherenkov radiation in a crystal placed in front of the window of a PMT-MCP. This radiation is converted into electronsby a photocathode. The electrons produce a shower in the micro- channel plates, and the shower is collected by the anodes. After transmission through an impedance matched segment, the signal is detected from a central collector, and conveyed to an on-board chip in where it is digitized. The Cherenkov emission light has been simulated as well as the MCP response spectra for several commercially available MCP's, showing that a TOF resolution on the order of 1 picosecond should be attainable. This would allow separation of the different vertices with a resolution of less than one millimeter. It may also be possible to associate a photon with its production vertex by conversion directly in front of the MCP. The system we are considering requires a custom large-area MCP design with an anode consisting of impedance-matched segments, directly coupled to a circuit capable of psec resolution. This anode is made in a multipads structure of 4 by 4 elements with equal time transmission lines to connect to a common collection point input of the on-detector readout ASIC. A description of the readout electronics chain and its preliminary implementation will be given.

A full description of all technical system issues associated with such particular implementation will be presented including the radiation level and shielding, cooling, clocks distribution and timing stability monitoring, data flow and wiring.

Plenary session P4 / 74

SYNCHRONIZATION OF THE CMS CATHODE STRIP CHAMBERS

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The synchronization of the trigger and data acquisition systems for the Cathode Strip Chambers (CSCs) in the Compact Muon Solenoid (CMS) detector at CERN is described. To date, asynchronous cosmic ray data have been used to define the protocol and to refine timing algorithms, allowing synchronization to be realized within and between chambers. From this baseline, final synchronization of the CSCs will be readily achieved using data taken with the synchronous beam structure of the Large Hadron Collider. Details regarding the definition, procedures, validation, and performance of the synchronization of the CSCs will be presented.

Summary:

The synchronization of the trigger and data acquisition (DAQ) systems for the Cathode Strip Chambers (CSCs) in the Compact Muon Solenoid (CMS) detector at CERN is described. To date, asynchronous cosmic ray data have been used to define the protocol and to refine timing algorithms, allowing synchronization to be realized within and between chambers. From this baseline, final synchronization of the CSCs will be readily achieved using data taken with the synchronous beam structure of the Large Hadron Collider (LHC).

The CSCs comprise 468 chambers covering the full azimuth, divided into 4 stations on each endcap of the CMS magnet, interleaved between the magnet yokes to detect muons produced at polar angles between 1<|eta|<2.4. The chambers contain 6 layers, with radial cathode strips to measure the muons' azimuthal position and bend from the magnetic field in this region, and anode wires to measure their polar angle. The trigger electronics are custom-designed, using FPGAs to process information in boards located on the chamber, and in VME crates both on the periphery of the magnet yokes and in the counting house. The electronics were designed to process events at the LHC bunch crossing rate of 40MHz, to be highly configurable, and to recover quickly from single-event upsets which will occur in the high radiation environment. Inaccessibility to the electronics during collisions requires that remote communication protocol be used to set timing parameters and to monitor trigger performance.

Anode wire signals are used primarily to determine the timing of the event. Cathode strip signals are processed by comparator ASICs to specify the muon's location within a layer to a precision of ½-strip. The strip-positions from all layers are compared with patterns to pick muons with large momenta. A coincidence between the cathode and anode information is required for the trigger candidate to pass to the next step. Up to 2 trigger candidates per chamber are sent, of which 3 are chosen within a trigger sector to be sent on for further processing. These trigger primitive candidates are passed via optical fibers to a Sector Processor, which combines information from different stations through LookUp Tables in order to pick the most desirable candidate muons and measure their momenta. The CSC trigger candidate is handed to higher levels of the CMS trigger system to be chosen or discarded as a "L1Accept" event. A robust procedure to carefully synchronize the steps in a system of this magnitude and complexity is necessary.

Further requirements are imposed by the CSC DAQ system. In order not to choke the CMS DAQ with mostly empty data, the CSC DAQ was designed to send data from a chamber only when that chamber has created a trigger. The coincidence of a trigger coming from the CSCs together with the receipt of the L1Accept signal in the DAQ boards imposes further constraints to the synchronization of the system.

Details on the definition, procedures, validation, and performance of the synchronization of the CSC trigger and DAQ paths will be presented.

Topical 2: Detector Power Supply and Distribution 2 / 75

Serial Powering of Silicon Sensors

Author: Giulio Villani[1]

Co-author: Niko Partanen [1]

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Serial powering of silicon sensors will reduce the volume of power cables, the passive material and power losses in cables of future silicon trackers by large factors. These benefits are crucial for silicon tracking at the Super-LHC. Noise performance and grounding and shielding of densely packaged modules are key challenges for serial powering. We extended our studies with six ATLAS Semiconductor Tracker (SCT) modules to enable noise measurements in different geometrical configurations and for various sources of injected noise. We will present measurements obtained with a silicon strip supermodule. We will discuss the specifications of radiation-hard custom serial powering circuitry.

Summary:

Current silicon detector systems for particle physics and elsewhere power individual detector modules independently. For large scale detectors, like the ATLAS Pixel detector and the ATLAS Semiconductor Tracker (SCT), this implies that tens of thousands of cables are needed to power the front-end electronics. The power cables are well above 100 m long (one way) and their resistance (including return) can be as high as 4.5 ohms. The power consumed by the front-end electronics is typically tens of kW; power efficiency is as low as 30% -50% due to thermal losses in cables. For future detectors, with five or ten times more electronic channels, independent powering is not practical. Serial powering provides an elegant solution to these problems and is of great interest for SLHC and ILC trackers and elsewhere.
A serial powering system for silicon detectors consists of four basic elements: a current source; a shunt regulator and power transistor (for digital power); a linear regulator (for analog power); and AC or opto-coupling of clock, command and data signals. The modules are all chained in series. The number of long cables can thus be reduced by a large factor, depending on the number of modules powered in series. The power efficiency is increased hugely.

We have extended our previous results [1] on noise performance substantially to include the effects of the following noise sources: injection of a voltage pulse in the serial powering line and a fluctuation in the current - source current. We also built a dedicated set-up to position two SCT sensors at a close distance of a few mm and measured their noise performance. We built and tested a silicon supermodule with six sensors powered in series.

Failure protection modes have been identified and compared quantitatively with independent powering schemes. In one failure condition where the module would become disconnected from the regulator circuitry, the shunt regulator power device would have to withstand the full module current. We designed and tested circuitry to sense an over-current condition and to reduce the regulator output voltage to a minimum value to minimize thermal stress due to extra power dissipation.

Measurements taken in the various configurations will be presented and discussed. The focus will be on noise performance, which so far is excellent.

Currently custom radiation-hard serial powering circuitry is not yet available for implementation in silicon strip detector systems. We will present different alternative shunt regulator architectures. We will discuss the specifications of a general-purpose radiation-hard serial powering ASIC for tracking detectors at SLHC and elsewhere.

Serial powering is compatible with data communication of power lines. Time permitting, we will introduce a novel scheme for full-duplex bi-directional data communication in serial powering systems, which could be of interest for slow-control applications.

[1] Marc Weber, Giulio Villani, Robert Apsimon, "Serial Powering of Silicon Strip Detectors at SLHC", Proceedings of the 6th "Hiroshima" conference on Silicon detectors (2006), accepted by NIM A.

Parallel session B2 - Trigger 2 CMS and Atlas / **76**

Installation and Commissioning the CMS Regional Calorimeter Trigger Hardware into the CMS Level-1 Trigger

Author: Pamela Renee Klabbers[1]

Co-authors: Jessica Leonard [1]; Joseph Lackey [1]; Mathew Jaworski [1]; Monika Grothe [1]; Phillip Robl [1]; Sridhara Dasu [1]; Thomas Gorski [1]; Wesley H. Smith [1]

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The electronics for the Regional Calorimeter Trigger (RCT) of the Compact Muon Solenoid Experiment (CMS) have been produced, tested. The RCT hardware consists of 18 double-sided crates containing custom boards, ASICs, and backplanes. The RCT receives 8 bit energies and a data quality bit from the HCAL and ECAL Trigger Primitive Generators (TPGs) and sends it to the CMS Global Calorimeter Trigger (GCT) after processing. Integration tests with the TPG and GCT subsystems have been sucessful.

Installation is complete and commissioning of the final system is underway. During installation, pattern tests were used to validate 1026 TPG links and 108 GCT cables. Additionally, the RCT was part of several successive Global Runs, where an increasingly larger fraction of the full chain of the final Level-1 trigger system was tested. These tests, their results, and the RCT installation will be described.

Summary:

The electronics for the Regional Calorimeter Trigger (RCT) of the Compact Muon Solenoid (CMS) Experiment have been produced and the individual boards and crates validated. The RCT has been integrated with the ECAL and HCAL Trigger Primitive Generators (TPGs) responsible for RCT input and the Global Calorimeter Trigger (GCT) that receives the RCT output. The hardware of the RCT consists of eighteen 9Ux680mm double-sided crates containing custom boards with custom ASICs and backplane. Including spares, almost 1800 boards of 6 different types have been produced. Included are a backplane, Clock and Control Card (CCC), Receiver Mezzanine Card (RMC), Receiver Card (RC), Electron Identification Card (EIC), and Jet/Summary Card (JSC). This system receives 8000 calorimeter trigger tower transverse energies (ETs) and characterization bits from the ECAL and HCAL TPGs via 4 GBaud copper links. These ETs are summed over 4x4 tower regions for jet-finding, missing ET, and total ET. Additionally, the individual tower energies and characterization bits are used to find electron candidates. These quantities are then forwarded to the GCT via their source cards for further processing and sorting.

The RCT crates, cables and associated hardware have been installed underground and the commissioning of the final system is underway. RCT integration tests started with a subset of the Trigger Timing and Control (TTC) hardware for clocking and control and a portion of the ECAL and HCAL TPG hardware as input. At first, simple patterns were sent to validate timing between systems and link operation, and were captured with a RCT custom test board, the Jet Capture Card (JCC) in lieu of the GCT Source Cards. When the GCT Source Cards became available, the testing chain was extended and the JCC used to verify the patterns seen at the GCT and predicted by the trigger emulation software. These patterns included simulated electron and jet triggers to validate the system. As more crates were installed and the cabling finished up, these patterns became more complex and testing was automated.

Additionally, monthly Global Runs were started at the end of May 2007, each lasting for one full week. The purpose of these runs was to validate the system in parts, gradually working up to the final system.

The RCT joined these runs in June 2007, when a slice of the full calorimeter trigger chain was available. Timing in the subsystems, using software to automate the configuration and monitoring, and the previous integration were all crucial to the success of these runs.

Details of the installation, integration, and commissioning for CMS trigger will be described, as well as the results from participating in the monthly Global Runs.

Parallel session B1 - Trigger 1 Atlas / **77**

Commissioning of the Jet/Energy-sum and Cluster Processors for the ATLAS Level-1 Calorimeter Trigger System

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The ATLAS first-level calorimeter trigger is a hardware-based system designed to identify high-pt jets, electron/photon and tau candidates, and to measure total and missing Et. The trigger consists of a preprocessor system which digitises 7200 analogue inputs, and two digital multi-crate processor systems which find jets, measure energy sums, and identify localised energy deposits (electron/photon and tau candidates). In order to provide a trigger quickly enough, the hardware is parallel and pipelined.

Experience so far of the jet/energy-sum and cluster processor system production, commissioning, and integration into ATLAS will be described.

Summary:

The ATLAS first-level calorimeter trigger (L1Calo) is a hardware-based system with a high degree of adaptability provided by widespread use of FPGAs. The real-time path of the trigger is subdivided into a preprocessor (PPr) which takes analogue signals from the calorimeters and digitises them, followed by two digital processor systems working in parallel: the jet/energy-sum processor (JEP) and the cluster processor (CP). This contribution discusses the digital processor systems and their commissioning: the PPr is discussed in a separate contribution.

The input to both CP and JEP systems are 8-bit digitised transverse energy deposits covering either 0.1x0.1 (CP) or 0.2x0.2 (JEP) in eta-phi space. These signals are transmitted

to the CP and JEP systems over high-speed serial LVDS cables. The CP and JEP systems are each comprised of two parts: a parallel set of high-density processor modules - the CPMs and JEMs respectively - and a common merger module (CMM) which collates results and sends them to the ATLAS central trigger processor (CTP), which in turn makes the overall first-level trigger decision. Both CP and JEP systems take events at the bunch-crossing rate of 40 MHz, and are heavily pipelined. The CP and JEP processors are allocated about 400ns processing time (in parallel), as their share of the overall trigger latency. The CP occupies four 9U VME crates, the JEP two.

One of the principal challenges of the processor systems is the connectivity over the large eta-phi array of trigger towers, required in order to avoid double-counting of energy deposits. The main component that ensures this is a dense custom backplane with approximately 22 000 pins per crate.

The output from the CP system passed to the CTP consists of a set of multiplicities of electromagnetic (EM) objects passing flexible Et thresholds on shower energy as well as limits on activity in surrounding cells, and in the hadronic samplings behind the EM cells. A simple alteration of how hadronic samplings are used also allows triggering on isolated hadrons from tau decays. Co-ordinates and classifications of these candidates are also made available to the second-level trigger system via regions-of-interest (RoIs).

The output from the JEP system includes information about hadronic jets passing Et thresholds, in a similar scheme to that of the CP system. In addition, the total Et deposited in the calorimetry is found, as well as a vector sum of Et deposits; these are compared to thresholds and the results are passed to the CTP.

Production of the modules for the full-scale calorimeter trigger system has taken place during 2006-7, and installation and commissioning of the full system is taking place during the spring and summer of 2007. The installation of the processor systems into the ATLAS counting rooms is outlined, together with results of commissioning tests, and lessons learnt. Integration with the CTP, ATLAS DAQ systems and higher-level trigger systems is also in progress and will be discussed.

Poster session / **78**

R/O Device based on USB1.0 for Spectroscopy DAQ

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A novel read-out (R/O) device based on universal series bus (USB1.0) for spectroscopy data acquisition (DAQ) together with software controlling analog-to-digital converters (type of Canberra, model 8715) will be presented. The interface exploiting the USB1.0 standard has two advantages: USB1.0 is spread out on all platforms and almost computers are equipped with this communication port;

and, the speed of such devices (about 1Mb/s) is sufficient for spectroscopy with average number of events detected per second at the level up-to 50kHz. FTDI chips together with prepared software libraries of the Future Technology Devices International Ltd. were used for the realization of several examples of the read-out device. The response of the constructed devices was compared with the response of a Cicero multi-channel analyzer made by Silena. Equal devices were also tested using statistical tests with intention to verify their perfect functionality as well as their long-term stability. Results of these tests will be also presented.

Parallel session B4 - ASICs 1 FE chips / 79

Development of a selftriggered high counting rate ASIC for read-out of 2D gas microstrip neutron detectors.

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In the frame of the DETNI project a 32-channel ASIC suitable for readout of a novel 2D thermal neutron detector based on a hybrid low-pressure Micro-Strip Gas Chamber and solid 157Gd converter has been developed. Each channel delivers position information, a fast time stamp of 2 ns resolution and signal amplitude proportional to the energy. The time stamp is used for correlating the signals from X and Y strips while the amplitude is used for finding center of gravity of a cluster of strips. The timing and energy information are stored in derandomizing buffers and readout via token ring architecture.

Summary:

In the frame of the EU project DETNI (DETectors for Neutron Instrumentation) of NMI3 three hybrid 2D thermal neutron detectors for future high intensity pulsed neutron sources (like ESS) are developed. One of these detectors is a low-pressure Micro-Strip Gas Chamber (MSGC) with solid 157Gd/CsI converter suitable for applications in imaging, quasi-Laue diffraction, very high resolution single crystal diffraction and very high resolution focusing low-Q small angels scattering. The very demanding requirements of global counting rate of 10^8 cps and two-dimensional position resolution of 50-100 um FWHM over a detector segment area of 25x25 cm^2 covered with 400x400 strips can be met only provided that the readout electronics is realized as multi-channel Application Specific Integrated Circuits (ASICs).
Reconstruction of a neutron position requires timing, spatial and energy data from both (X/Y) detector planes. To extract these data, after the preamplifier each readout channel is split into a timing and an amplitude (energy) channel. The preamplifier incorporates a transimpedance amplifier with a folded cascode core and a switchable feedback loop employing bridged-T lowpass filter. One can choose between 5 different loops to cover possible variation of the internal multiplication gain of the detector. The timing channel consists of a fast shaper (Tp = 25 ns) and a comparator with a Time Walk Compensation circuit (TWC) while the energy channel comprises a slow shaper (Tp = 85 ns) and a classical peak detector and hold circuit (PDH) which detects the peaks of incoming pulses and holds their values for a given time period controlled with respect to the response of the comparator in the fast timing channel. To compensate the threshold offsets on the channel basis, each comparator is equipped with a 5-bit trimming DAC.
The output signal from the timing channel is used to latch a 14-bit time stamp with 2 ns resolution and to enable the PDH circuit in the energy channel. The 14-bit time stamp signature is combined of a 12-bit Gray-encoded counter (TS<13:2>), a toggle flip-flop (TS<1>) and the buffered input clock (TS<0>). The correct timing of bits TS<1> and TS<0>, to ensure Gray encoded of all 14 bits, allows us achieve 1 ns resolution at 250 MHz clock frequency.

The output signals from the PDH and the time stamp are stored in analogue and digital derandomizing buffers (four-stage FIFOs), respectively. The readout of the memories is performed via a token-ring based multiplexer which ensures data sparsification, so that only non-zero data are read out from the buffers.
The MSGCROC ASIC has been designed and manufactured in the 0.35um CMOS process from Austria Microsystems. The dimensions of the ASIC are 3.2×6.7 mm^2.
In the paper we present the functional architecture and critical aspects of the ASIC design, results of electrical testing as well as examples of physical measurements.

Poster session / **80**

Track momentum discrimination using cluster width in silicon strip sensors for SLHC.

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The cluster width of a particle crossing a silicon strip (mini strip) detector can be exploited to measure its transverse momentum when the strips are parallel to the B field. This suggests the discrimination of the clusters widths to filter the majority of low momentum particles.
Once performed directly on the detectors, such discrimination can be used both for low level trigger (L-1,L-2) and for data reduction. This approach is discussed in the context of a first level trigger based on Tracker for SLHC.
The quality of the measurements and their discrimination capability are discussed with respect to the geometry of the sensors and to the detectors layout. Electronics issues and constraints are also reviewed.

Parallel session B3 - Trigger 3 / **81**

A first-level track trigger architecture for Super-CMS

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We present a first architectural study of a first-level hardware track trigger for CMS at SLHC. The design of a hardware track trigger at 10^35cm-2s-1 is challenging. A primary constraint on implementation will be power consumption within the detector, in turn driven by the data transmission bandwidth to off-detector electronics. We therefore emphasise the minimisation of the data flow through local filtering of track candidates on the detector. The architecture presented does not comprise a stand-alone track trigger, but uses identified muon and calorimeter trigger objects to seed track-matching within an integrated first-level system.

Summary:

The Super-LHC (SLHC) proposal would increase the luminosity of the LHC machine by a factor of ten, to 10^35cm-2s-1. Since this is also likely to require a change to the bunch structure of the machine,

the incoherent background in the LHC detectors could exceed that observed at LHC by up to a factor of twenty. The ability to trigger efficiently on high-pt physics signatures, with good control of rate, is therefore of paramount importance, and it is clear that the first-level hardware trigger systems designed for LHC will need to be upgraded. One promising route to maintain trigger performance is to incorporate tracking information into the first-level hardware trigger decision. Algorithms including track information for refinement of trigger object identification and pt measurement are already in use in the very first stages of the CMS high level trigger. Data bandwidth (and the associated on-detector power consumption) is likely to be a key constraint in the implementation of such a hardware system. We present here an architecture combining several elements of on-detector and off-detector data reduction, while preserving sufficient track information to maintain the performance of the muon and calorimeter triggers at a similar level to that expected at LHC. We do not propose a full stand-alone track trigger, but maintain the concept of triggering primarily on lepton, photon and jet objects. The proposed architecture makes use of the stacked detector layer concept defined in previous design studies, allowing an effective geometric pt-cut on track candidates. An on-detector data reduction step is performed on track stubs found in two such layers, using outer and inner radius detector stacks; this step includes the flagging of track stub multiplicity, allowing a simple isolation criterion. The final inter-stack correlation step is performed off detector after seeding by candidate objects from the muon and calorimeter systems, allowing a substantial reduction in the required data processing capacity. This system also has the potential for further rate reduction by correlation of the z-vertex of trigger objects in multi-object signatures.

Topical 2: Detector Power Supply and Distribution 2 / 82

The implementation of the power supply system of the CMS silicon strip tracker

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The power supply system of the silicon strip tracker of the CMS experiment provides HV bias and LV power to the 15 thousand silicon modules comprising the detector, arranged into 1944 “power groups” and 256 “control rings”.
Around 1200 power supply modules, disposed on 29 racks, operate in a “hostile” radiation and magnetic field environment, 10 m away from the beam crossing region. They power the detector through ~50 m long custom-designed “Low Impedance” cables, adopting the sensing technique to compensate the voltage drop. Separate board models are deployed for detector power groups and control rings. The required 48V power is provided by AC-DC converters installed on the same racks.
This paper reports the experience with the implementation of the system, which requires a careful study of the rack layout, grounding scheme, power budget, heat dissipation on racks. Comprehensive Quality Assurance and burn-in programs ensure the performance of the system, establishing the protocol, shared with the board’s manufacturer, for acceptance tests and failure detection.

Poster session / 83

Design of an integrated particle detector-cell based on latchup effect

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The paper describes a novel approach to detect particles by means of an integrated device susceptible to latchup effects; it is proposed as a powerful means of achieving the precise detection and positioning of a broad range of particles with a micrometer spatial resolution. The cell is designed using state-of-the-art AMS 0.35 micron BiCOMS technology. We show the design of a mixed-mode

Bipolar-MOS circuit that is going to be fabricated and tested. Previous investigations indicate that the recognizable charge might be comparable to that collected into to-date detectors. The idea is proposed for possible a implementation as beam monitor or ion-selector in future high-energy experiments.

Summary:

Here is described a novel approach to detect particles by means of a solid-state device susceptible to latchup effects [1]. The stimulated ignition of latchup effects caused by external radiation has so far proven to be a hidden hazard. Here this is proposed as a powerful means of achieving the precise detection and positioning of a broad range of particles with a micrometer spatial resolution. The basic latchup circuit is built up of a two-transistors positive feedback loop that provides a current amplification and an output latch, all in one. Here the cell is designed using state-of-the-art AMS 0.35 micron BiCMOS technology. In particular, a mixed-mode Bipolar-MOS circuit is designed and it is going to be submitted. The circuit is basically composed of a p-channel bipolar and a n-channel MOS transistors, plus some biasing resistors. The choice of the transistors are based upon the technology features and models. These devices show a good latchup ignition after a charge injection. After this, the sensitive cell retains the position of the crossing particle by means of a self-locked thyristor-like component that provides, digital, robust and stable signal until the whole system has been powered off. During the ignition, the cell's output signal does not depend on the input deposited charge, provided it is over threshold and capable of making the positive feedback current loop start. Conversely, the output voltage of the circuit saturates towards ground level in any case as the two transistors are forward biased. In addition, the charge here is collected only in the base-emitter, for the bipolar, and gate, for the MOS, regions of the transistors. For this reason, in principle, a thick detector is not required. Previous investigations [2-3] indicate that the recognizable charge might be comparable to that collected into to-date detectors. In fact, a prototype made up of discrete components was realized and exploited and the tests with daylight, electrons, via a current pulse generator and with a laser beam showed a charge sensitivity of the order of 1 pC. It is expected to scale the charge sensitivity with an integrated version of the prototype. According to the features described above, the application fields may range from beam monitors, where high radiation hardness is required, to heavy ion selectors where tunable sensitivity is crucial.
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Parallel session B4 - ASICs 1 FE chips / 84

Test results on the n-XYTER ASIC, a self triggered, sparcifying readout ASIC

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n-XYTER is a 128 channel asynchronous, self triggered, self sparcifying readout ASIC developed as a front-end for neutron scattering detector applications. Due to the novel architecture it has attracted a considerable interest from future heavy ion experiments around the FAIR project. In particular for CBM and PANDA, n-XYTER is currently seen on one hand as the basis and starting point for a dedicated ASIC development on its own. On the other hand it will serve as the prototype readout electronic front-end for broad detector prototyping efforts that have just started and will span from silicon strips to gas detectors.
The first dies of the n-XYTER ASIC are currently under thorough and intensive tests, so that the

test results on operation and performance will be presented. Further, an outlook for FAIR related applications will be given.

Summary:

Increasing demands for readout channel numbers as well as general rate capability finally iniciated a push for on-chip integration of front-end electronics
in the thermal neutron scattering community as well. The typical neutron scattering application introduces the additional challenge of generally asynchronous, poisson distributed events. To address the statistical nature of neutron events, a novel self triggered, entirely data driven, derandomizing and sparsifying readout architecture was developed and cast in silicon as a 128 channel neutron detector readout chip. The analogue pre-amplifier and shaping circuit was designed for a noise performance below 1000 ENC at 30 pF input capacitance. The ASIC provides readout bandwidth for an average signal rate of upto 32MHz, where pulse hight, time of incidence and channel number are registered. Though engineered for a specific application, these specifications correspond perfectly well to the demands imposed upon a front-end when MIPs are to be detected in typical silicon strips.
Additionally, the data driven and sparcifying readout architecture turned out to attract considerable attention in the heavy ion community of the future FAIR project, where mere event rates and multiplicities due to signal latencies impede the installation of any low level trigger facilities. n-XYTER has grown to be the readout ASIC prototype for FAIR and
in particular the CBM as well as the PANDA experiments. It will on one hand serve the basis for a dedicated ASIC development and on the other hand it will be employed for the broad detector prototyping efforts that have just started.
The first dies of the n-XYTER ASIC are currently under thorough and intensive tests, so that the test results on operation and performance will be presented.

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Parallel session A7 - Systems, Installation and Commissionning 6 / 85

The TOTEM Front End Driver, its Components and Applications in the TOTEM Experiment

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The TOTEM Front End Driver or TOTFED receives and handles trigger building and tracking data from the TOTEM detectors, and interfaces to the global trigger and data acquisition systems. The TOTFED is based on the VME64x standard and has deliberately been kept modular, very flexible and programmable to deal with the different TOTEM sub-detectors and possible evolution of the data treatment and trigger algorithms over the duration of the experiment. The main objectives for each unit are to acquire on-detector data from up to 36 optical links, to perform fast data treatment (data reduction, consistency checking, etc...), to transfer to the next level of the system, and to store data on request for slow spy readout via VME64x or USB2.0. The TOTFED is fully compatible with CMS and permits TOTEM to run both standalone and together with CMS. The TOTEM Front End Driver, its components and applications in the TOTEM experiment are presented in this paper.

Summary:

The TOTEM experiment has three sub-detectors: Roman Pots (RP) with silicon strips, T1 detector with Cathode Strip Chambers (CSC) and T2 with Gas Electron Multiplier detectors (GEM). All detectors use the VFAT chip [*] for tracking and trigger generation and use the same data readout system based on the TOTEM Front End Driver or TOTFED. The TOTFED consists of the following physical units: the "VME64x Host Board", the "OptRX12" (a 12 channels at 800Mbps optical receiver card) and the "S-Link64" transmitter card. The TOTFED hardware was developed in collaboration with the CMS preshower, where TOTEM developed the HOST board, and the CMS preshower the optoRX. Each TOTFED consists of one host board and a maximum of three optical receiver cards and three transmitter cards. These three channels are independent and can send data to the data acquisition system at 200MBps each. The merger unit on the board allows collecting data from all the channels, performing additional data reduction and treatment and sending it via the fourth "S-Link64" to the event builder. This feature enabled its use for the CMS preshower data handling (the Preshower Data Concentrator Card "ESDCC"). Slow readout for spying the stored data from the corresponding memory is implemented via VME64x interface and four independent USB2.0 interface channels. There are additional user defined interfaces on board for future usage. The system makes use of the latest generation of FPGA components. The modularity and the programmability of the FPGAs make the TOTFED extremely flexible for different applications. Within TOTEM a number of TOTFEDs will be used to receive and process the trigger building data from the three sub-detectors. In standalone operation this system will generate the level 1 trigger signal and during operation in conjunction with CMS it will transfer a limited number of trigger building signals to the CMS global trigger system. The TOTFED can also be used to send a programmed data stream for testing purposes. The presentation will give a detailed overview of the design of the components of the TOTFED, and its application in the TOTEM experiment.

[*] VFAT documentation reference

Topical 3: Detector Power Supply and Distribution 3 / **86**

Low Voltage Power Supply Incorporating Ceramic Transformer

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A low voltage power supply provides the regulated output voltage of a few volts from the supply voltage around 48 V. The low voltage power supply incorporates a ceramic transformer which utilizes piezoelectric effect to convert voltage. The ceramic transformer isolates the secondary from the primary, thus providing the ground isolation between the supply and the output voltages. The ceramic transformer takes the place of the conventional magnetic transformer. The ceramic transformer is constructed from a ceramic bar and does not include any magnetic material. So the low voltage power supply can operate under a magnetic field.

The output voltage is stabilized by feedback. A feedback loop includes an error amplifier, a voltage controlled oscillator and a driver circuit. The amplitude ratio of the transformer has dependence on the frequency, which is utilized to stabilize the output voltage.

The low voltage power supply is investigated on the analogy of the high voltage power supply similarly incorporating the ceramic transformer. Stability of the power supplies is studied from the theoretical viewpoint of stability. It is shown that the compensation, which has been applied to the high voltage ceramic transformer, could work similarly for the low voltage power supply.

Summary:

The article describes a low voltage power supply incorporating a ceramic transformer. The low voltage power supply provides the regulated output voltage of a few volts from the supply voltage around

48 V. The ceramic transformer utilizes piezoelectric effect to convert voltage. The ceramic transformer isolates the secondary from the primary, thus providing the ground isolation between the supply and the output voltages. The ceramic transformer takes the place of the conventional magnetic transformer. As the ceramic transformer is constructed from a ceramic bar and does not include any magnetic material, there is no leakage of magnetic flux such that it can be operated under a magnetic field. An inductance element is needed to obtain efficient voltage conversion, being implemented by an air-core coil that can also be operated under a magnetic field.

When energy is stored in inductance L loaded with resistance R, the time constant is L/R. To maintain voltage across the resistance, energy is injected into the inductor at switching time intervals roughly equal to the time constant. Accordingly, a large resistance increases the switching frequency. Since the load resistance of power supply tends to be large, the inductance is a good energy reservoir for the low voltage power supply. It might be difficult to implement the ground isolation between the supply and the output voltage without the magnetic transformer. Yet the magnetic transformer can not work in a magnetic field.

When energy is stored in capacitance C, the time constant is RC such that the switching time required maintaining voltage becomes longer as the resistance increases. The capacitance is therefore a good energy reservoir for the high voltage power supply. The piezoelectric ceramic transformer stores energy as mechanical vibration, with energy dissipation at the load decaying the vibration. The transformer is similar to capacitance in that the time constant of the decay is proportional to load resistance. In this sense, the low voltage power supply incorporating the ceramic transformer is similar to the charge-pump power supply. But it is difficult for the charge pump power supply to implement the ground isolation.

Many Japanese manufactures compete in development of the low voltage power supply employing the ceramic transformers. Main objective is miniaturization of power supplies. The competition is keen due to a large market of power supplies miniaturized in size. The power supply of a laptop computer is so far a small box placed outside the computer. The box is to be replaced with the card that can be inserted into the slot of the laptop computer. Yet such the card-size power supply is not yet available so far.

The ceramic transformer reduces the power supply in size mainly for the following two reasons. Firstly power density of the ceramic transformer is more than five times larger than that of the conventional magnetic transformer. Secondly the ceramic transformer can be operated efficiently at high frequencies where the conventional magnetic transformer increases in loss.

From the viewpoint of the ceramic transformers for the power supply operating in a strong magnetic field, it is not so important to reduce the size. To moderate the requirement for size brings large freedom to the design of the ceramic transformer. Following the view of an expert in the ceramic transformer, further studies are unnecessary to manufacture the low voltage ceramic transformer operating in the magnetic field. A manufacturer is ready to supply such the ceramic transformers if there is enough demand.

Such the ceramic transformer is not yet commercially available. So we have no chance to learn the low voltage ceramic transformer by experience. Yet manufacturers have already accumulated a lot of experience and knowledge about the low voltage power supply employing the ceramic transformer. No manufacturer has put such the power supply to market. Price might be a problem or there may be difficulties which we have not yet understood.

The output voltage of the power supply is stabilized by feedback. A feedback loop includes an error amplifier, a voltage controlled oscillator and a driver circuit. The feedback mainly utilizes the frequency dependence of the amplitude ratio of the ceramic transformer which depends on the driving frequency whose range is designed to be higher than the resonance frequency of the ceramic transformer. The feedback increases the driving frequency when the output voltage is higher than a reference voltage at the input of the error amplifier. Similarly, the driving frequency decreases when output voltage is lower than the voltage specified by the reference voltage.

The stability of the low voltage power supply is studied by analogy with the high voltage power supply similarly incorporating the ceramic transformer. The compensation, which has been applied to the high voltage ceramic transformer, could work similarly for the low voltage power supply. Simulations based on a lumped-constant equivalent circuit for the ceramic transformer are extensively utilized to understand the compensation. Responses of the power supply are simulated into details. Hopefully we could compare the simulations with the responses of a practical circuit and report its efficiency and

performance.

Parallel session A2 - Optoelectronics / **87**

Radiation-Hard Optical Link for SLHC

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We study the feasibility of fabricating an opto-link for the SLHC ATLAS silicon tracker based on the current pixel optio-link architecture. The electrical signals between the current pixel modules and the optical modules are transmitted via micro-twisted cables. The optical signals between the optical modules and the data acquisition system are transmitted via rad-hard SIMM fibers fusion spliced to rad-tolerant GRIN fibers. The link has several nice features. We will present measurements of the bandwidths of the transmission lines, irradiated PIN and VCSEL arrays, and optical packages of novel design, plus the design of new optical driver and receiver chips using the 0.13 μm process.

Summary:

The SLHC is designed to increase the luminosity of the LHC by a factor of ten. In the present ATLAS pixel detector, the electrical signals between the pixel modules and the optical modules (opto-boards) are transmitted via ~ 1 m of micro twisted cable. The optical fiber ribbons consist of 8 m of rad-hard SIMM fibers fusion spliced to 70 m of rad-tolerant GRIN fibers. We currently transmit optical signals at 80 Mb/s and expect to transmit signals at ~ 1 Gb/s at the SLHC. The design of the present pixel optical links has several nice features: 1) Since the optical components are mounted on patch panels instead of directly on the pixel modules, the radiation exposure is much reduced. 2) The separation of the opto-boards from the pixel modules decouples the production of both components and greatly simplifies their design and fabrication. 3) An optical package on a pixel opto-board couples to a removable and robust fiber ribbon terminated with an MT connector. For the SLHC, we would like to take advantage of the many years of R&D effort. If the present architecture can transmit signals at the higher speed, the constraint of requiring no extra service space is automatically satisfied.

We have measured the bandwidths of the transmission lines and the results indicate that the micro twisted-pair cables can transmit signals up to ~ 1 Gb/s and the fusion spliced fiber ribbon can transmit signals up to ~ 2 Gb/s. We have irradiated silicon PIN and GaAs VCSEL arrays with 24 GeV protons and find at least one candidate PIN and one VCSEL array that can survive to the SLHC dosage. We plan to irradiate more silicon and GaAs arrays this sumer. In addition, we plan to irradiate GaAs PIN arrays from three vendors. The results will be presented at the conference.

We previously designed the optical driver and receiver chips using the 0.25 μm process. We are in the process of converting the chips for operation at the much higher bandwidth using the 0.13 μm process. The chips are expected to be submitted for fabrication in a MWP run in the fall. We will present the design of the new chips together with the results from the simulations.

Topical 2: Detector Power Supply and Distribution 2 / **89**

The CMS Low Voltage System

Author: Sergei Lusin[1]

[1] *Fermilab*

The low voltage system for the on-detector electronics of the CMS Experiment comprises 12090 channels of low voltage power supplies, requiring 1182 KVA of power at the entrance to the CMS facility at CERN.

The severe radiation environment inside the CMS experimental cavern combined with an ambient magnetic field reaching up to 1.3 kGauss at the detector periphery severely limit the available choices of low voltage supplies, effectively ruling out the use of commercial off-the-shelf DC power supplies. Typical current requirements at the CMS detector front end range from 1A-30A per channel at voltages ranging between 1.25V and 8V. This requires in turn that the final stage of the low voltage power supply be located within ~10m of the front-end electronics, that is, on the detector periphery.

Power to the CMS front-end electronics is stabilized by a 2 MVA UPS located in a CMS surface building. This UPS isolates the CMS detector from disturbances on the local power grid and provides for 2 minutes of autonomy following a power failure.

This talk will describe the architecture of the CMS Low Voltage system as well as the considerations that went into its design.

Summary:

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The severe radiation environment inside the CMS experimental cavern combined with an ambient magnetic field reaching up to 1.3 kGauss at the detector periphery severely limit the available choices of low voltage supplies, effectively ruling out the use of commercial off-the-shelf DC power supplies.
The preparation for data-taking at the LHC experiments required a dedicated development effort on the part of two vendors specializing in equipment for high-energy physics, in coordination with the electronics design staff of the individual experiments.

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The CMS detector is quite large, having a diameter of 15m and a length of 21.5m. It is built around an iron yoke weighing 12500 tons, part of which supports the cryostat of a 4 Tesla superconductiong solenoid. This yoke functions as the main structural element of CMS and serves as the flux return path for the solenoid.

The detector is segmented into 13 sections. The central section (which supports the solenoid) is stationary, while the others can move up to 10m in the longitudinal direction. This allows the detector to be opened up for access to subdetector assemblies mounted on and inside the yoke. All cables to the 12 movable sections pass through articulated cable chains in trenches beneath the detector. The cable paths between the on-detector electronics and the power distribution area in the service cavern (adjacent to the CMS detector and shielded from it by concrete) are typically 100m-140m in length.

Power to the on-detector power units is supplied via these cables at voltages of 385VDC or 230VAC and 380VAC three phase, depending on the system. No neutral is distributed. The on-detector systems convert between input power at several hundred volts to an output between 1V and 8V in one step or two, depending on system architecture.

Power to the CMS front-end electronics is stabilized by a 2 MVA UPS located in a CMS surface building. This UPS isolates the CMS detector from disturbances on the local power grid and provides for 2 minutes of autonomy following a power failure, allowing for an orderly shutdown of detector electronics and controls.

Following the UPS stage, power is fed to the underground power distribution area, which contains isolation transformers, static compensators, distribution switchgear and banks of rectifier units providing 385VDC, as well as electronics for monitoring and control of the system.

This talk will describe the architecture of the CMS Low Voltage system as well as the considerations that went into its design.

Parallel session A6 - Systems, Installation and Commissioning 4 (Lumi, MU) / 90

Development and Commissioning of the CMS Luminosity Monitor

Author: John Jones[1]

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We discuss the development and commissioning of a luminosity monitor. It is based on hardware that provides real-time histograms of data from the forward hadronic (HF) calorimeters in CMS. Measuring the total energy deposition and occupancy in these detectors allows us to calculate the relative instantaneous luminosity of the collider on a bunch by bunch basis also useful for machine diagnostics. Once calibrated with measurements from the LHC we will be able to make the first proton-proton inelastic cross-section measurement. The methods for achieving this will be discussed, as well as the readout hardware design and implementation details.

Summary:

Luminosity monitoring is a critical component of any particle physics experiment, allowing one to compute the cross-section for the physical processes occurring in the detector. The luminosity measurement in CMS will be used to monitor the LHC beam and provide overall normalization for physics analyses. For off-line analyses in CMS, the design goal is a systematic accuracy of less than 10% for a range of beam luminosities from 1028cm-2s-1 to 1034cm-2s-1.

The CMS luminosity monitor is a system based on a mezzanine card called the HLX, mounted on the HCAL Trigger and Readout (HTR) board. It operates by histogramming data from the HTR boards for the forward hadronic (HF) calorimeters in CMS, which provide coverage from a pseudorapidity of 3 to 5 in both CMS end-caps. It computes both energy sums and counts of the number of physical towers below a preset energy threshold for this region, both of which can be extrapolated to measure luminosity. Combined with a careful off-line study, both the delivered and recorded luminosity can be measured. Using smaller sets of data, the real-time behavior of the system will be monitored online.

Parallel session A2 - Optoelectronics / 91

Optical absorption in commercial single mode optical fibers induced by gamma rays and complex radiation fields

Author: Thijs Wijnands[1]

Co-authors: Jochen Kuhnhenn [2]; Luit Koert De Jonge [1]; Stefan Hoeffgen [2]; Udo U. Weinand [2]

[1] *CERN*

[2] *Fraunhofer INT – Institut Naturwissenschaftlich Technische Trendanalysen*

The optical absorption in 13 SM fibers from 6 manufacturers was studied as a function of dose, dose rate, light power, wavelength and temperature. Two pure Si-core fiber exhibits extreme low radiation induced absorption.

Summary:

Introduction

In the 27 km long LHC tunnel, some 8000 kilometers of single mode optical fibers are being installed for accelerator controls and for beam instrumentation. Most of these fibers will be exposed to low or intermediate levels of radiation (approximately 1-10 Gy per year). Around 85% of the fibers are made

of Germanium doped (Ge-doped) silica from Draka Fibre Technology BV hereafter referred to as the "Draka 445755" fibre. This is a standard communication fiber, manufactured using the Plasma Chemical Vapour Deposition (PCVD) process. Initial optical absorption measurements during irradiation with with rays from a 60Co source [1] showed that the remnant attenuation for light at a wavelength of 1310 nm is linearly depended on the total absorbed dose and equal to 0.01 dB Gy-1 km-1 at least up to doses of some 100 Gy. In large majority of the accelerator tunnel, radiation induced attenuation is therefore not an issue.

Approximately 1300 fibers in the LHC tunnel (representing a total of 2500 km fiber length) will be exposed to much higher dose rates of 50 kGy per operational year (180 days) [2]. The total ionizing dose in these areas is deposited by various types of particles at different energies and such a radiation field is referred to as a complex high energy radiation field. The use of the standard Draka 445755 optical communication fiber in these areas is excluded because the attenuation of light at 1310 nm would reach approximately 25 dB per operational year and largely exceed the 7 dB/km power budget limitation imposed by accelerator controls applications and by beam instrumentation.

This paper reports on the joined efforts from CERN and Fraunhofer INT and to find a large quantity of commercially available single mode optical fiber with a constant quality and an optical absorption not exceeding 7 dB per km for light at 1310 nm after a total dose of 500 kGy in a complex radiation field.

Experimental

Sample screening test

Test procedure

All irradiation tests have been carried out with a calibrated 60Co source at Fraunhofer INT (TK1000 Gammamat) in accordance with the IEC 60793-1-54 specifications [3] and at room temperature (24–28°C). The light from the laser diode light source (LD Profile 1310) is divided by a coupler to a reference and measurement channel. The reference channel compensates drifts of the light source. The fiber samples are wound up on aluminum spools to assure homogenous irradiation by the point source on the centre of the spool. The light transmitted via the fibre samples and via the reference channel is measured with a high precision dual channel optical power meter (HP 8153).
Before each irradiation, the system stability in terms of noise and drift is verified. During irradiation, the noise and drift observed via the reference channel was always inferior to 1% of the total induced loss. By varying the length of the samples, the total induced loss after irradiation in each sample was kept between 2 and 5 dB. By limiting the total attenuation in the samples during irradiation, a good compromise is found between the signal to noise ratio in the measurements on the one hand and the light power of the measurement channel on the other. The total uncertainty in the optical absorption measurements presented here is estimated to be below 5%.

Attenuation measurements at constant dose rate

Seven commercial companies were contacted and invited to participate in the radiation screening test for the LHC project. Eventually 12 fiber samples from 6 different manufacturers were obtained, including the standard Draka 445755 communication fiber already installed in other parts of the LHC tunnel. The other glass silica based fibers had a Ge-doped core (2 fibers), a pure silica core (4 fibers) or no information from the manufacturer was given on the composition of the fiber core (5 fibers).
All samples were exposed to gamma rays under near identical experimental conditions. Only for one specific sample, the light power was increased from 10 microW to 40 microW to improve the stability of the measurement chain. It was later verified experimentally that photo bleaching effects in this specific fiber sample are negligible and that the variation of light power had no influence on the measurements. Figure 1 shows the induced loss in dB/km as a function of the dose for each of the fibers on a logarithmic scale (figure 1, left) and on a linear scale (figure 1, right). Amongst the Ge-doped fibers, the Draka 445755 standard communication fiber (black dotted curve) has the lowest induced loss. The pure silica core (PSC) fibers show a lower induced loss as compared doped silica fibers which is in agreement with previous experimental observations [4]. Sample #7 (PSC) and #12 show a remarkably low attenuation for light at 1310 nm above a total dose of 4 kGy.

Figure 1: Induced loss in dB/km as a function of the dose for each of the fibers in the screening test (double logarithmic scale on the left, linear scale on the right). Ge-doped fibers are plotted with dotted lines, pure silica core (PSC) fibers are plotted with solid lines and the samples with an unknown composition are plotted with dash-dot lines.

Dose rate dependence studies

To study the radiation induced loss under conditions closer to those expected for the LHC, the optical absorption of 1310 nm light was also measured at different dose rates. Samples #6, #7, #11, #12 and the Draka 445755 sample were irradiated up to a total dose of 100 kGy at dose rates varying between 0.02 Gy/s to 3.1 Gy/s.

Figure 2: Variation of the optical absorption as a function of the dose rate for sample #7 and #12 (double logarithmic scale on the left, linear scale on the right).

It was found that samples #7 and #12 again showed the lowest absorption of light at 1310 nm for all dose rates. In general, all fiber samples showed an increase in attenuation with increasing dose rates as expected. However, sample #7 is an exception to this general observation. For this fiber, variations in the dose rate have a very small or even negligible impact, in particular at higher total dose (figure 2). Compared to the second best performing fiber (sample #12) the induced loss at 100 kGy in fiber sample #7 is approximately 10 times lower.

Similar results were obtained in other experimental conditions. In particular, it was found that varying the wavelength, the light power or the temperature had a very small impact on the radiation induced optical absorption in samples #7 and #12. In none of these experiments did the attenuation of light in sample #7 exceed the 4 dB/km.

Another remarkable result was obtained during isothermal annealing experiments. The radiation induced damage in fiber sample #7 annealed at the highest rate reaching a recovery of 80% with respect to the conditions before irradiation after 104 seconds.

Detailed tests in a pulsed, complex high energy field

Test procedure

Samples #6, #7, #11, #12 and the Draka 445755 fiber sample were equally irradiated in a complex radiation field in the primary target hall of the Super Proton Synchrotron (SPS) at CERN. The aim of this experiment was to compare the optical absorption induced by gamma rays from a 60Co source to that induced by secondary particles in a hadronic shower at very high energies (up to 450 GeV) and to quantify the possible beneficiary effects of short term annealing at room temperature in a pulsed radiation field of a high energy accelerator.
The radiation spectrum in the radiation test facility of the SPS [5,6] is very similar to that expected in the LHC tunnel but the dose rate is considerably higher which makes this area ideally suited for LHC baseline equipment testing [7]. In the SPS, fixed target beams are accelerated from 14 GeV/c to 450 GeV/c in 3 seconds and then dumped on various primary targets during a 5 second long extraction procedure. This process is repeated every 14.4 seconds 24 hours per day and 7 days per week which creates a pulsed radiation field in the test facility with an averaged dose rate of 0.15 Gy/hr and a peak dose rate of 0.3 Gy/hr. The dose rate to the fibers is measured on line with various types of ionization chambers [8] and a remote radiation monitoring system using Radiation Sensing Mosfets (RADFETs) [9].
Two independent systems were used to measure the radiation induced attenuation in the fiber samples on line during the mixed field radiation test. The first system is based on a planar wave guide system to distribute light of a very stable LED light source with cable leads to the fiber samples in the irradiation zone. The light is guided back and multiplexed with a high precision micro-electro-mechanical switch to an optical power meter. The second system is using a direct measurement with an optical time domain reflectometer (OTDR) connected to the same micro-electro-mechanical switch. During the test, all components of the test setup are shielded from EM radiation and operated at a constant temperature.

Attenuation measurements

Samples #6, #7, #11, #12 and the Draka 445755 fiber sample were irradiated during the SPS proton campaign in 2006 during 120 days at a constant temperature of 26 degrees. Figure 3 shows the attenuation of light at 1310 nm as function of time (figure3, left) and as a function of the dose (figure 3, right). During this irradiation campaign, the total dose to the fibers is increasing at a constant rate except during the occasional technical stops of the accelerator. These stops are clearly visible in figure 3 (left) and are marked by the onset of an exponential decrease in the attenuation (annealing).

The total accumulated dose in this campaign is 512 Gy. These experiments will continue during the SPS proton campaign 2007 which is planned to begin on the 25th of May. We are confident to be able to

discuss the attenuation at higher total dose and to provide a comprehensive and complete comparison with the 60Co data at the conference.

Figure 3 : Radiation Induced attenuation of 5 selected fiber samples a pulsed, complex, high energy radiation field as a function of time (left) and as a function of the total dose (right).

Conclusions

In this study a commercially available SM fiber has been found that fully fulfills the requirements for the LHC. The radiation induced absorption of light at 1310 nm does not exceed the 4 dB/km at dose rates below 10 kGy per hour. In addition, the fiber shows exceptional annealing behavior. The fiber manufacturer of sample #7 is Fujikura Ltd. Japan (reference RRSMFB0602). The fiber is produced under very specific and tightly controlled circumstances using the standard Vapor phase Axial Deposition technique with Outside Vapor Deposition. Based on the results presented in this paper, CERN has recently purchased 2500 km of fiber length which is presently being prepared for installation in the LHC tunnel.

Provided the required corporate approval is obtained, data on the radiation induced attenuation of the series production samples will be presented during the conference together with the optical properties of the series production.

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Parallel session A2 - Optoelectronics / 92

Quality Control of the CMS Tracker and ECAL Installed Optical Cabling

Author: Daniel Ricci[1]

Co-authors: Alberto Jimenez Pacheco [1]; Francois Vasey [1]; Jan Troska [1]; Karl Gill [1]; Luis Santos Amaral [1]; Mohsin Abbas [1]; Robert Grabit [1]; Stefanos Dris [1]; Valeria Radicci [2]

[1] *CERN*

[2] *CERN (Imperial College)*

The readout and control optical links, developed for the CMS Tracker and ECAL at CERN, are approaching the final phase of the integration process at LHC Point 5. The individual component parts have been successfully integrated and connected at the innermost distributed patch-panels.

Currently, efforts are concentrated on the multi-ribbon optical cables installation and connection to ribbon cables at the dense, in-line optical patch-panel inside CMS and to the racks at the back-end patch-panel in the service cavern. Within the quality assurance programme, the quality control activities can give an online feedback during cable installation and provide an acceptance of the installed fibres. The final optical link lengths can also be measured as a precise input to the Tracker synchronization procedures. The recent integration experience and the quality control test system based on an Optical Time-Domain Reflectometer are described.

Summary:

The CMS detector is currently undergoing its final integration phase at CERN LHC Point 5. It includes the largest and densest fibre optic system in the world of its type. The inner Silicon Strip Tracker is read out and controlled by 43000 point-to-point optical links routed to three different patch panels: an inner (distributed) one, a dense intermediate (in-line) and a (distributed) backend patch panel. Similar optical links are used in the ECAL, preshower and pixels sub-detectors (about 15000 in total), as well as a smaller number links for RPC, BCM/BLT and TOTEM.
The integration of the optical components inside the sub-detectors has been completed and various tests have been made to check the functionality and the quality of the optical connections for the Tracker. In the Tracker case, the inner patch panel is now fully connected, the Tracker has been closed and the optical (12-fibre) fanouts have been carefully routed to the edge of the structure and there arranged, ready to be connected to the intermediate patch panel (PP1).
From PP1, situated in the central CMS barrel wheel (YB0), about 560 multi-ribbon (96-fibre) cables (120 for ECAL barrel) have to be connected and routed between the experimental (UXC55) and counting room (USC55) caverns. During the whole process, acceptance and quality tests have to be performed in order to validate the cable installation, give an assessment on the quality of the connections and measure the full optical link lengths, which are needed later for the synchronization of the Tracker.
In order to do this, a specific quality control procedure was defined, as part of the quality assurance procedure, and a test setup, based on a photon-counting optical time-domain reflectometer (OTDR), was developed.
The basic test principles of the instrument consist of injecting light of a certain wavelength and with a certain pulse repetition rate into the fibre to be tested, measuring the back reflection peaks. Reflections are typically due to a connection, a termination or a break in the fibre. Under certain conditions, also an estimation of the light-loss in the fibre and connection is possible.
During the trunk cable installation (pre-cabling), the time is an issue and the test system must be efficient and fast enough to allow the operator to work in the shadow of the ongoing activities. A novel method using the high resolution OTDR combined with a customized optical splitter module, with 12 parallel fibre channels of different lengths, allows separating the reflected signals coming from 12 fibre channels simultaneously.
Over 100 multi-ribbon cables have been installed and connected for testing the Tracker at CERN TIF. All of them were tested before and many (80%) after the connection, using the OTDR setup, with encouraging results: no cable was broken or damaged during the installation and, in all cases, it was possible to measure the lengths with a precision of 10cm or better.
Even though the test setup was developed basing on the Tracker cables configuration, it is flexible enough to be used also on the other subsystems as well as debugging tool during the Tracker integration activities.

Poster session / 93

ELMB Microcontroller Firmware and SCADA Integration for the LHCb Muon Detector Readout Control System

Author: Rafael Nobrega[1]

Co-authors: Davide Pinci [1]; F. Messi [2]; Francesco Iacoangeli [3]; Valerio Bocci [1]; Walter Rinaldi [2]

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The LHCb Muon Detector System will be equipped with about 1400 high efficiency chambers (Multi-Wire Proportional Chambers and Triple-GEM detectors) which will host a total of 7500 front-end boards, each receiving 16 readout channels and having 93 registers for access. A distributed PC network runs the supervision program and allows download of start-up settings and procedures, and upload of data logs. This document presents an outline of the LHCb Muon Detector Readout Control System and recent improvements regarding mainly the ELMB (Embedded Local Monitor Board) microcontroller firmware and the Supervisory Control And Data Acquisition (SCADA) system in use, PVSS.

Summary:

Hardware and software of the Chamber Readout Control System will be described. Control related data transfer is carried out utilizing CANopen between the host computer and control modules, and an I2C-like protocol based on LVDS for the connections with front-end boards. A distributed PC network runs the supervision program and allows download of start-up settings and procedures, and upload of data logs. A specific board (Service Board - SB) has been developed; it relies on Embedded Local Monitor Boards (based on a CAN controller and an ATMega128 microcontroller), allowing front-end circuitry monitoring and control by means of customized firmware development. In addition, the SB is provided with facilities as a flash-memory to data archiving and a radiation tolerant Actel FPGA, used mainly to generate test and synchronization pulses for front-end boards. The hardware control core is the ATMega128, a 8-bit RISC microcontroller. The microcontroller firmware is being implemented to fulfill the LHCb Muon requirements and many embedded procedures have been developed.
Each FEB contains 93 registers: as a consequence in total there will be more than 690000 byte wide registers in the LHCb Muon System which will be accessed by the SCADA system. For this reason, about 400 microcontrollers will be used and a server-client model communication system known as OPC (OLE for Process Control) is being used. It provides data-transfer between CAN devices and high-level software. The SCADA system in use has been chosen by CERN JCOP Group as a general solution for all LHC experiments. It is well adapted to large controlling systems, allowing manipulation of a high number of devices and registers by means of data acquisition, alarm handling, communication protocols, graphic user interfaces, etc.
A specific based SCADA system has been implemented for the LHCb Muon Detector with features which permit management of front-end by means of threshold calibration, auto-injection testing, chamber noise analysis, adjustment and initialization of front-end parameters, on-line monitoring, diagnostic procedures, data archiving and alarm handling. During data acquisition the system is capable of making decisions, correcting failures without human intervention, reporting changes and logging actions taken. In pre-acquisition state, users are allowed to alter parameters such as threshold, mask and signal width or check channels response and control noise rate. Such a control system has been modeled and implemented as Finite State Machine to be integrated to the LHC Experiment Control System. FSM hierarchical tree and states and actions for every control unit have been defined.

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Hardening ASICs against radiation effects

Author: Federico Faccio[1]

[1] *CERN*

Application-Specific Integrated Circuits (ASICs) designed for application in LHC experiments have to operate reliably in a severe radiation environment. This lecture will introduce the main reasons for failure of CMOS circuits in such environment, and how the sensitivity to radiation effects has evolved with the constant decrease of lithographic dimensions in CMOS manufacturing processes. Design techniques to protect the ASICs designed in commercial-grade technologies against radiation effects will be presented along with examples where they have been successfully used in the development of ASICs for the first generation of LHC experiments.

Parallel session B2 - Trigger 2 CMS and Atlas / 95

First Results on the Performance of the CMS Global Calorimeter Trigger

Author: Costas Fountas[1]

[1] *Imperial College*

The CMS Global Calorimeter Trigger(GCT) is the device within the CMS Calorimeter Trigger system which is assigned the tasks of finding and sorting forward, central and tau-jets, sorting isolated and non-isolated electron candidates and reading out all the calorimeter trigger data. The GCT system also provides for a cross-point switch which facilitates the connection between the Calorimeter and Muon Trigger systems. The GCT system uses 1.125 Gb/s optical links to concentrate the calorimeter data in eight processing cards and accomplishes the algorithm tasks by utilizing V2-Pro Xilinx devices. After a rapid development phase the GCT system has been produced and a large fraction of it has been installed at the CMS electronics cavern (USC-55). There it has been under test since March 07. Testing focused on two aspects of the GCT performance. First GCT was tested for synchronization and data transmission integrity using test pattern data injected in various places in the trigger chain. These tests aimed to establish that the GCT hardware performed as designed. Entire Monte Carlo events will also be propagated in the system to tests the algorithm performance. Results on the performance and testing of the GCT system at USC-55 are presented.

Summary:

Summary

The CMS Global Calorimeter Trigger (GCT) is an integral part of the CMS trigger system. Its function is to receive and process data from all 18 Regional Calorimeter
Trigger (RCT) crates and send the highest ranking electron and jet candidates to the Global Trigger, where they are used for generating the First Level Trigger Accept decision. This system has been designed to be modular in design as well as commissioning. Due to a compressed development schedule, it borrows heavily from existing designs.

The primary requirements of the GCT are to sort electron triggers, and generate and sort jet triggers. The design has been optimized for these tasks. Secondary requirements include jet trigger counters, total jet transverse energy trigger, total transverse and missing transverse energy trigger, luminosity monitoring, and RCT readout. The GCT is composed of four module types, the Source, Leaf, Wheel, and Concentrator cards.

Source cards receive input directly from the RCT crates, and transmit the data via multi-Gigabit optical links to the GCT crate. They are located in the same racks as the RCT,
and provide differential ECL to high speed serial conversion. In addition, they provide a means of data capture and readout for the RCT. The Leaf cards are configured to receive either electron or jet trigger data on high speed optical fibers. Each electron leaf card processes the electron data from 9 RCT crates, selecting the four highest energy candidates for further processing. Similarly, the jet leaf cards process data from 3 RCT crates, and forward the 4 highest energy jets to the Wheel cards. However, the jet finding algorithm implements a sliding window – which requires data from adjacent RCT crates (corresponding to adjacent physical areas on the detector). Jet leaf cards are linked to their neighbours in a corresponding fashion to facilitate this algorithm. The Wheel cards are only used for processing jet data, and combine the output of 3 Leaf cards. These 3 Leaf cards process the data from 9 RCT crates, or ½ of CMS. The Wheel cards sort the jets generated by the Leafs, and forward the 4 with the highest energy to the Concentrator. The Concentrator card accepts data from 2 electron Leaf cards and 2 Wheel cards. It performs the final sorting of both electron and jet events, and sends the 4 highest energy candidates of each type to the Global Trigger. In addition, it provides a VME interface (slow control interface), and S-link data acquisition interface for the entire system.

Over the past year a major part of the GCT has been manufactured and installed at the CMS electronics room, USC-55. Half of the source Cards (30) have been installed in 6 crates at the USC-55 along with 2 Leaf cards and one Concentrator card. This system represents the final CMS electron trigger plus a large fraction of the Jet triggers. This system has undergone detailed testing and is in the process of being integrated in the CMS Trigger chain. This talk will focus on results from tests for synchronization, the performance of the trigger algorithms, and bit error rate tests which were preformed in the period between March and August 2007. The experience acquired from manufacturing, integrating and testing such a trigger system will also be discussed.

Plenary session P1 / **96**

Introduction and Welcome

Plenary session P1 / **97**

Particle Physics in the Czech Republic

Author: Vaclav VRBA[1]

[1] *Institute of Physics, ASCR, Prague*

Several Czech universities and research institutes pursue active research in the field of particle physics. An overview of this research with the stress on experimental and instrumentation aspect will be presented.

Plenary session P1 / **98**

Organization

Author: Zdenek Dolezal[1]

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Plenary session P1 / **99**

The LHC machine status, commissioning plans and interface with the experiments

Author: Daniela Macina[1]

[1] *CERN*

The status of the ongoing Large Hadron Collider (LHC) installation is described with particular attention to the Long Straight Sections around the experiments. A summary of the present beam commissioning schedule will be given with some details on the beam conditions during first collisions. The second part of this talk will address in detail the experiment protection system from beam failures (including interlocks) and the exchange of data and control signals between the accelerator and the experiments.

Plenary session P1 / **100**

The Time Projection Chamber for the ALICE Experiment

Author: Luciano Musa[1]

[1] *CERN*

ALICE will search for evidence for quark-gluon plasma, the state of matter which is believed to have existed just after the Big Bang, in head-on collisions of lead-ions at the LHC. This requires a very precise tracking capability to record the paths of thousands of particles produced in the collisions. ALICE is therefore built around the largest Time Projection Chamber (TPC) in the world. The task of large acceptance tracking in a heavy ion experiment is similar to that encountered in the NA49 and STAR experiments at the SPS and RHIC respectively. However, the extreme multiplicities of ion collisions at the LHC set qualitatively and quantitatively new demands making new designs indispensable. The construction and assembly of the ALICE TPC were completed in 2006. Before being lowered to the underground experimental area, an extensive commissioning was carried out with cosmic rays and tracks produced by a UV laser system. In January 2007, the TPC was transferred into the ALICE underground area, where it will be put into service by summer 2007 to be ready for first collisions in spring 2008. This paper presents an overview of the main components, with special focus on the front-end and readout electronics, and some of the most crucial aspects addressed by the R&D activities that have preceded the design and construction of the ALICE TPC. The commissioning, including preliminary results from the analysis of data on noise, electron diffusion, drift velocity, and spatial resolution, will be also presented.

Plenary session P2 / 101

Fault-tolerant and radiation-hardened SPARC processors

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The paper will describe the development and status of radiation- hardened SPARC processors. The SPARC architecture was adopted by the European Space Agency (ESA) in 1992, and has since then been the baseline for most Eropean space missions. SPARC-based processor such as ERC32 are used to control many satellites, including the International Space Station. Newer devices based on the LEON acrhitecture are being developed, and are available on both radiation-hardened ASIC and FPGA technologies. A summary of availble LEON devices and software development tools will be provided in the paper.

Plenary session P2 / 102

Field-programmable technology: today's and tomorrow's

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The latest field-programmable technology, with enhanced processing, storage and interface capacity, enables the development of powerful and flexible systems that can be customised for specific applications and operating conditions. This presentation describes recent field-programmable systems and tools which have been developed to optimise design quality and designer productivity, and illustrates their use in various application domains such as real-time data analysis, facilities for

high-speed networks, and Monte Carlo simulation.
The issues addressed include: how to make the best of today's field-programmable technology, and what can we expect of tomorrow's field-programmable technology?

Parallel session A2 - Optoelectronics / 103

Joint ATLAS-CMS working group on optoelectronics for SLHC: Status Report

Parallel session A3 - Joint ATLAS-CMS working group on optoelectronics for SLHC / 104

WGa (lessons learned)

Parallel session A3 - Joint ATLAS-CMS working group on optoelectronics for SLHC / 105

WGb (radiation & reliability)

Parallel session A3 - Joint ATLAS-CMS working group on optoelectronics for SLHC / 106

WGc (reference chain)

Parallel session A3 - Joint ATLAS-CMS working group on optoelectronics for SLHC / 107

Discussion

Plenary session P3 / 108

Electronics and Sensor Study with the OKI SOI process

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We are evaluating SOI (Silicon-On-Insulator) technology for radiation-hard electronics and monolithic radiation sensor applications. The process we used is a 0.15um CMOS, fully-depleted SOI technology developed by OKI Electronics Industry Co. Ltd.
This SOI device has two Si layers; one is a thick substrate (handle wafer) which is Czochralski high-resistivity silicon, and another is SOI layer which is 40nm thick, low-resistivity silicon. Those Si layers are separated by a 200nm thick buried oxide (BOX) layer.
The SOI layer is used to implement standard CMOS circuits. Although the handle wafer is normally

just a physical structure in the SOI device, we developed a process to create p-n junctions in the handle wafer and connect them to transistors in SOI layer. Thus the handle wafer can be used as a radiation sensor.
Since there is no mechanical bonding between the sensor and electronics, the capacitance of the sensor node is very low and it has excellent sensitivity to irradiation. By thinning the handle wafer, we can make low-material pixel detectors.
We submitted first test designs at the end of 2005, and had successful results of test chips consisting of a 32x32 pixel detector, strip detectors and front-end electronics chips. At the end of 2006, we then performed our own MPW (Multi Project Wafer) run by collecting 17 different designs from US and Japanese universities/laboratories.
The OKI SOI process and the results from this MPW run are presented.

Plenary session P3 / 109

3D System Integration for high density interconnects

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3D-Integration is a promising technology towards higher interconnect densities and shorter wiring lengths between multiple chip stacks, thus achieving a very high performance level combined with low power consumption. This technology also offers the possibility to build up systems with high complexity by combining devices of different technologies. Ultra thin silicon is the base of this integration technology. The fundamental processing steps will be described, as well as appropriate handling concepts.
Three main concepts for 3D integration have been developed at IZM. The approach with the greatest flexibility, called Inter Chip Via - Solid Liquid Interdiffusion (ICV-SLID), is introduced. This is a chip-to-wafer stacking technology which combines the advantages of the Inter Chip Via (ICV) process and the solid-liquid-interdiffusion technique (SLID) of copper and tin. The fully modular ICV-SLID concept allows the formation of multiple device stacks. A test chip was designed and the total process sequence of the ICV-SLID technology for the realization of a three-layer chip-to-wafer stack was demonstrated. The proposed wafer-level 3D integration concept has the potential to build multi-layer high-performance chip stacks and is well suited as a replacement for embedded technologies based on monolithic integration. To address yield issues, a wafer-level chip-scale handling is presented as well, to select known-good dies and work on them with wafer-level process sequences before joining them to integrated stacks.

Topical 1: Detector Power Supply and Distribution 1 / 111

System aspects of the ILC-electronics and power pulsing

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The detector development for the ILC experiments is driven by the bunch structure of the accelerator, short trains with long empty intervals, and high granularity of the detector. This requires the electronics to be integrated into the active detector volume.
This talk exemplifies the concept for the electronics aiming for mechanical compactness through the CALICE-calorimeter. ASIC's nearby the active cells store the signals while the train and multiplexed data are transfered to the DAQ during the intervals between trains on a few signal lines. The compactness also requires components to be integrated into thin PCB's.
The compactness and complexity of a system is also defined by the infrastructure. Therefore the concept aims for low power consumption to avoid active cooling. This can be reached by power pulsing synchronous to the train structure.

Topical 1: Detector Power Supply and Distribution 1 / 112

ATLAS SCT Power Supply System

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The ATLAS SCT (semiconductor tracker) comprises 2112 barrel modules mounted on four concentric barrels of length 1.8m and up to 1m diameter, and 1976 endcap modules supported by a series of 9 wheels at each end of the barrel.

Each module is powered by its own independent, floating low and high voltage power supplies, referenced to ground at the detector shield. Correspondingly each module has its own, distinct cable chain all the way back to the service cavern.

This presentation outlines the structure and specification of the SCT Power Supply System, including the high level control software and operational model.

Summary:

In the ATLAS service caverns, the SCT power supply system comprises a total of 22 racks. In addition to standard units such as the turbine, deflector and heat exchangers, each rack contains two power pack shelves, one circuit breaker box (CBB), four fan trays and four SCT power supply crates. Each power supply crate services up to 48 SCT modules. It houses 12 LV cards of four channels each, 6 HV cards of 8 channels each, one SCT Interlock Card (SIC), one Crate Controller card (CC), and one shorting card (for safety reasons).

Each LV channel provides analogue and digital power to one module, as well as two low current control lines, bias for two NTC thermistors used to monitor the module temperature, and bias for the on-detector part of the opto-electronic readout scheme. Sense wires are provided for all high current lines. Each HV channel provides up to 500V bias to the silicon sensors of one module. Both LV and HV supplies may be controlled, and monitored parameters may be readout, by means of a parallel bus implemented on the crate backplane.

Power input to the LV and HV cards is at 48V DC, supplied by four commercial units housed in the power pack shelves. All units are connected to a common bus, power being distributed to the crates through minature circuit breakers housed in the CBB. Only three power packs are needed to power four fully loaded crates: the fourth power pack provides redundancy. At each LV/HV card, an oscillator block modulates the 48V DC input: each channel is isolated by means of a transformer. Each group of four channels is associated with a hardware interlock line, electrically isolated by means of opto couplers on the SIC card, to provide a safety interlock which does not depend upon software.

The crate controller interfaces an ELMB card to the crate backplane to provide a link between the power supply channels and CAN bus. Three user defined sets of channel parameters, corresponding to operational states of the detector, are stored in the ELMB's non-volatile memory such that common operations may be performed with a minimum of bus traffic.

The highest levels of the SCT Power Supply software take the form of a Supervisory Control and Data Acquisition system, PVSS II. The software is distributed between 9 PCs, 8 systems each being connected to 11 PS crates over CAN bus.

The top layer solution for the overall control of ATLAS takes the form of a Finite State Machine (FSM) written in SMI++. Accordingly an FSM has been built following the operational model of the SCT power supplies, with channels grouped together according to the physical

cooling structures of the detector. The physical routing of the SCT power cables dictates that, in many cases, the PS channels servicing the modules of a single cooling structure are distributed amongst several PS crates. This has added greatly to the complexity of the control software.

Topical 2: Detector Power Supply and Distribution 2 / 114

Power distribution for SLHC trackers: challenges and solutions

Author: Marc Weber[1]

[1] *Rutherford Appleton Laboratory*

Current silicon detector systems power each detector module independently. For large-scale detectors like the LHC trackers, tens of thousands of cables are needed to power the front-end electronics. At the price of added material, the conventional independent powering is just manageable. For the SLHC trackers, with a five- to ten-fold increase in the number of electronic channels and increased total current, independent powering becomes prohibitive. Solving the power distribution problem is a major challenge, which must be met to make tracking at SLHC possible. I will give an overview of alternative power distribution concepts, summarise the current R&D activities and discuss power distribution requirements from a system perspective.

Parallel session A7 - Systems, Installation and Commissionning 6 / 115

The TOTEM electronics system

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TOTEM is an LHC experiment around the same interaction point as CMS. It contains cathode strip chambers (CSC) and gas electron multiplier detectors (GEM) in the CMS cavern and 24 Roman Pots with silicon strip detectors in the LHC tunnel. TOTEM should run both standalone and together with CMS, and should be fully compatible with CMS. All three sub-detectors provide level one trigger building signals and use the same chips: VFAT2 providing both tracking data and fast trigger generation signals, the programmable Coincidence Chip, and the LVDS repeater chip. The same counting room hardware receives and handles both trigger building and tracking data.

Summary:

TOTEM is an LHC experiment in construction around the same interaction point as CMS. The cathode strip chambers (T1) and the GEM detectors (T2) are two gas detectors located within the CMS cavern. Four groups of six Roman Pots with silicon strip detectors are mounted in the straight sections of the LHC tunnel on both sides of the interaction point at 150 and 220 m distance.

The TOTEM electronics system is fully compatible with CMS. Limited manpower, resources and time imposed significant standardization with the same chips for all three sub-detectors and the same hardware in the counting room for data acquisition and level 1 trigger generation.

The TTC system was adopted with the CMS specific TTCci card. The slow control system of CMS tracker/ecal is used with the CMS FEC-CCS card and the CCU token ring. All programmable chips on the TOTEM detector have been equipped with an I2C interface which can be connected to the CCU.

The TOTEM experiment requires all three sub-detectors to participate in the trigger building with a high degree of flexibility. To realize this, three new chips (the VFAT2, the Coincidence Chip and the LVDS repeater chip) were designed in a collaboration with C4i funded by the Departement de la Haute Savoie and produced in a single run. All were designed using special layout techniques for total radiation dose tolerance, with additional measures for robustness against single event upsets.

The VFAT2 front end ASIC provides tracking and trigger building data and can be configured to match the geometry of the three different sub-detectors. It also contains a special circuit to protect itself against gas discharges.

The Coincidence Chip provides on-detector coincidences to reduce the trigger data sent to the counting room. Both VFAT and Coincidence Chip are programmable through their I2C interface and include counters on the fast trigger outputs to monitor hit rates.

Both trigger building and tracking data are optically transmitted to the counting room using the GOH hybrid. The Roman Pots at 220 m from the interaction point are too far removed for the optically transmitted trigger data to arrive within the allowed latency and electrical transmission was adopted. The LVDS repeater chip is inserted at regular distances along the 270 m long cable and preserves the electrical signals.

The HOST board in the counting room with opto-receiver mezzanines receives both trigger and tracking data. This was a shared development: the CMS preshower designed the opto-receiver mezzanine and TOTEM the HOST board. The fully CMS compatible system is equipped with SLINK, USB and VME interface. The level 1 trigger generation is also carried out by HOST boards. Trigger building signals can be sent to the CMS global trigger or a level 1 trigger signal can be generated directly for TOTEM standalone operation.

In conclusion, the TOTEM electronics system, fully compatible with CMS, became possible through standardization across its sub-detectors, adopting the same hardware for trigger building and tracking data, the collaboration with the CMS preshower, and the support of the Departement de la Haute Savoie for the collaboration with C4i.

Topical 3: Detector Power Supply and Distribution 3 / 116

Topical Discussion

Plenary session P4 / 117

ILC Detector R&D

Author: Marcel Demarteau[None]

Although the LHC will explore the energy frontier, and is destined to provide new insights in the fundamental understanding of matter and space-time, it has its intrinsic limitations. The proposed International Linear
Collider (ILC) will add significantly to the scientific program of the LHC. This, however, can only be realized if the experimental challenges of the ILC can be overcome. The detectors at the ILC are envisioned to be precision instruments and are a far extrapolation in performance and technology from the current generation experiments. This talk will discuss some of the critical detector R&D that is needed to bring about a successful ILC physics program.

Plenary session P1 / **118**

Distributed Power Architectures for Computing Systems

Author: Giorgio Spiazzi[1]

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Nowadays computing systems comprise a large number of different processing equipment (servers, routers, etc.) with a total power consumption up to some megawatts. In these applications system-level issues like system and component architectures, modeling, control, power management, overall efficiency are of major concern.

Different distributed power architectures are firstly reviewed, together with the most important converter topologies employed. Then, a particular emphasis is dedicated to the discussion of the Voltage Regulator Modules (VRMs) and their specific aspects. Finally, the future trend and applications of integrated digital controllers in distributed architectures, both at power management level and at the IC controller level, are discussed.

MicroElectronics User Group / **119**

MUG

Close out / **120**

Close out

Tutorial 1 / **121**

Hardening ASICs against radiation effects

Tutorial 2 / **122**

Robust ASIC designs for hostile environments

Co-author: Herman CASIER [1]

[1] *IEEE*

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Executive summary

Author: Francois Vasey[1]

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