Design of on-chip data sparsification for a mixed-mode MAPS device

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The device described in the paper is built up of a bidimensional matrix of MAPS, already designed and fabricated in the past by the SLIM5 Collaboration, and of an off-pixel digital readout sparsification. The readout logic is based on std-cells and implements an optimised token-like technique. It is aimed at overcoming the readout speed limit of future large-matrix pixel detectors for particle tracking, by matching the requirements of future HEP experiments. In particular, the readout architecture extends the flexibility of the MAPS devices to be also used in first level triggers on tracks in vertex detectors.

Summary

The paper describes the design of a mixed-mode ASIC that implements a matrix of MAPS cells along with a digital readout sparsification circuit. The design has been carried out within the SLIM5 Collaboration and it is aimed at overcoming the readout speed limit of future large-matrix pixel detectors for particle tracking, by matching the requirements of future HEP experiments. In particular, the readout architecture extends the flexibility of the MAPS devices to be also used in first level triggers on tracks in vertex detectors. The MAPS cells have been fabricated and tested in the past years with different layout flavours and now this ASIC includes readout capabilities. Plus, the mixed-mode design approach extends the performance of the chip as both the matrix and the readout logic have been developed separately and, lately, integrated together. In particular the matrix of MAPS has been described with a VHDL-Verilog model and used as a macro-cell block within a bigger digital design. The global place-and-route has been also digitally designed. The design is implemented via the STM 0.13mm CMOS digital technology. Let's give a brief functional description of the readout logic. The matrix of pixels is grouped into regions of 16 pixels (macro-pixels). Each region is activated and frozen via dedicated wires while the reset and readout phases are carried out via wires that are shared over the whole matrix. The dedicated wires may also be masked, one by one, in case they would be too noisy or burned, to avoid reading not-significant hits at any readout phase. At a given time, for example when a bunch-crossing signal is provided, the columns of macro-pixels that own at least one hit are seen via fast-or wires and frozen. The coordinates of these columns are associated with a time-stamp, whose buffers are located outside the matrix. Then, one at a time, the columns are enabled and the macro-pixels'output data are written on a readout bus. Once the column of pixels has been readout it is set free. Then the process moves to another column. The readout phase involves one column of macro-pixels at a time and this leaves the rest of the matrix free and capable of detecting new hits. Thus, the matrix may own hits, along with their personal time-stamps, belonging to different bunch-crossings. During the readout phase the matrix is swept and all the hits belonging to a given bunch are readout, reset and set free. The process continues till all the macro-pixels have been readout. All these capabilities have been designed into a single die composed of a large full-custom matrix of pixels that is readout via a standard-cell based digital circuit.

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