MAPS in 130 nm triple well CMOS technology for HEP applications

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Abstract

Deep N-well CMOS monolithic active pixel sensors (DNW-MAPS) represent an alternative approach to signal processing in pixellated detectors for high energy physics experiments. Based on different resolution constraints, two prototype MAPS, suitable for applications requiring different detector pitch, have been developed and fabricated in 130 nm triple well CMOS technology. This work presents experimental results from the characterization of some test structures together with TCAD and Monte Carlo simulations intended to study the device properties in terms of charge diffusion and charge sharing among pixels.

I. Introduction

Recently the properties of monolithic active pixel sensors (MAPS) have been intensely investigated by several research teams involved in the development of detectors for particle physics experiments. Their monolithic structure, featuring a few μm thick superficial active volume, makes them interesting for applications to experiments at the future high luminosity colliders (International Linear Collider, Super B-Factory). In particular, deep N-well (DNW) MAPS, whose basic structure is shown in Fig. 1, make use of a buried N-type layer, available in modern triple-well deep submicron CMOS processes, as the charge collecting electrode and, instead of the classical three transistor readout scheme [1], [2], employ a charge sensitive amplifier to perform signal amplification [3].

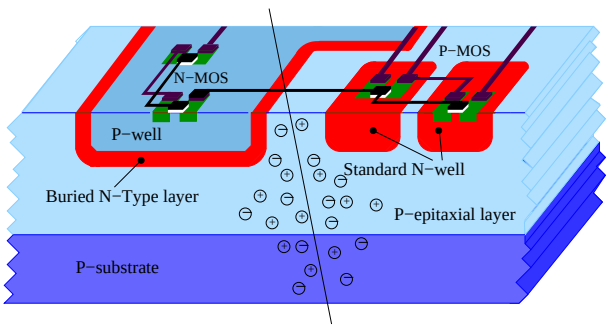

Figure 1: simplified structure of deep N-well MAPS. N-MOS transistors can be housed inside the sensor while P-MOS transistors are integrated in standard N-wells.

The use of a DNW as the collecting electrode makes it possible to lay out all of the N-channel transistors belonging to the front-end electronics over the sensor area, therefore reducing the impact of the electronics itself on the detector fill factor. In order to fully exploit the potential of complementary MOSFET processes and include also PMOS transistors (which need to be integrated in standard N-wells) in the design of the pixel level electronics, without significantly degrading the collection efficiency, the sensitive element has to take up a significant fraction of the elementary cell surface. The above described approach results in an increased functional density which may be exploited to add a filtering stage and some simple logic blocks to the charge preamplifier. These guidelines have been followed in the design of different prototype chips fabricated in 130 nm epitaxial, triple well CMOS processes provided by STMicroelectronics. In the following sections two different MAPS topologies, developed for different spatial resolution constraints, are presented. This work is aimed to discuss results coming from device simulations and from the experimental characterization of the devices in terms of charge collection and charge sharing among the pixels. Simulations have been performed with the TCAD suite provided by Synopsys and with a Monte Carlo code specifically developed to simulate random walk of minority carriers in an undepleted detector substrate. A laser source, operating in the infrared region of the electromagnetic spectrum, has been employed for the experimental characterization of the MAPS test chips.

II. The test chips for the Apsel series MAPS

A set of test chips, called Apsel (Active Pixel Sensor ELectronics) and including single pixel structures and MAPS matrices, has been designed in the STM 130 nm CMOS technology. Results from the test of the Apsel0 and Apsel1 chips have already been published [3], [4], while a new generation of test chips, Apsel2M and Apsel2T, are currently available for experimental characterization. Pixel-level front-end electronics in the Apsel2 chips, as well as in the previous prototypes, includes all the blocks of a typical readout channel for capacitive detectors i.e. a charge preamplifier and a shaping stage and is suitable for the design of detectors with a pitch in the 50 μm range. Peaking time in the shaping filter can be programmed to assume one of the following values: 0.5 μs, 1 μs or 2 μs. Fig. 2 shows a schematic view of the elementary cell geometry integrated, almost without any modification, in all of the Apsel family chips.

All the experimental results shown hereafter refer to a 3×3 matrix, surrounded by a ring of dummy pixels, which is integrated in the Apsel2T chip. In such a matrix each of the 9 shaper outputs is available at a LEMO connector on the test board.

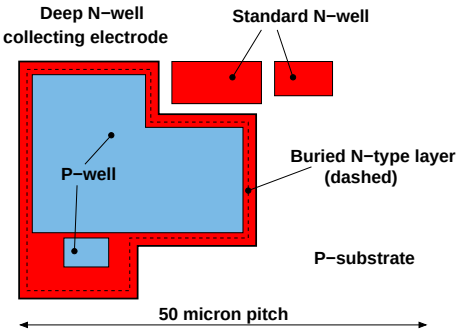

Figure 2: top view of the Apsel2 elementary cell layout. The two standard N-well, housing the PMOS transistors, are signifi cantly smaller with respect to the deep N-well collecting electrode in order not to degrade the detection effi ciency.

A. *Laser source tests*

In order to investigate the properties of the DNW MAPS sensor, a low power InGaAs/GaAlAs/GaAs laser source, operating at a wavelength λ of 1060 nm, has been used. The experimental apparatus includes the laser source, a Newport universal motion controller and a LeCroy Waverunner 64Xi digital storage oscilloscope, included in a fully automatic system controlled by means of a NI Labview (release 8.2) virtual instrument. A single mode coupler operating at 1060 nm and a fiber optic focuser, providing a spot diameter close to 20 μm are also included in the optical setup. The need for an automatic setup arises from the relatively large number of incident points necessary to perform a full characterization of a 150×150 μm^2 matrix with an incremental step, along both the X and Y directions, not larger than 5 μm. As a consequence each scan procedure featured 961 test points. In order to avoid reflection from the thick net of metal interconnections on the top side of the die, samples were back-illuminated. Since the absorption coefficient in silicon at λ=1060 nm is about 12 cm^{-1} and the device thickness is 254 μm, pulses with an energy close to 200 fJ are required to emulate a minimum ionizing particle (MIP) at the die surface where the detector lies.

Table 1: charge sensitivity values from laser source tests.

Pixel	Charge Sensitivity [mV/fC]
1_1	614
1_2	610
1_3	540
2_1	573
2_2	576
2_3	500
3_1	565
3_2	600
3_3	534

In the central pixel of the matrix a purposely integrated 60 fF injection capacitor can be used to measure the charge sensitivity of the analog processor and, therefore, to calibrate the charge collected by the sensor as a responce to a laser pulse. This result can be exploited to measure the charge sensitivity in all of the matrix channels as reported in Table 1 for a peaking time of 0.5 μs. Charge sensitivity values reported in Table 1 have been taken into account in order to express the scan test results in terms of charge, therefore eliminating the dependence on the charge sensitivity. Fig. 3 shows, using a graduated grey-scale, the total charge collected by the matrix for each position of the laser spot on the MAPS matrix.

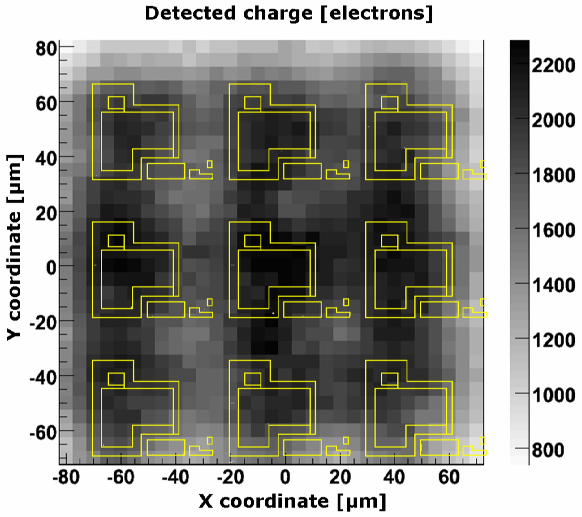

Figure 3: charge collected by the 3×3 matrix as a function of the laser spot position.

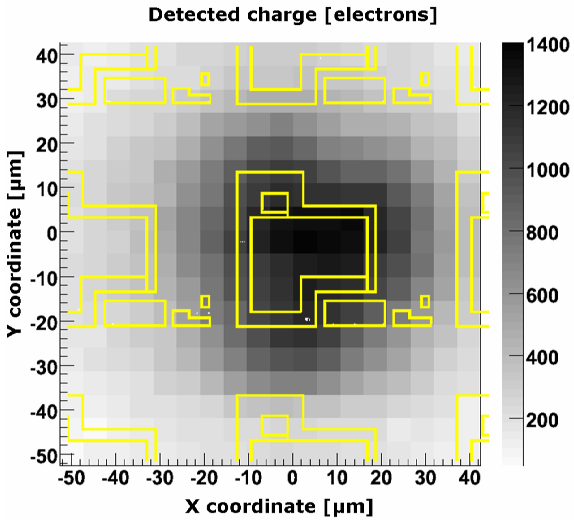

Figure 4: charge collected by the central pixel in the 3×3 matrix as a function of the laser spot position.

The matrix layout has also been superimposed to the figure. Detected charge decreases moving toward the periphery where also dummy pixels are involved in charge collection. The regions featuring a brighter grey tone can be related to the presence of standard N-wells, which subtract charge from the DNW collecting electrodes. When the laser beam hit such regions, a reduction of about 30% in charge collection is observed with respect to the best case (2283 electrons). Fig. 4 shows the charge detected by the central pixel in the 3×3 matrix; the maximum value has been found to be about 1400 electrons.

B. *Monte Carlo simulations*

Experimental characterization of the Apsel2 chips, has been used to validate the results obtained by means of the Synopsys TCAD package and, in particular, of a specifically developed Monte Carlo code based on random walk [5]. As a matter of fact, the Dessis physical simulator, belonging to the TCAD package, employs finite element methods and requires very long simulation time for 3D devices like the 3×3 Apsel matrix; therefore its use has been restricted to the simulation of a few ionizing events. In order to evaluate the overall matrix collection capability in response to a MIP, a Monte Carlo algorythm has been developed to simulate the random walk of electrons in the undepleted substrate of MAPS detectors, where diffusion is the main transport mechanism of minority carriers. Information about the depletion region thickness provided by the TCAD analysis was used to determine the effective depth of the collecting electrode diffusion to be hardcoded in the Monte Carlo simulation. Given the electron concentration $n(x, y, z, t)$ as a function of the three spatial coordinates *x, y, z* and the time t, diffusion equation can be expressed as

$$\frac{\partial n(x,y,z,t)}{\partial t} = D_n \nabla^2 n(x,y,z,t), \qquad (1)$$

where D_n is the electron diffusion constant. Random walk can be regarded as a discrete representation of carrier diffusion. In the three dimensional random walk, the carrier spatial step Δl and the associated time step Δt can be expressed through the relation

$$\Delta l^2 = 6 D_n \Delta t, \qquad (2)$$

where D_n can be fed to the simulator once the substrate doping is known. Results obtained by means of Monte Carlo simulations can be exploited to get an evaluation of the device properties in terms of collected charge and charge spreading in a much shorter time than in the case of finite element calculation. Simulations with Monte Carlo techniques have been performed with the following assumptions:

- 80 electrons/μm are generated uniformly along a linear track which is normal to the device surface and features a gaussian distribution in the plane normal to the track itself. Standard deviation associated to the gaussian distribution is 0.5 μm.
- The Apsel simulation volume is 230×230×80 μm^3.
- Electrons lifetime, according to the Scharfetter model [6], is about 9.2 μs at the considered doping levels ($10^{15}\ cm^{-3}$) and sets a limit to the random walk duration for each carrier.

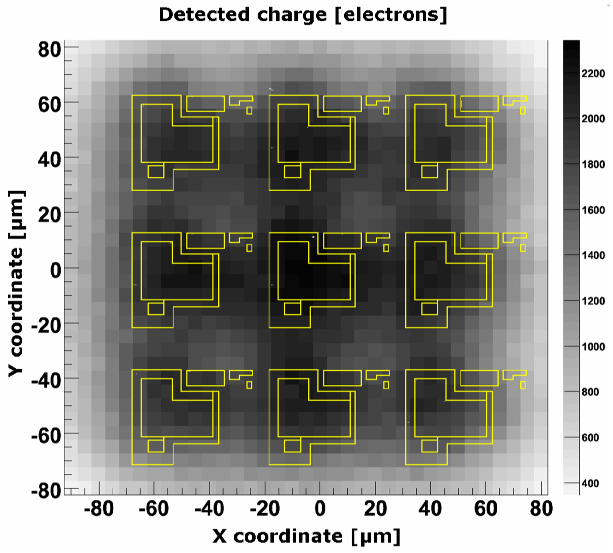

Figure 5: Monte Carlo simulation results. Charge collected by the Apsel2 3×3 matrix is displayed as a function of the position of the MIP collision point.

Fig. 5 shows, for each of the 1225 simulated collision points, the total charge collected by the matrix using a graduated greyscale. The presence of standard N-wells, similarly to what was pointed out by the laser source tests, reduces the detected charge by about 30% with respect to the best case (2343 electrons). The maximum value of the charge detected by the single pixel is about 1500 electrons, in good agreement with the measurement results.

III. THE SDR0 TEST CHIP

A MAPS sensor with different topology, designed for applications to the International Linear Collider experiments, has been integrated in the SDR0 (Sparsified Digital Readout) prototype chip fabricated in the same STM 130 nm technology as the Apsel2 MAPS. The SDR0 chip, not yet available for experimental characterization, includes single pixel structures, an 8×8 matrix and a 16×16 pixel matrix featuring sparsified data readout and a 25 μm pitch. As compared to the prototypes of the Apsel series, in the analog section of the SDR0, no shaping stage was included in order to fullfil the resolution constraints [7]. Moreover, due to the large number of transistors in the digital section, which is based on a simplified version of the scheme implemented in the FPIX chip [8], a non negligible portion of the cell area has been covered with standard N-wells to integrate PMOS devices. This is shown in Fig. 6, togheter with the layout of the DNW collecting electrode.

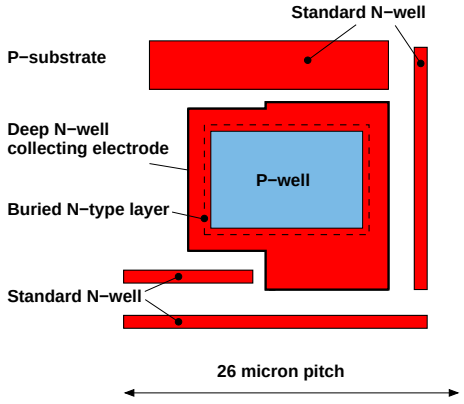

Figure 6: top view of the SDR0 elementary cell layout.

In the next sections results obtained with the Synopsys TCAD suite and with Monte Carlo techniques will be presented with the aim of evaluating the impact of the standard N-Well diffusion on the pixel charge collection.

A. TCAD simulations

Physical simulations with the TCAD package have been performed on a 3×3 matrix with elementary cells featuring the geometry shown in Fig. 6. The device thickness was set to 50 μm. Such a value has been chosen keeping into account the results of TCAD simulations performed on 2D MAPS devices that pointed out a saturation trend in the charge collected by a single pixel for subtrate thickness greater than about 2 tens of microns [4].

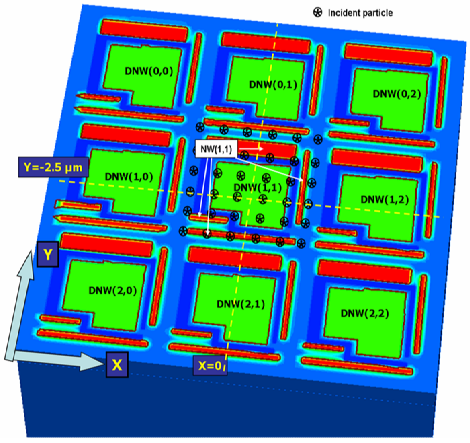

Figure 7: 3×3 matrix featuring the SDR0 geometry simulated with the Synopsys TCAD package.

The simulated structure, which reproduces the geometry of the SDR0 matrix, required a mesh with 165000 vertices. Because of the really long computational time only 36 simulations, each one involving a different MIP collision point, have been performed according to the point grid shown in Fig. 7.

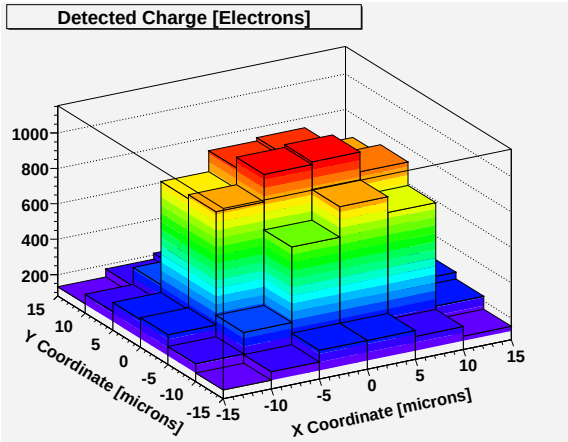

Figure 8: charge collected by the central SDR0 cell as a function of the MIP collision point (Synopsys TCAD simulations).

The Heavy Ion model, available for transient simulations, was used to generate a uniform charge distribution along the particle track with a release rate of 80 electron-hole pairs/μm. Fig. 8 shows the charge collected by the central pixel as a function of the position of the impinging particle. Detected charge, featuring a maximum value close to 1000 electrons, almost uniformly decreases down to less than 200 electrons at the pixel periphery.

B. Monte Carlo simulations

As in the case of the Apsel family chips, Monte Carlo techniques have been used to further investigate the SDR0 properties in terms of charge detection and charge sharing making the same assumptions described in section II.B except for the simulated structure volume which is 85×85×80 μm^3 in the case of the SDR0.

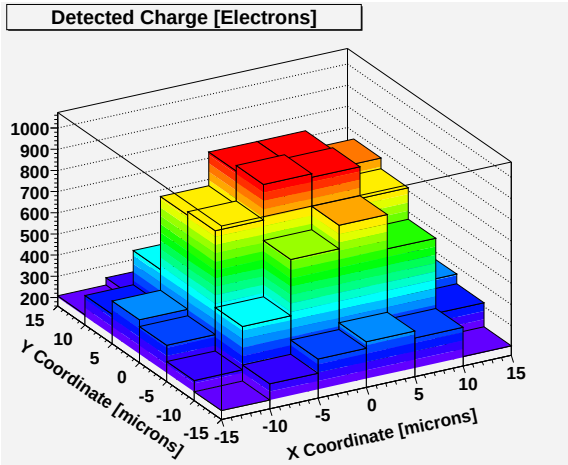

Figure 9: Monte Carlo simulation results. Charge collected by the central pixel of the 3×3 SDR0 matrix as a function of the position of the MIP collision point.

With reference to Fig. 9, which shows the charge collected by the central pixel matrix for the same 36 collision points used in the TCAD simulations, both the maximum collected charge value of about 1000 electrons and the overall distribution are in good agreement with results shown in Fig. 8. The good agreement between TCAD and Monte Carlo simulations is maintained also in the case of the maximum value of the charge collected by the full matrix which is, as displayed in Fig. 10, about 1600 electrons. In the neighborhood of the central pixel, where the standard N-well diffusions are located, a collected charge reduction of about 50% with respect to the maximum value was observed for both the simulation tools.

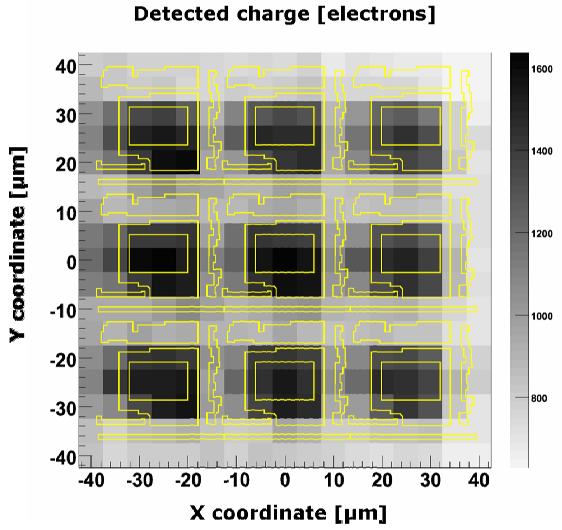

Figure 10: Monte Carlo simulations results. Charge collected by the 3×3 SDR0 matrix is displayed as a function of the position of the MIP collision point.

IV. Conclusions

In this work the properties of different deep N-well MAPS detectors, designed and fabricated in a 130 nm triple well process, have been investigated both through experimental characterization and simulations. Standard N-wells in the elementary cells interfere, as expected, with the charge collection process of the DNW electrode. In the case of the Apsel2 chips, the extent of such parasitic effect could be quantitatively estimated and was found to be in good agreement with the results from Monte Carlo simulations. Results obtained for the SDR0 pixel geometry indicate a worst case loss in the total detected charge of about 50% with respect to the maximum value. These results will be compared to the experimental characterization data as soon as the chip will be available. In the future, taking advantage of the really short computational time, Monte Carlo methods will be used, beside the Synopsys TCAD software package, in the design of the next generation prototypes in order to determine the best collecting electrode geometry from the standpoint of charge collection efficiency.

References

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