due to the presence of N-
housing P-type transistors
ignificant whether the deep
aratively larger.

chips

charge preamplifier,
discriminator and latch.

grammed to assume
s: 0.5 µs, 1 µs, 2 µs.

ip

charge preamplifier,
nd latch.

m and is suitable for
ational Linear Collider

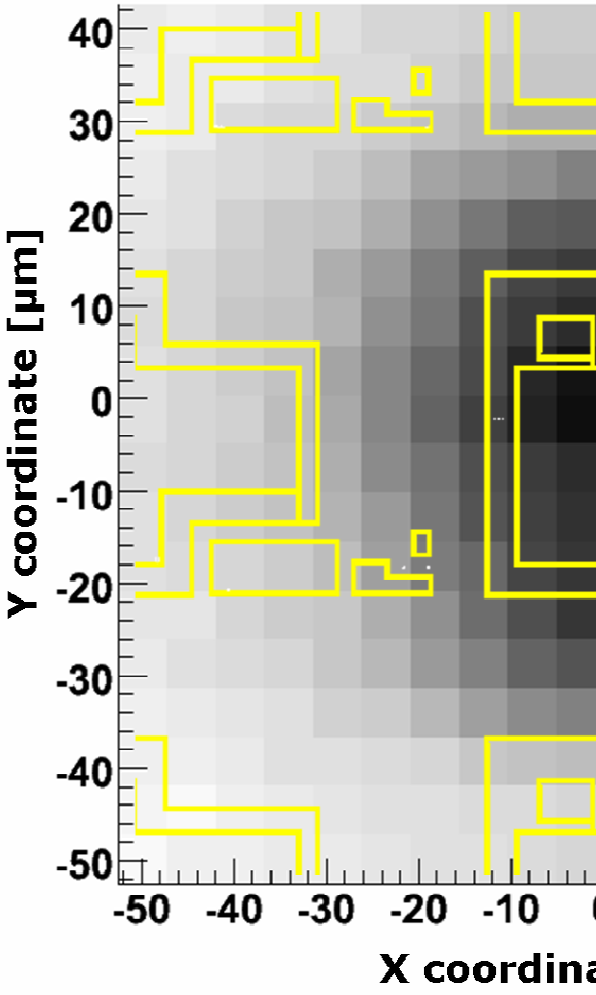
level include sparsified

mulation

ed charge [electrons]

- Electrical pulses with ar
are required to emula
surface (substrate thick
- Matrix scan tests featu
points with a 5 µm ste
directions.

Detected char



Charge collected by the
matrix as a function of th

Apsel2-g

Monte Carlo simula