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MAPS in 130 nm and 90 nm triple well CMOS technologies for HEP applications

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In this work deep N-well CMOS monolithic active pixel sensors (DNW-MAPS) are presented as an alternative approach to signal processing in high energy physics experiments. Based on different resolution constraints, some prototype MAPS, suitable for applications requiring different detector pitch, have been developed and fabricated in 90 nm and 130 nm triple well CMOS technologies. Experimental results from the characterization of the test structures with different features will be presented together with TCAD and Monte Carlo simulations intended to study the device substrate properties in terms of charge diffusion and charge sharing among pixels.

Summary

Recently, monolithic active pixel sensors (MAPS) properties have been intensely investigated by several research teams involved in the development of detectors for particle physics experiments. Their monolithic structure, featuring a few μm thick superficial active volume, makes them interesting for applications to experiments at the future high luminosity colliders. In particular, deep N-well (DNW) MAPS make use of a buried N-type layer, available in modern triple-well deep submicron CMOS processes, as the charge collecting electrode and, instead of the classical three transistor readout scheme, employes a charge sensitive amplifier to perform signal amplification. The use of a DNW as the collecting electrode makes it possible to layout all of the N-channel transistors belonging to the front-end electronics over the sensor area, therefore reducing the impact of the electronics itself on the detector fill factor. In order to fully exploit the potential of complementary MOSFET processes and include also PMOS transistors (which need to be integrated in standard N-wells) in the design of the pixel level electronics, the sensitive element has to take up a significant fraction of the elementary cell surface. The above described approach results in an increased functional density which may be exploited to add a filtering stage and some simple logic blocks to the charge preamplifier. These guidelines have been followed in the design of different prototype chips fabricated in 90 nm and 130 nm epitaxial, triple well CMOS processes provided by STMicroelectronics. A set of test chips, called Apsel (active pixel sensor electronics) and including single pixel structures and MAPS matrices, has been designed both in 130 nm and 90 nm CMOS technologies. Pixel-level front-end electronics in the Apsel2 family chips takes advantage of a typical readout channel for capacitive detectors including a charge preamplifier and a shaping stage and is suitable for the design of detectors with a pitch in the 50 μm range. A different readout topology, lacking the shaper, has been integrated in the SDR0 prototype chip which includes single pixel structures, an 8X8 matrix and a 16X16 pixel matrix featuring sparsified data readout and a 25 μm pitch. Noise and charge sensitivity properties of the front-end electronics will be measured by means of charge injection in some dedicated structures. Functionality tests of the sparsified digital readout architecture will be carried out in the SDR0 chip. A laser source will be used for the experimental characterization of the device properties in terms of charge diffusion in the substrate, charge collection and charge sharing among the pixels. Such results will be compared to results from the simulations performed with ISE-TCAD tools by Synopsys and with Monte Carlo techniques specifically developed to

simulate random walk of minority carriers in an undepleted detector substrate.

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