Data transmission and selection for the L0 calorimeter trigger of LHCb

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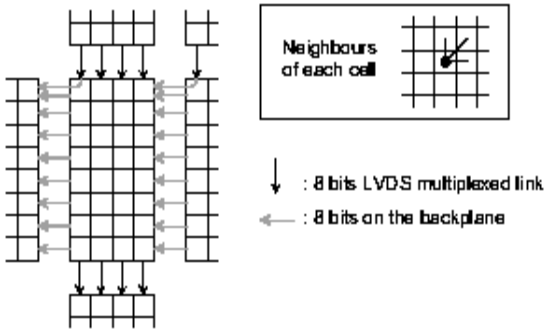
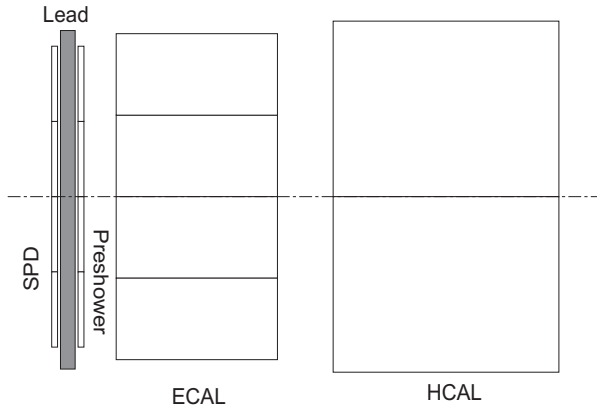
Introduction

The L0 trigger system of LHCb is used to reduce the bunch crossing rate of LHC (40.08 MHz) to the 1 MHz rate sustainable for the High Level Trigger.

The calorimeter system of LHCb is used to select the highest energetic clusters in the ECAL (electromagnetic calorimeters) or HCAL (hadronic calorimeters) for the L0 calorimeter trigger.



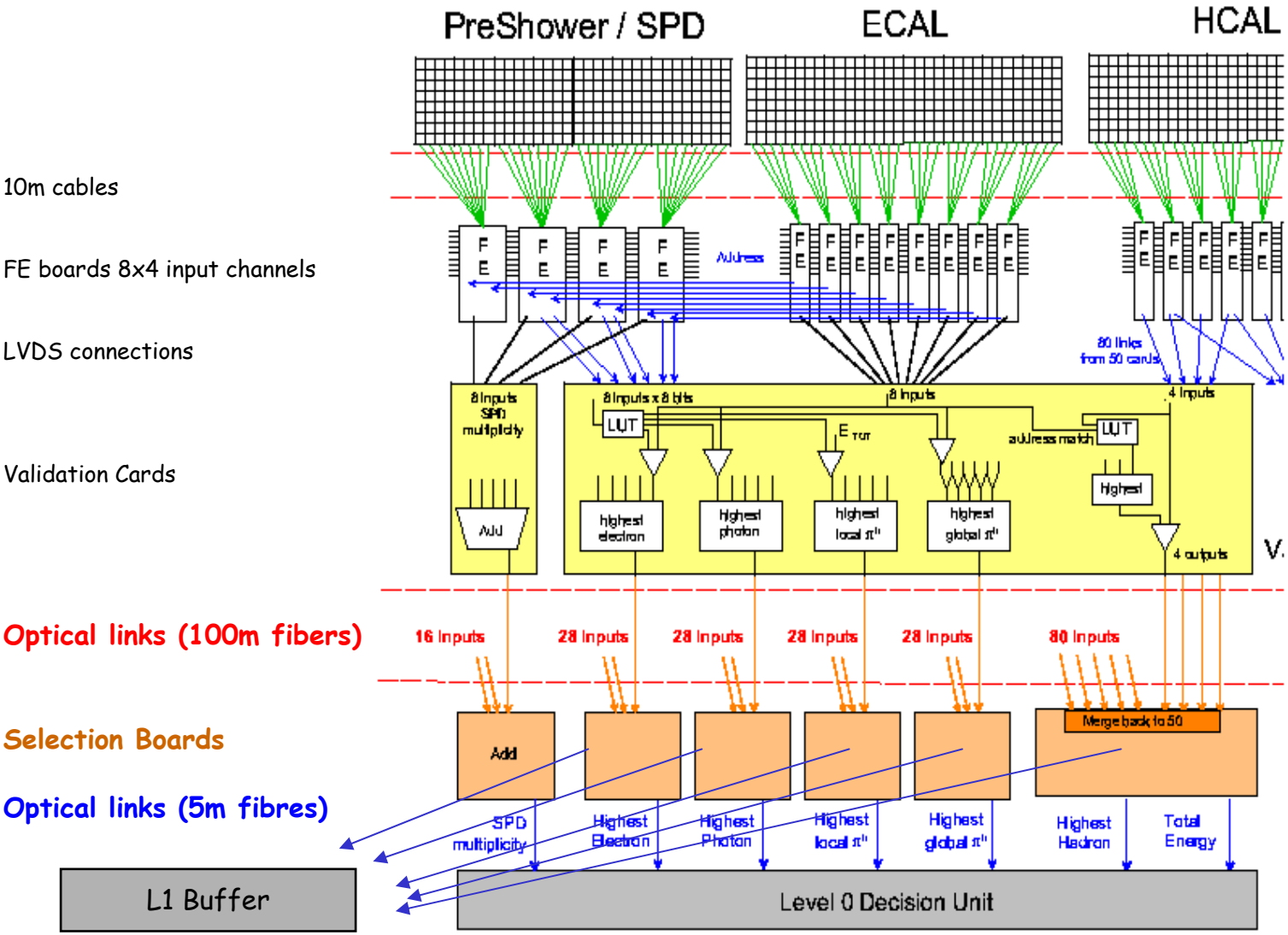
The 32 channels front end board selects a cluster as a 2x2 local maximum energy deposit.



Signal from the auxiliary detectors SPD and Pre-Shower are used in the Validation phase to assess the cluster type (Particle Identification).

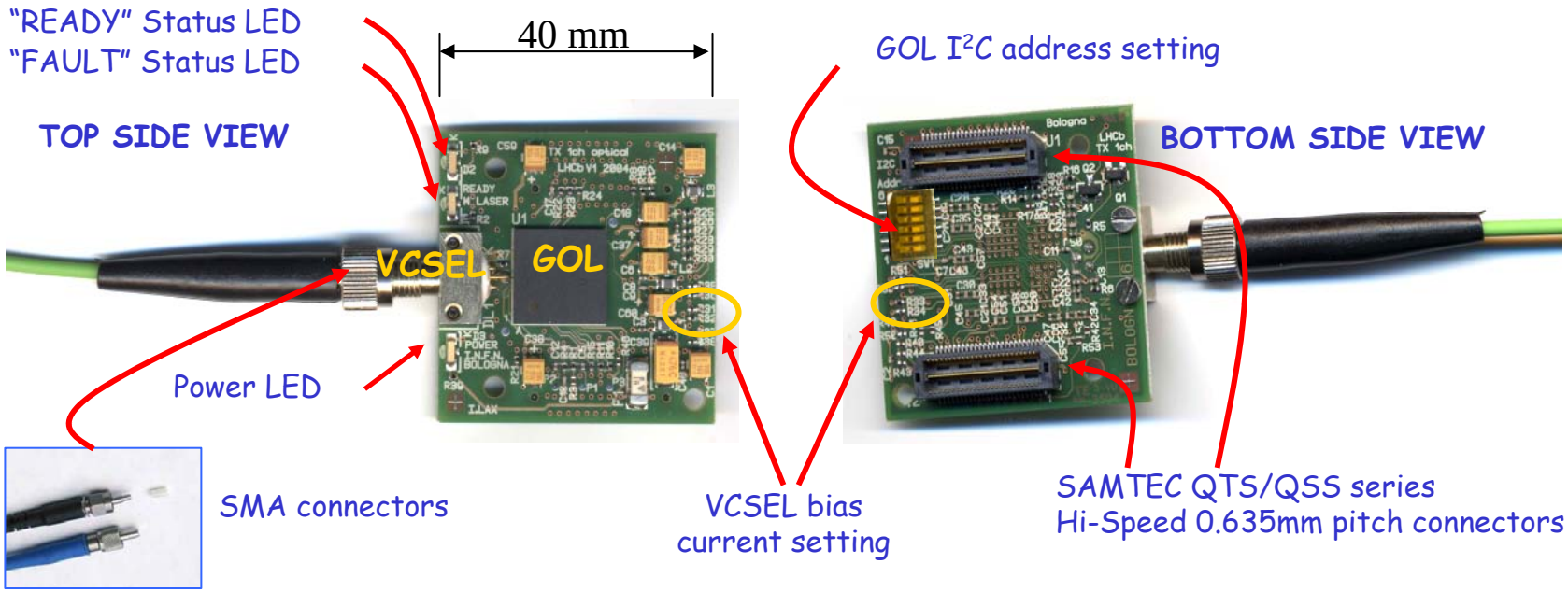
The cluster energy is measured on 2x2 cells at the front-end board, from 8x8 cm^2 (inner ECAL) to 52x52 cm^2 (outer HCAL).
ECAL is segmented in 5952 cells (each cell is a possible cluster).
Validation (to determine the cluster type) is done by the PS/SPD (same geometry) to get the electron and photon candidates. Combination of the detector signal to select π^0 candidates are also foreseen.
HCAL is segmented in 1484 cells (each cell is a possible cluster). Addition of the energy possibly lost in ECAL if available.

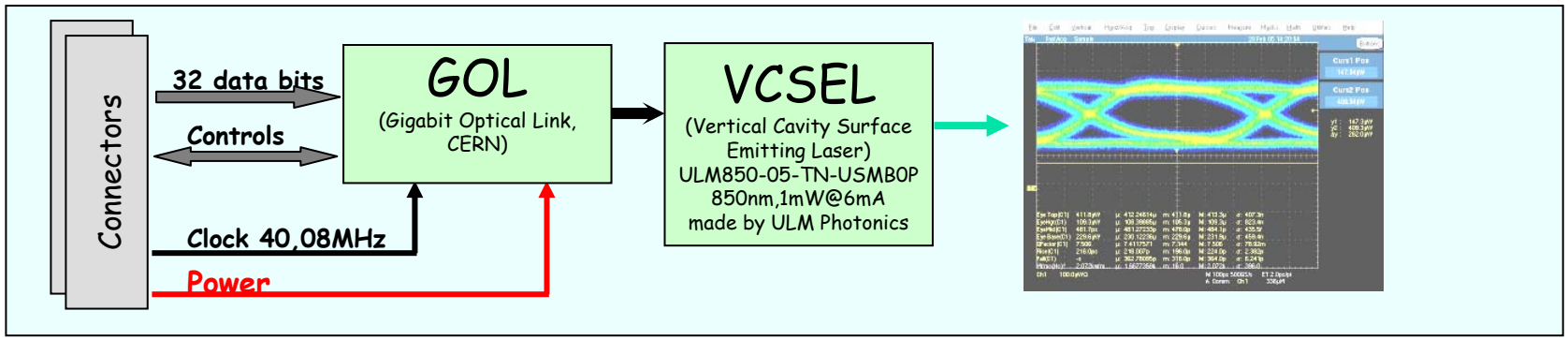
L0 Calorimeter Trigger



Single-Channel TX

Assembled and tested: 16 (PreShower & SPD) + 24 (SB) + 10 (spares) = 50 boards



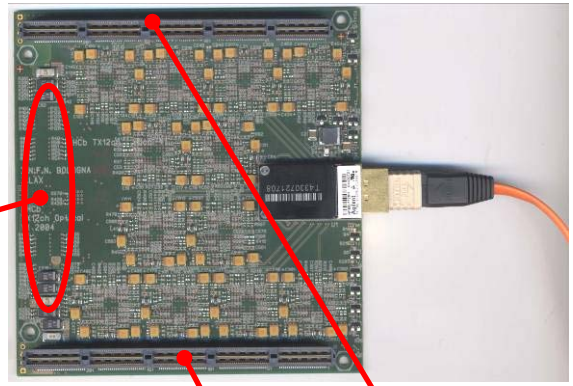


Multi-Channel TX

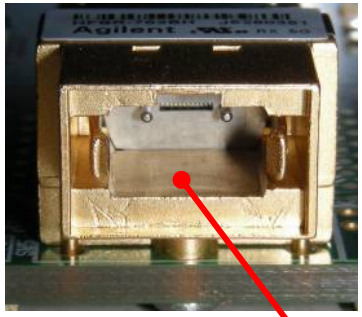
Assembled and tested: 28 (VC) + 44 (CROC) + 28 (spares) = 100 boards

BOTTOM SIDE VIEW

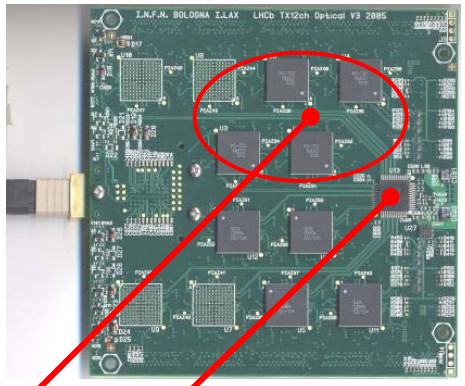
GOL I2C address setting



AGILENT HFBR-772BH MPO receptacle with guiding pins



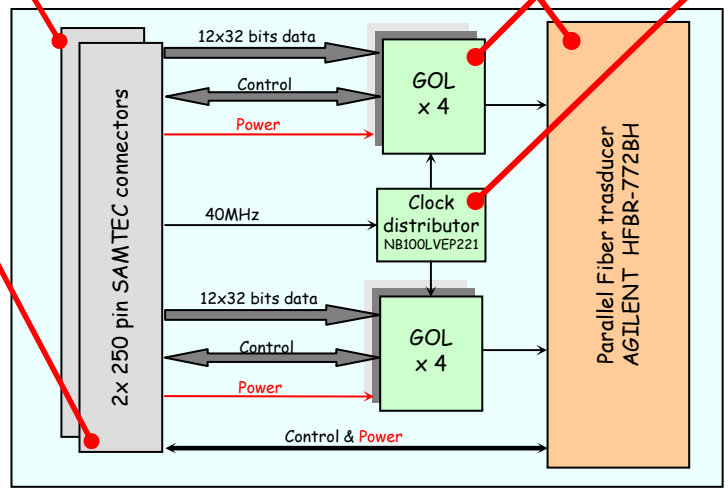
TOP SIDE VIEW



116 mm.

MAIN FEATURES:

- 8 independent electro-optical transducers accept 8x32-bit at 40.08MHz;
- 1 multimode 850nm 50/125u optical ribbon fiber with MPO connector;
- 2 independent JTAG chains;
- I2C bus for individual GOL addressing;

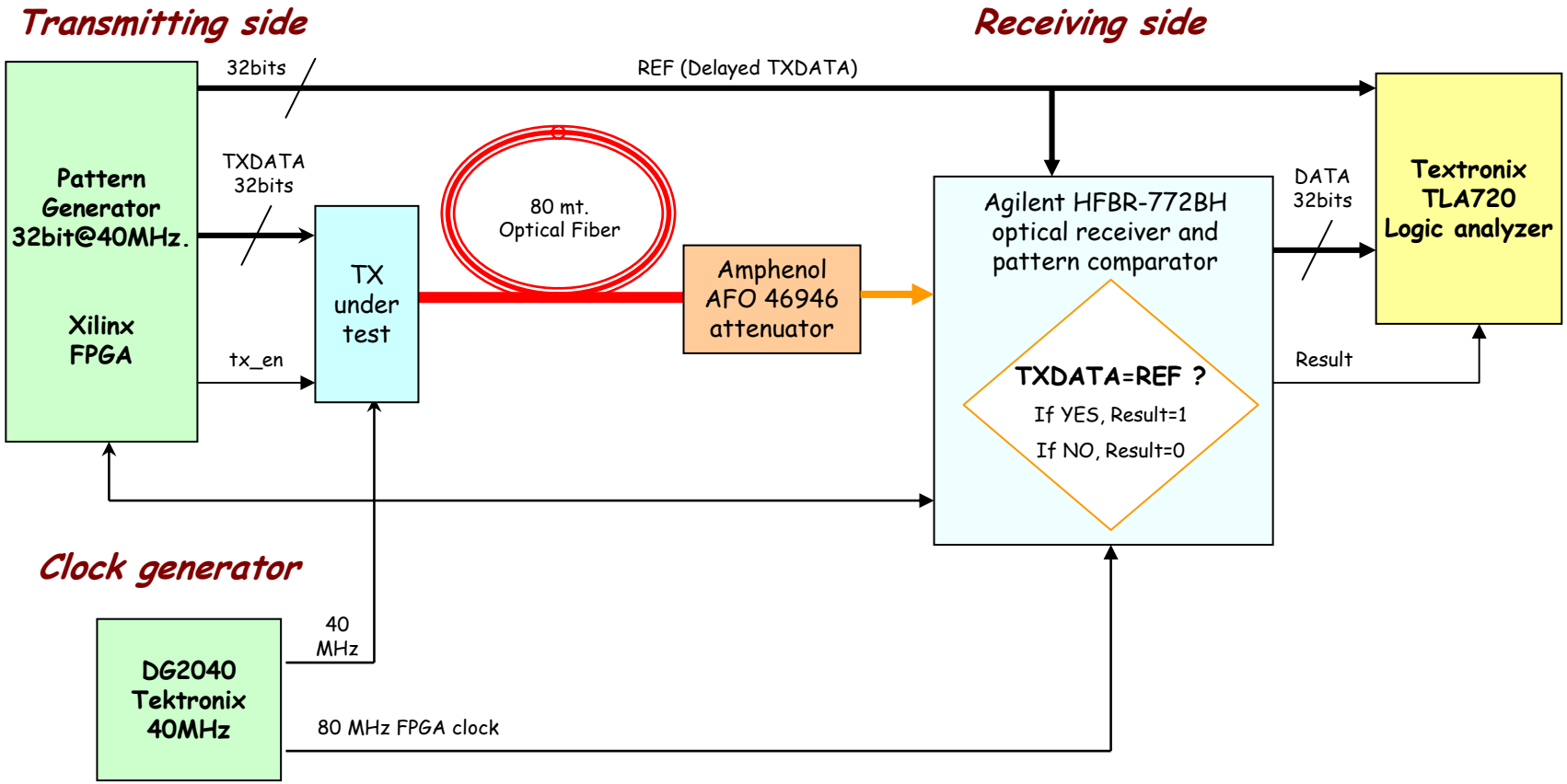


CROC= Calorimeter Readout Optical Cards

VC=Validation Cards

BER Measurement

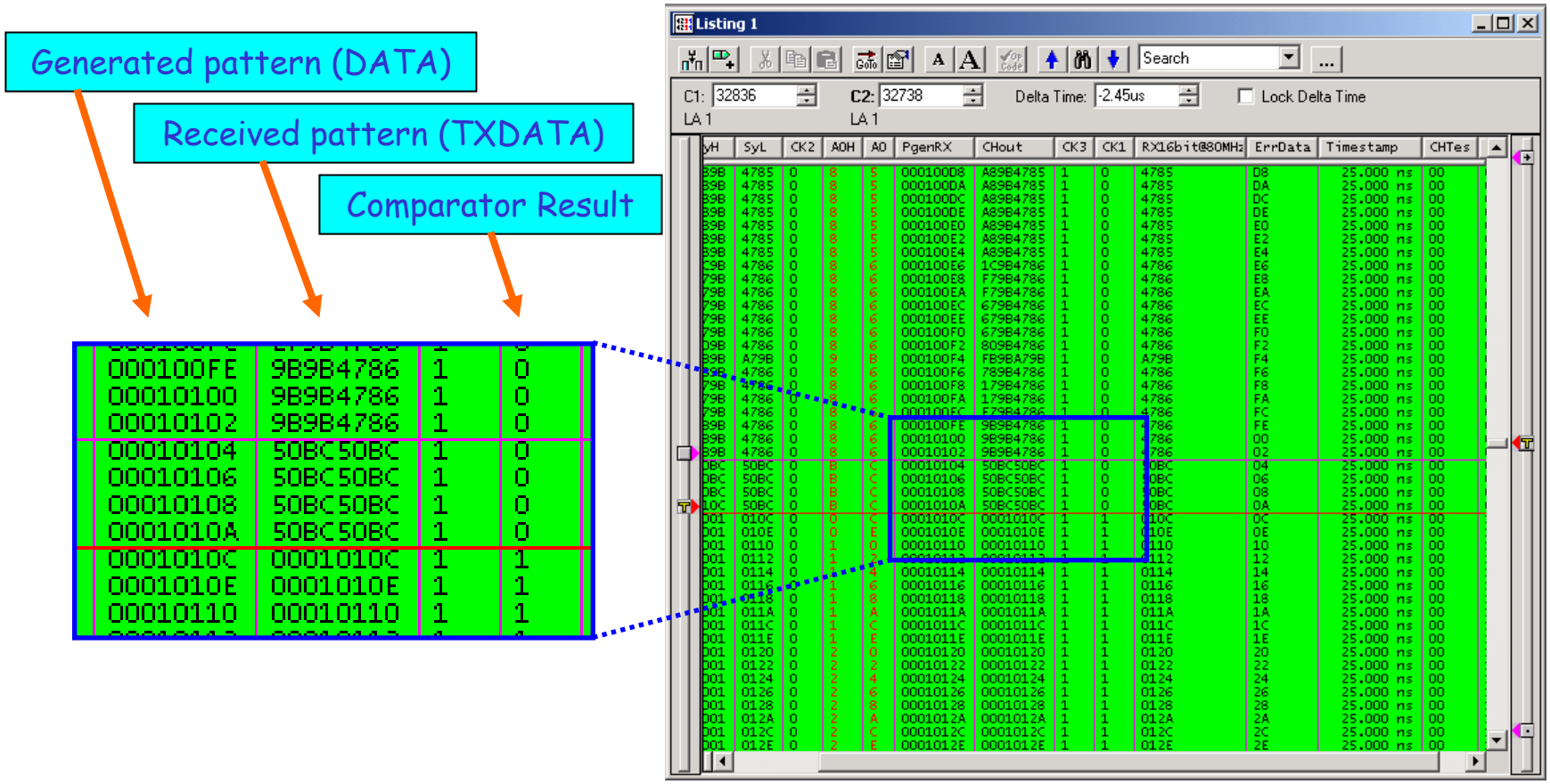
For prototype qualification



Testing time: from 5hrs up to 1 day.
In a range of attenuation values between 0 and 8dB, the results show that the BER is better than 10^{-13} as expected.
In the final conditions, the measured attenuation of the entire optical path is less than 1dB.

BER Measurement II

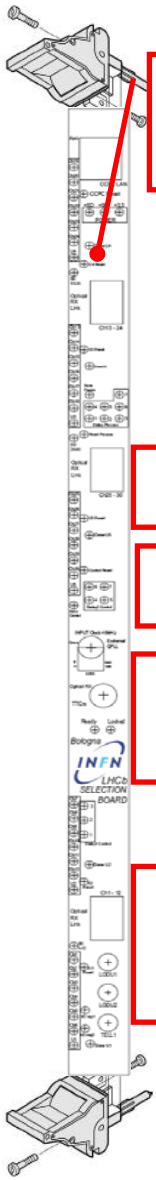
TX synchronization - This logic analyzer screenshot shows how the receiver got synchronized by IDLE patterns.

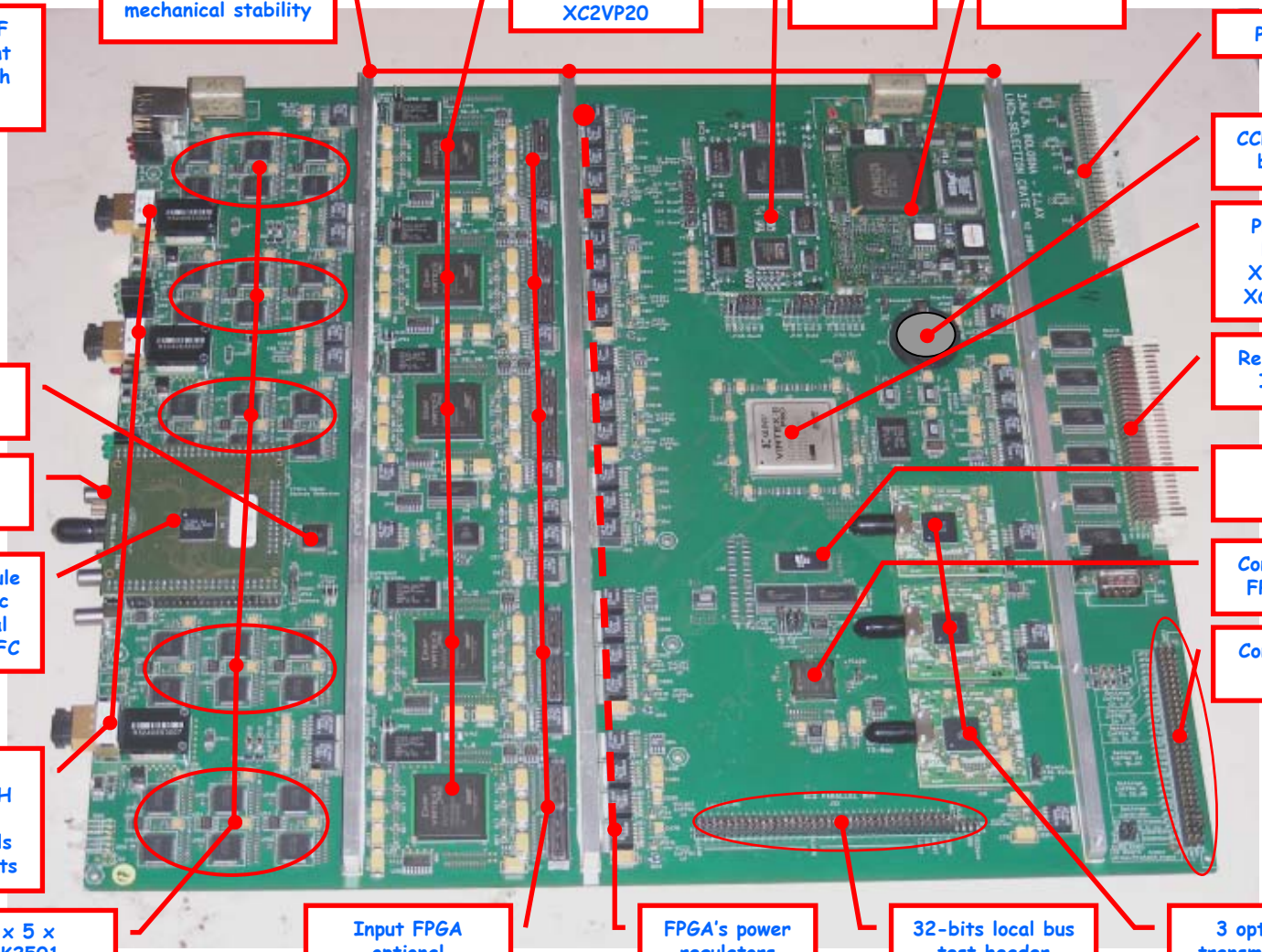


Selection Board (SB) Main Features

- 8 SB hosted in the Selection Crate are needed to perform the entire data selection (4 additional boards as spare).
- Trigger information to the L0DU:
  - selection of the highest energy candidate for each particle type;
  - complete cluster address translation, converting the 8-bit address in the 14-bit address by means of a dedicated Look-Up-Table (LUT);
  - computation of the total HCAL energy release and the SPD multiplicity that are used as auxiliary trigger information (for example, an empty or a too complex event to be rejected);
- Trigger information to the HLT:
  - In case of L0-accepted events, all the input and output data of the SBs are moved forward to the TELL1 boards.
- The hardware of the SB boards is identical, but individually programmed depending on the required selection task to be performed.

SB Overview





SCHROFF 4TE Front panel with handles

3 Metal bars for thermal and mechanical stability

5 Input FPGAs XILINX XC2VP20

Glue Card

CCPC

Power source

CCPC CMOS battery

Process FPGA XILINX XC2VP40

Report board I/O port

CLOCK distributor

External CLOCK

Process LUT AT28LV010

TTCrq module with plastic ST optical input for TFC

Control FPGA

Configuration jumpers

3 Agilent HFBR782BH MPO 12_channels optical inputs

6 x 5 x TLK2501 deserializers

Input FPGA optional expansion ports

FPGA's power regulators

32-bits local bus test header

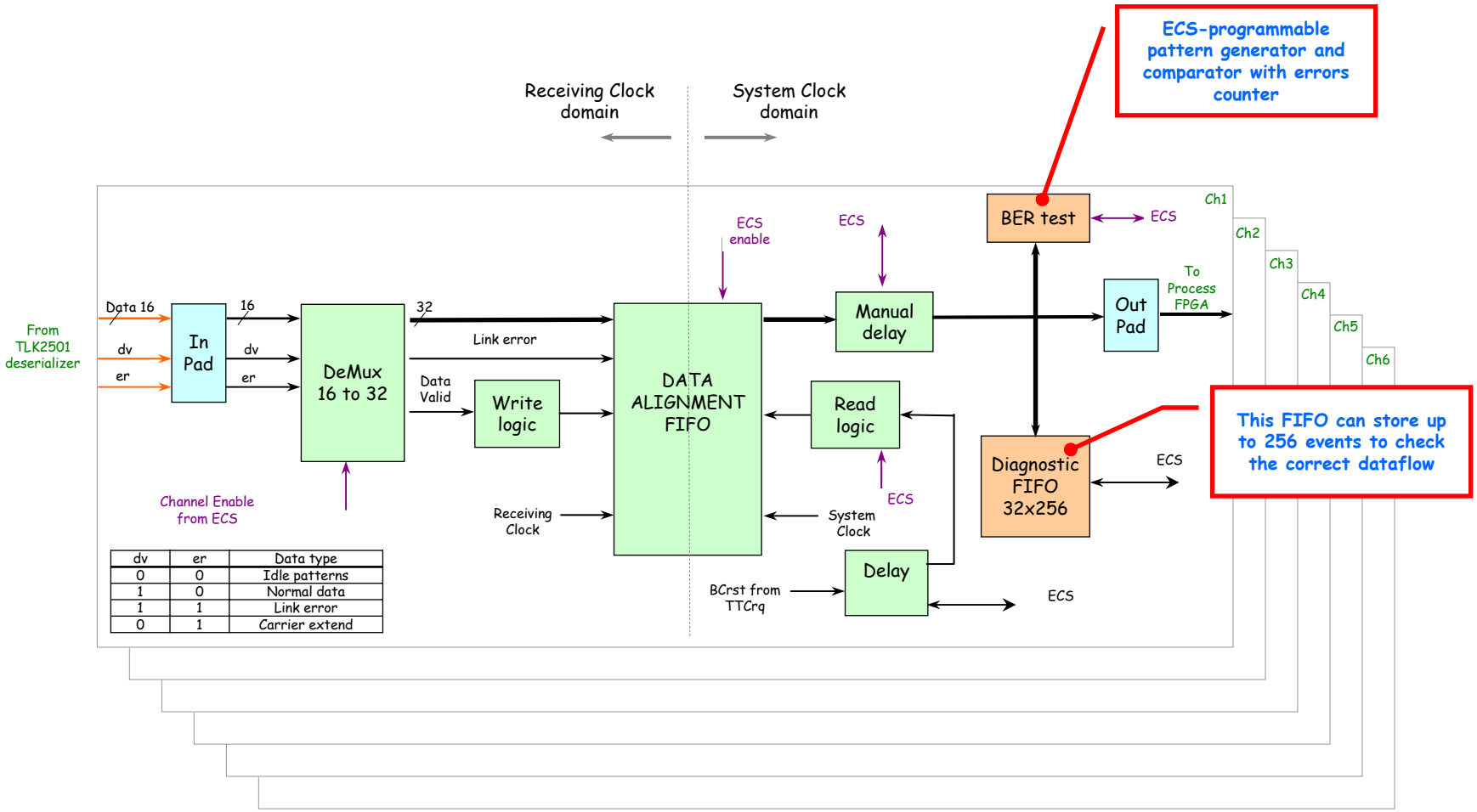
3 optical transmitters

SB Technical Features

PHYSICAL:
- VME 9U/4TE standard, 2.6 mm PCB thickness, 16 PCB layers;
- Controlled impedance paths designed for critical signals (i.e. clock, serial data);
- Similar length of the traces between different deserializers;

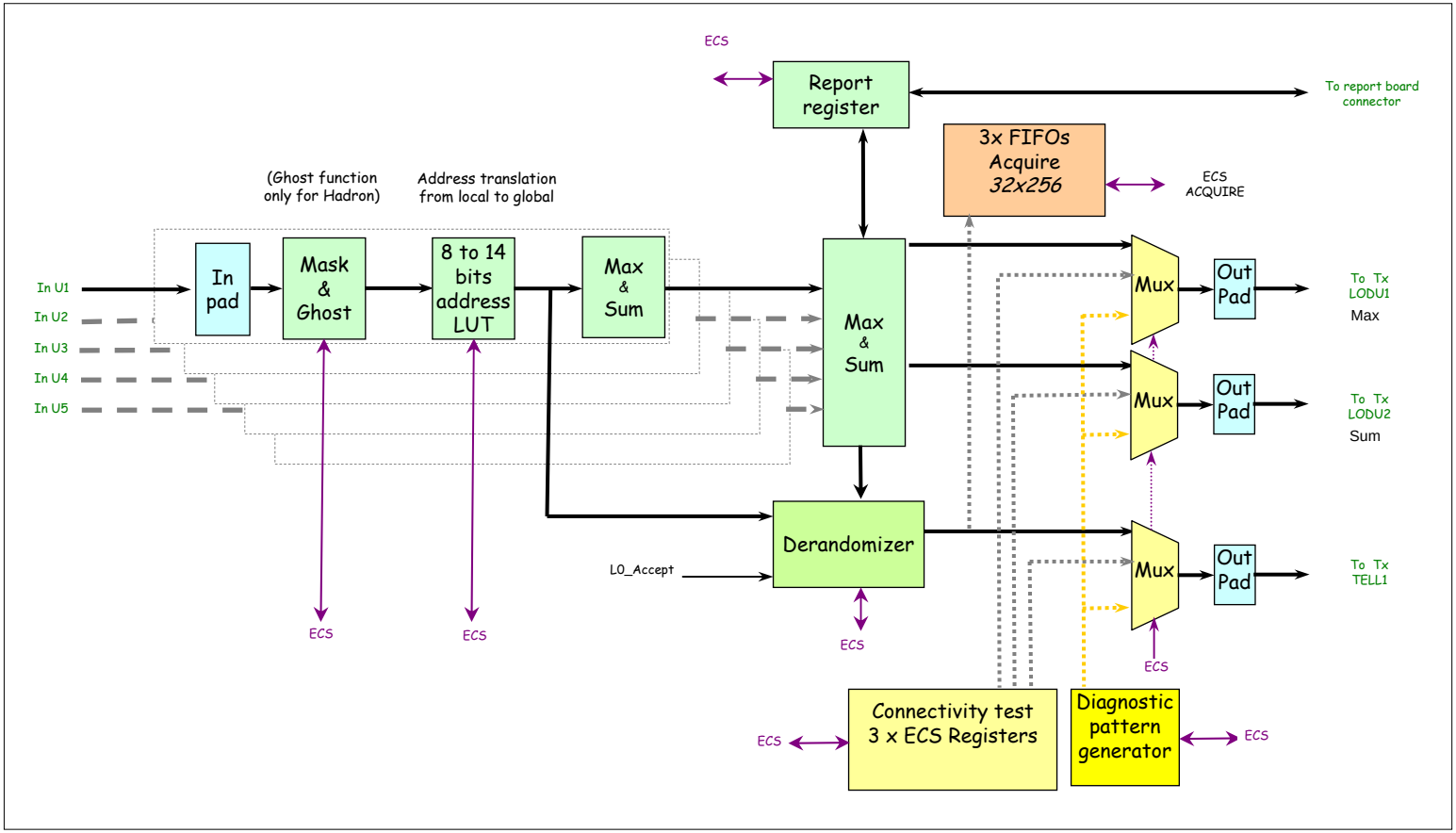
FUNCTIONAL:
30 optical inputs (28+2 spares) suited for MPO-F connectors and ribbon of 12 fibers;
3 optical outputs, suited for single-fiber SMA connector boards, carrying event information such as total energy, total sum, L0 trigger;
On-board programming and debugging hardware (4 x I2C buses, 3 x JTAG chains, 1 x 32 bits parallel multiplexed local bus, optional expansion ports);
Automatic logic block for input data alignment;
ECS-addressable Look-Up-Table (LUT) provided for event address translation from 8bits to 14bits (the process FPGA automatically loads its on-board LUT at start-up);
ECS-addressable input and output FIFOs, provided to check the correct data flow during normal operation of the entire selection process;
Capability of inter-board communication, through a dedicated interface and a point-to-point connector (feature used in the HCAL, which requires 3 SBs to handle 80 optical channels);
Temperature sensors for monitoring of several areas of the board;

SB Input Logic



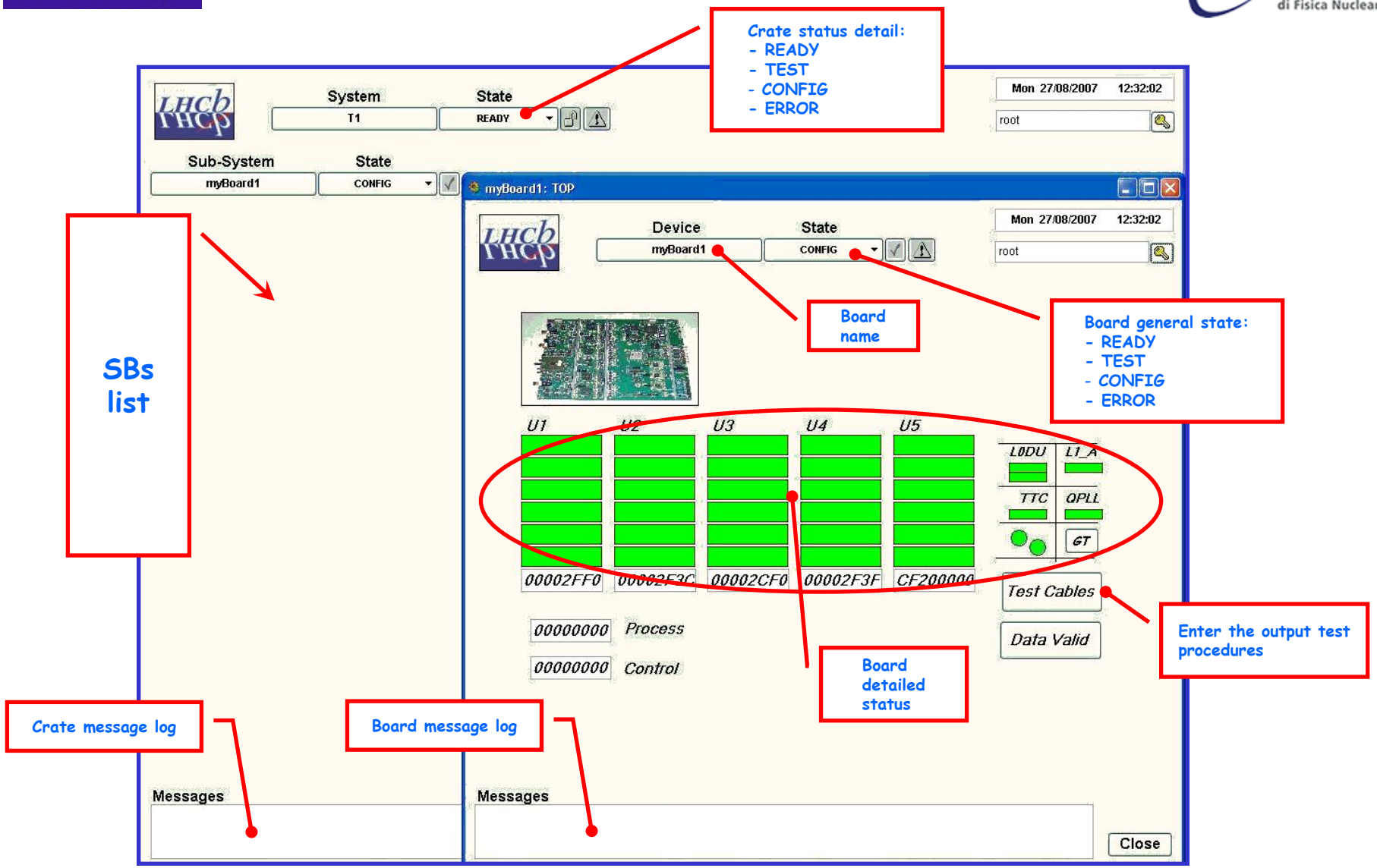
Input FPGA XILINX XC2VP20: project implementation overview

SB Process Logic



Process FPGA XILINX XC2VP40: project implementation overview

SB Control Panels

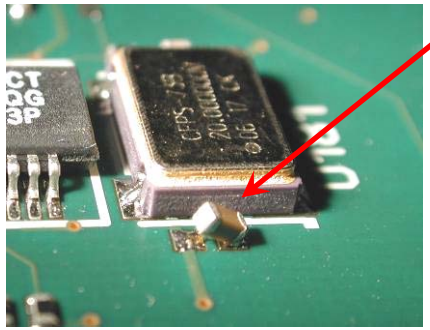


SB Debugging

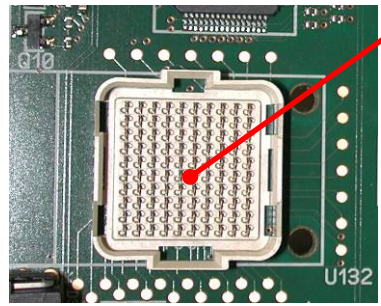
The assembling has been done by an external company.

During the debugging, a few "common" issues needed to be fixed.

Nevertheless, the overall quality is outstanding.

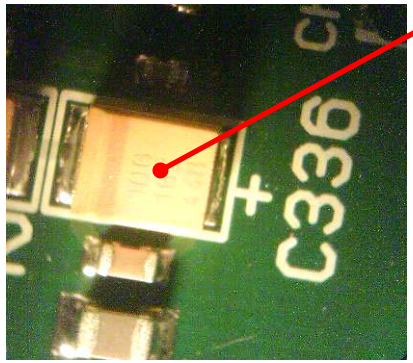


Ceramic capacitor badly soldered

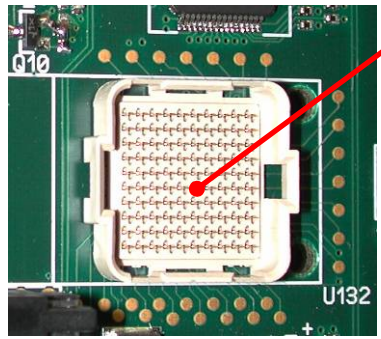


BADLY oriented

HFBR-782BH
10x10 array socket



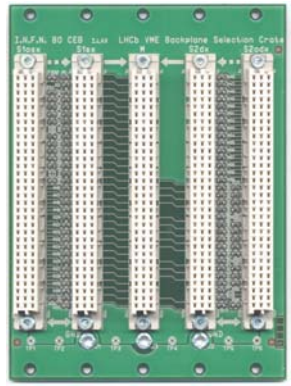
Tantalum capacitor reverse mounted



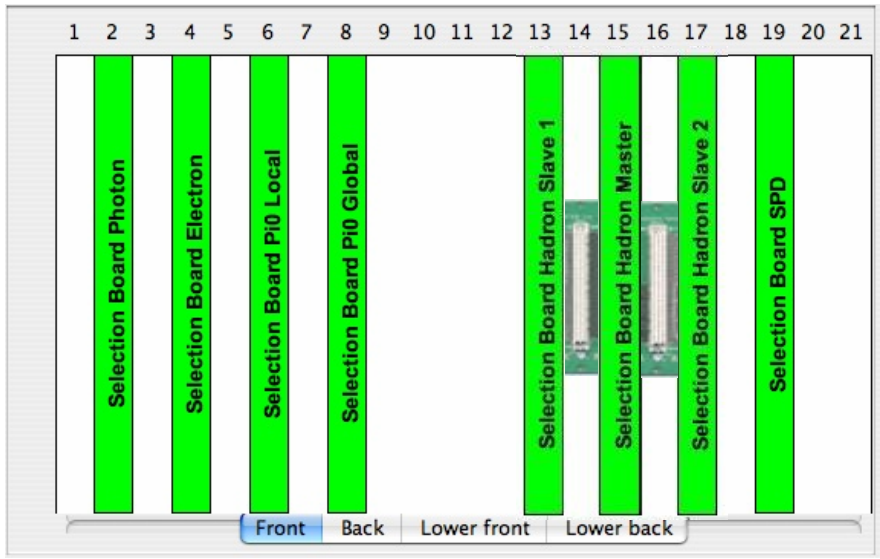
CORRECTLY oriented

SB Installation

SB-dedicated point-to-point connector



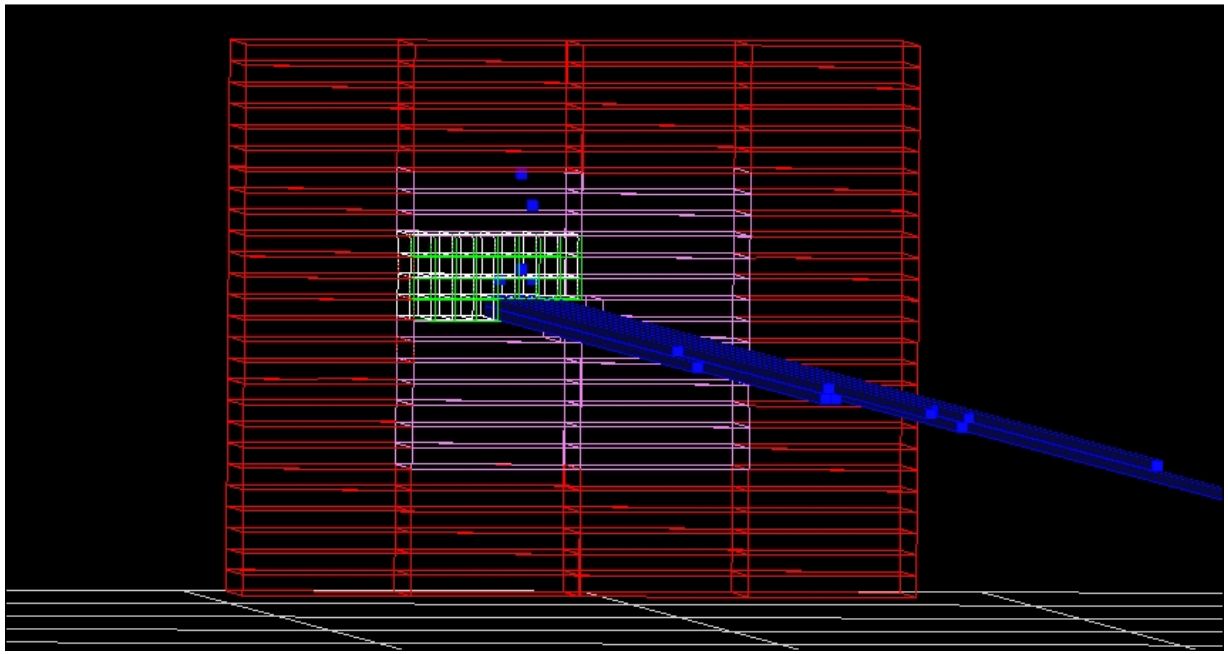
Installation of the first SB at Point 8, CERN, April 2007



The SB layout in the Selection Crate (note the 3 joined SB for Hadron)

SB Test Results

HCAL



First acquisition results, CERN,
May 2007

An HCAL response to LED pulses simulating a high energy deposit. The event has been triggered and reconstructed.

Conclusions

Optical TX

- We built up 150 optical transmitter modules for the LHCb calorimeter system, needed both for the L0 trigger and data acquisition.
- We successfully tested the entire set of single- and multi-channel optical TX modules.
- They have already been tested by plugging them to their carrier main boards.
- The optical TX modules behave as expected.

Selection Boards

- 12 boards have been produced and globally tested in our lab in Bologna.
- A first board has been successfully installed last April at CERN.