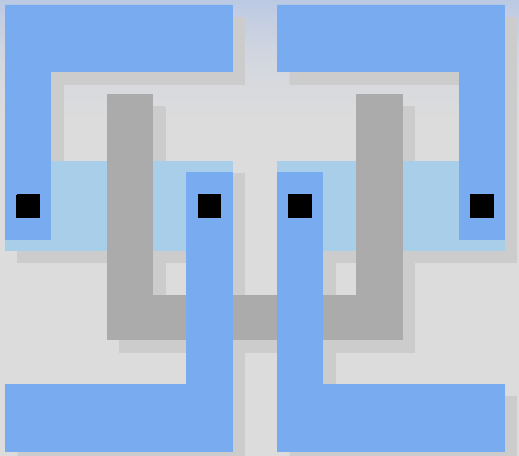
Steering and Readout Chips for DEPFET Sensor Matrices



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–TWEPP Conference

–05.09.2007

–Prague, Czech Republic

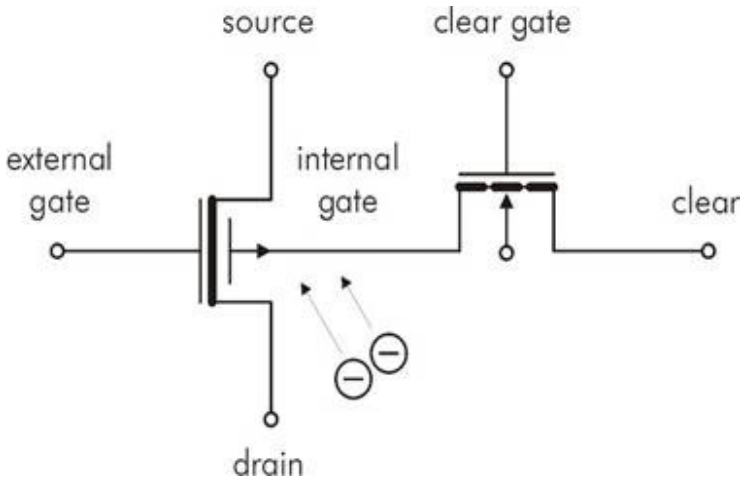
Outline

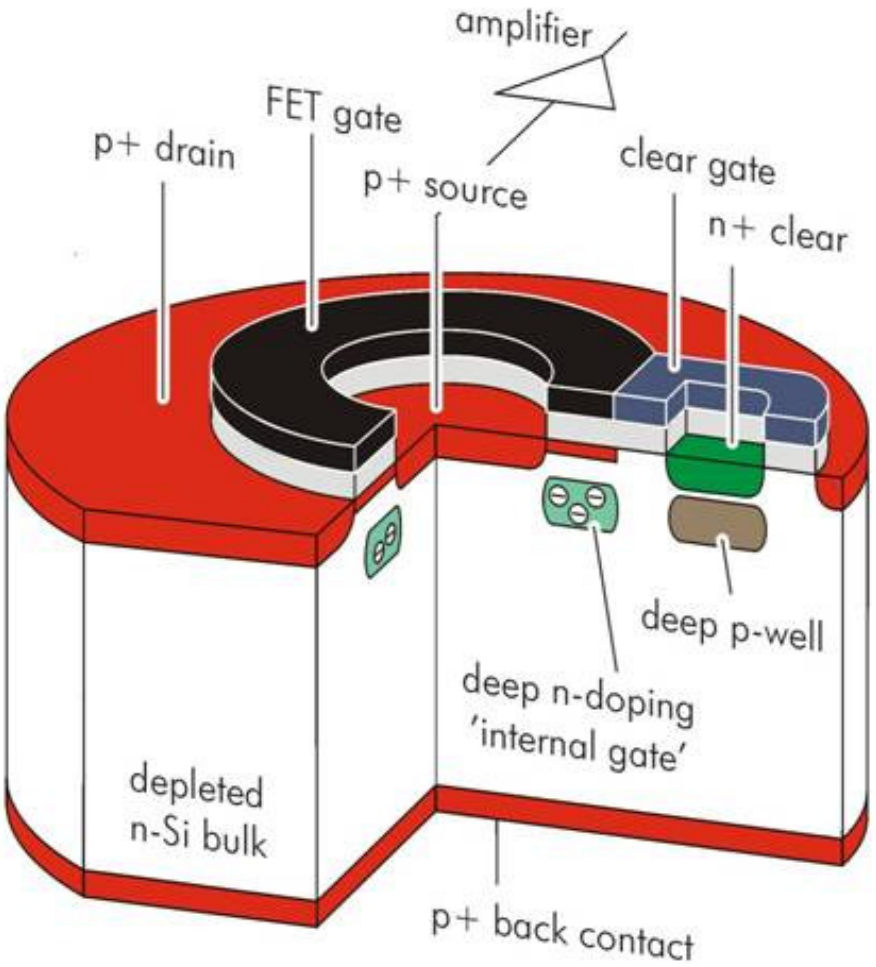
- Introduction
  - DEPFET - Principle of Operation
  - Thinned Devices
  - Module
- Switcher3 Steering Chip
  - Block Diagrams
  - Test Setup
  - Test Results
  - Sequencer
  - Power Consumption
- DCD1 Readout Chip
  - Block Diagrams
  - Layout

Introduction

DEPFET Principle of Operation

- A **p-FET** transistor is integrated in every pixel
- A **potential minimum for electrons** is created under the channel by **sideward depletion**
- Electrons are collected in the „internal gate" and **modulate the transistor current**
- Signal charge is removed via a clear contact

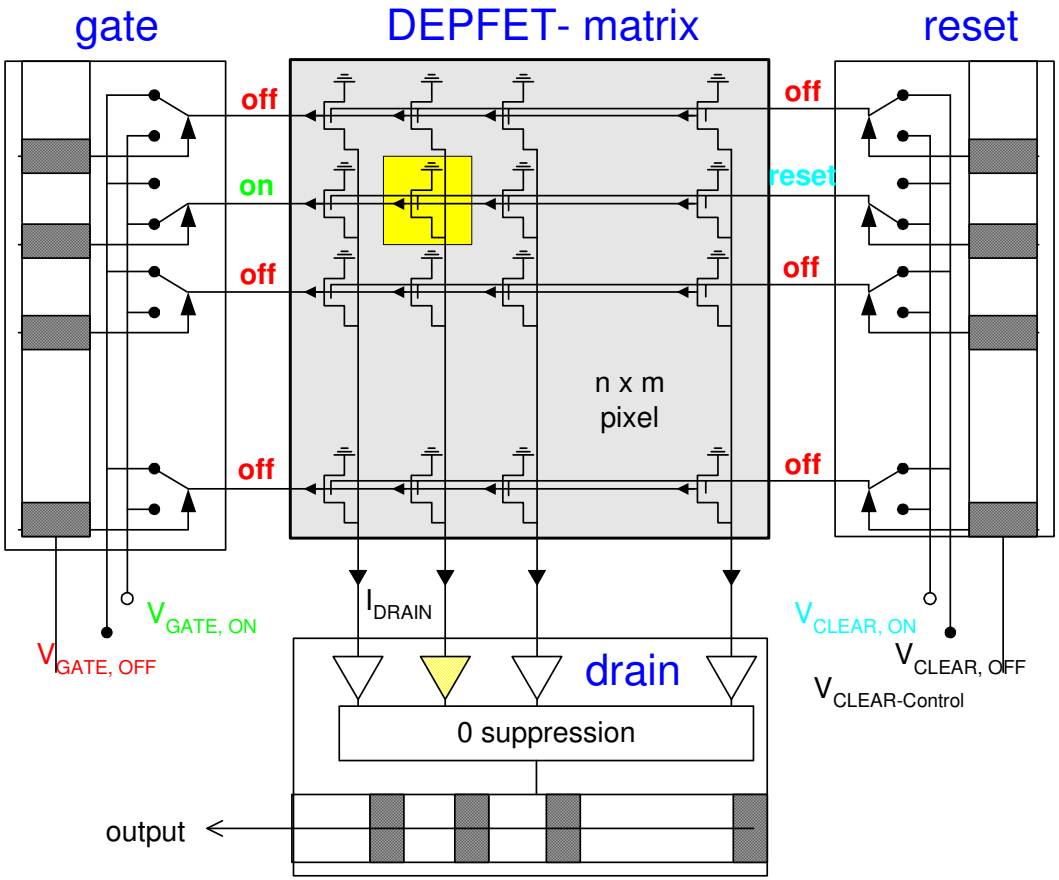


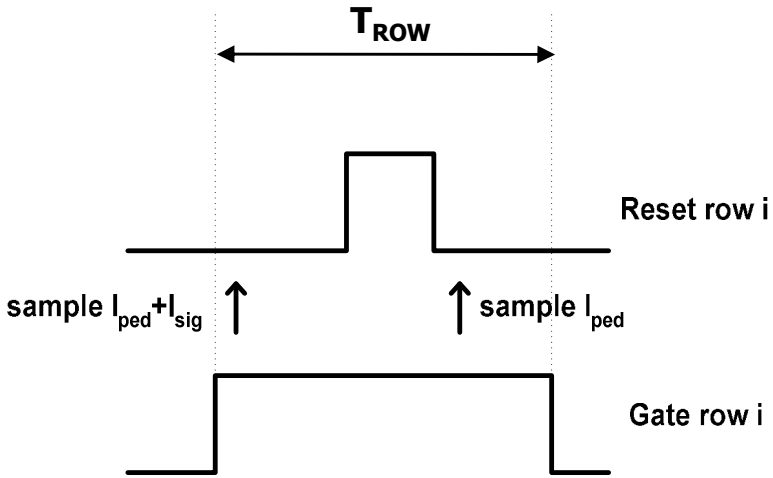


+ **Fast** signal collection in **fully depleted** bulk
+ **Low noise** due to small capacitance and **internal amplification**
+ Transistor can be **switched off** by external gate – charge collection is then still active !
+ Readout can be at the source ('voltage signal') or at the drain ('current signal')
- very special technology, only available at Semiconductor Lab ('HLL'), MPI Munich

DEPFET-Matrix

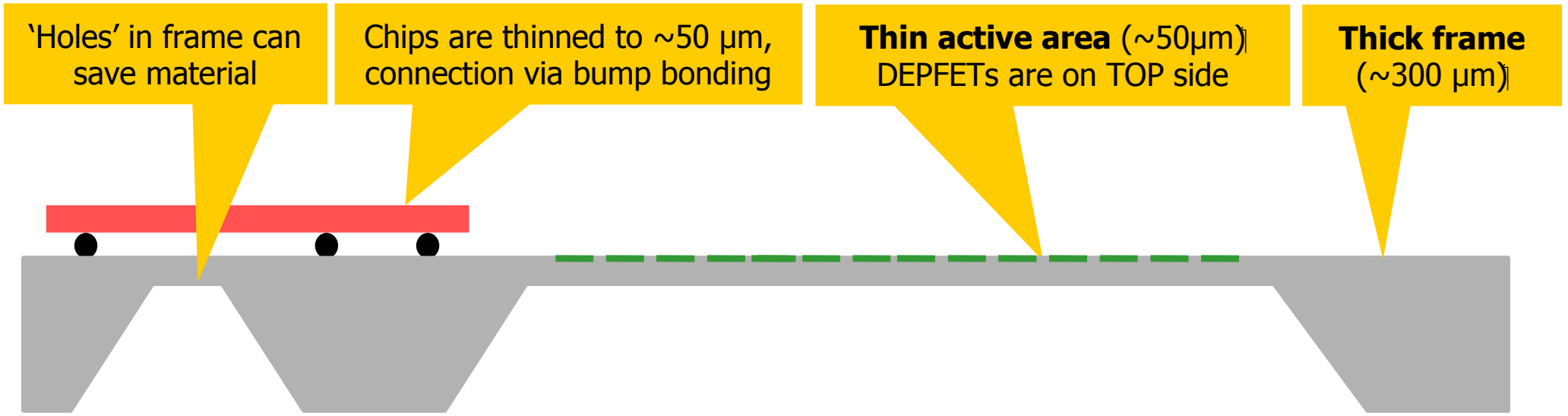
- Connect **gates and clears horizontally** to select / clear single rows: SWITCHER chips
- Connect **drains (or sources) vertically** and amplify current (or voltage): DCD chip
- Charge is not shifted!
- Readout sequence:
  Enable row – read current (I_{sig} + I_{ped}) – clear – read current (I_{ped}), subtract – move to next row

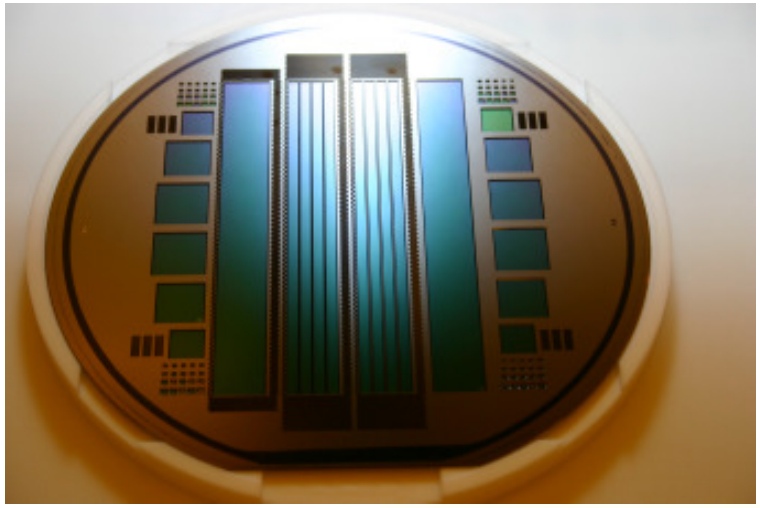


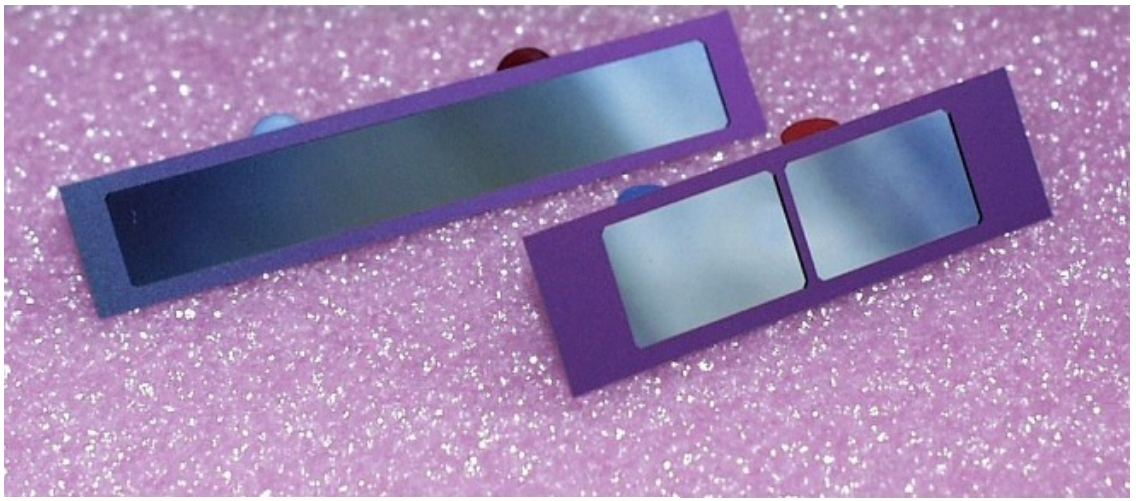


Readout sequence

Thinned Devices



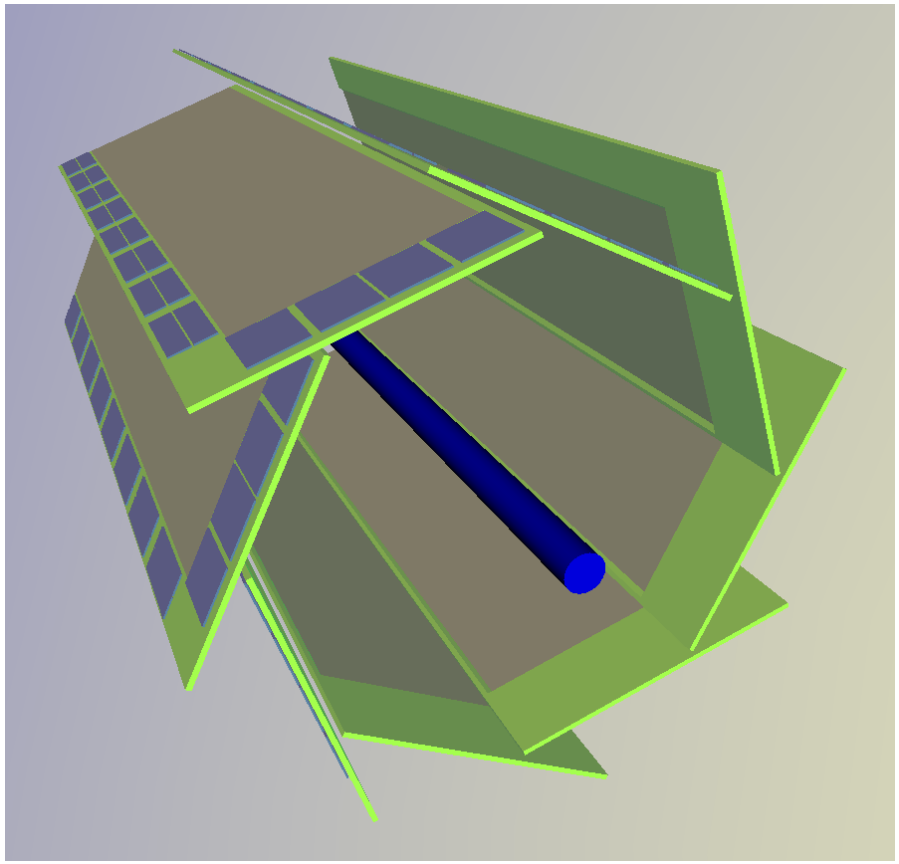


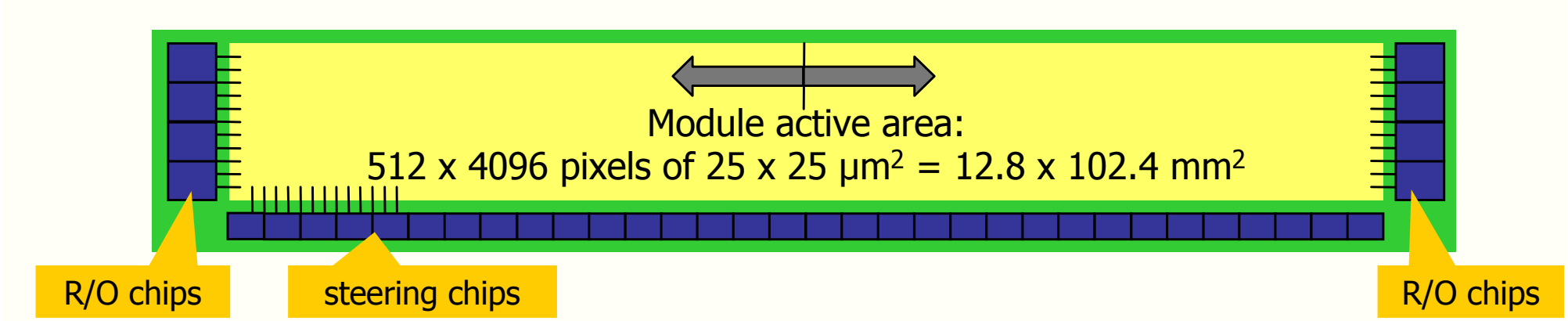


dummy samples: 50µm silicon with 350µm frame

Proposed Module Concept

- compact module designs
- smaller chips
- many channels
- gold stud bump bond can be done in the lab
- single chips are possible



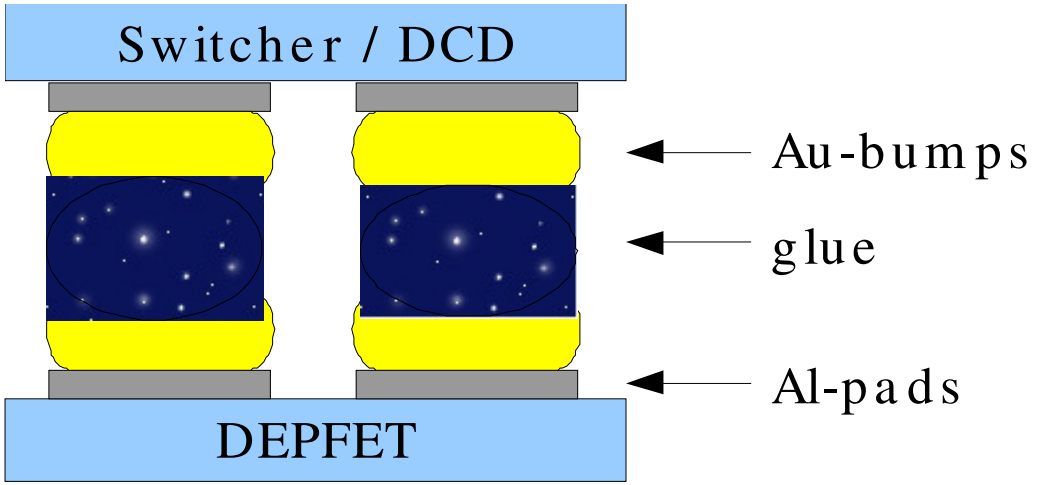


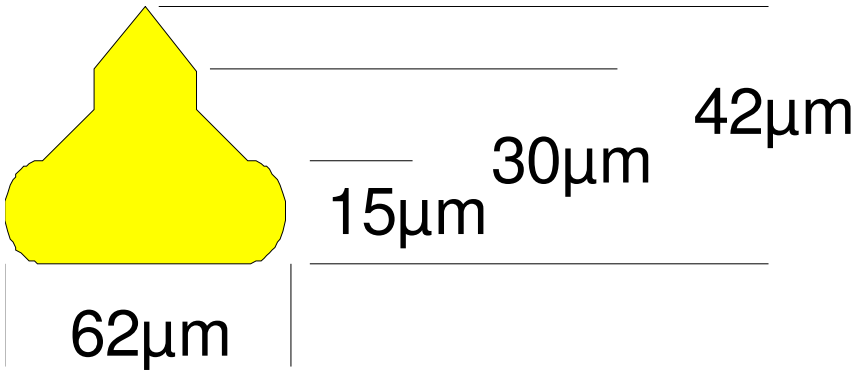
Interconnect Technology

- 60µm bump-pad diameter
- 100µm pad pitch
- added material:

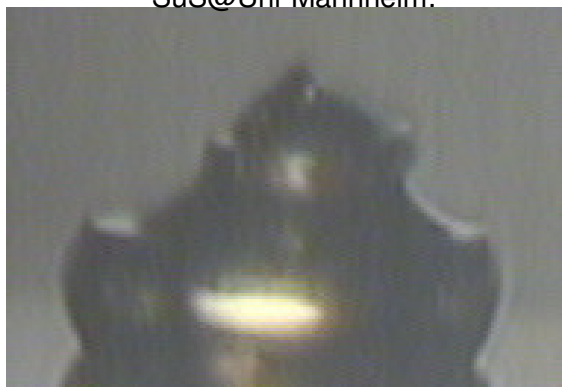
  4,5µm equivalent Si thickness

  across active area





SuS@Uni-Mannheim:



smashed ball, 48µm free-air-ball, 17,5µm wire

SuS@Uni-Mannheim:

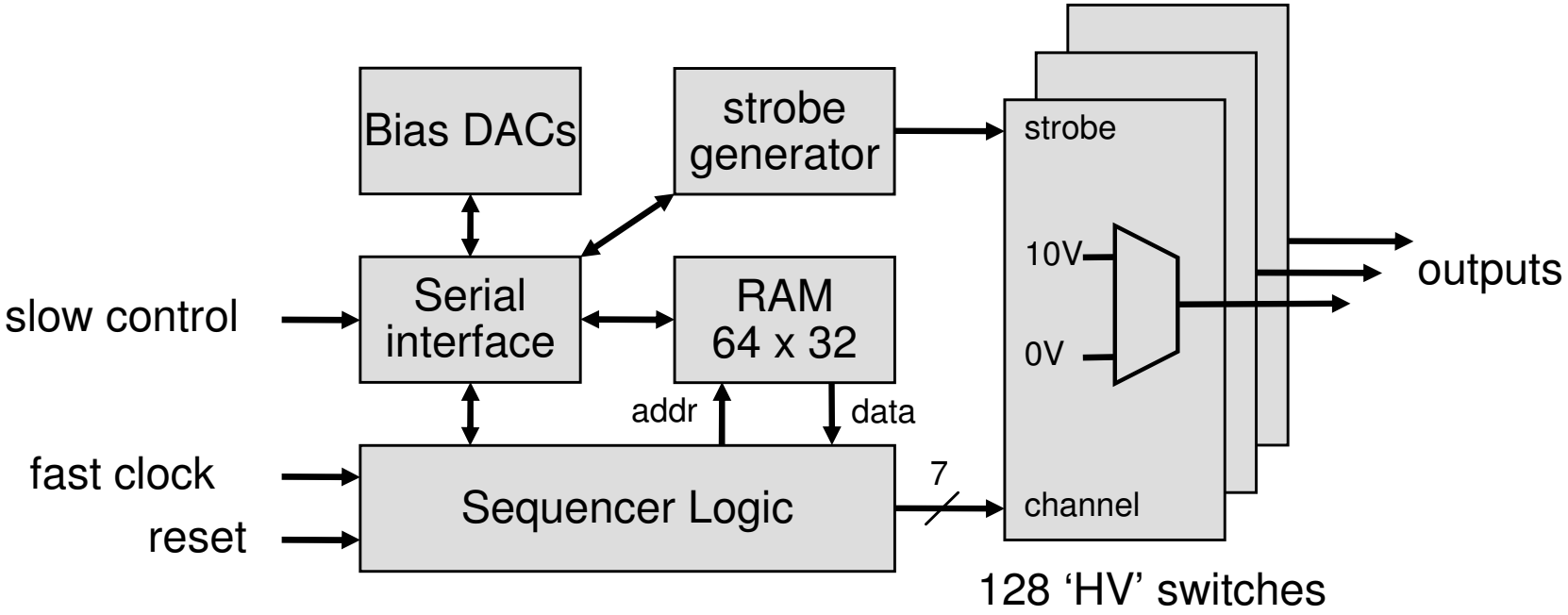
65µm smashed
25µm wire

Switcher3
DEPFET Steering Chip

Switcher3 Requirements

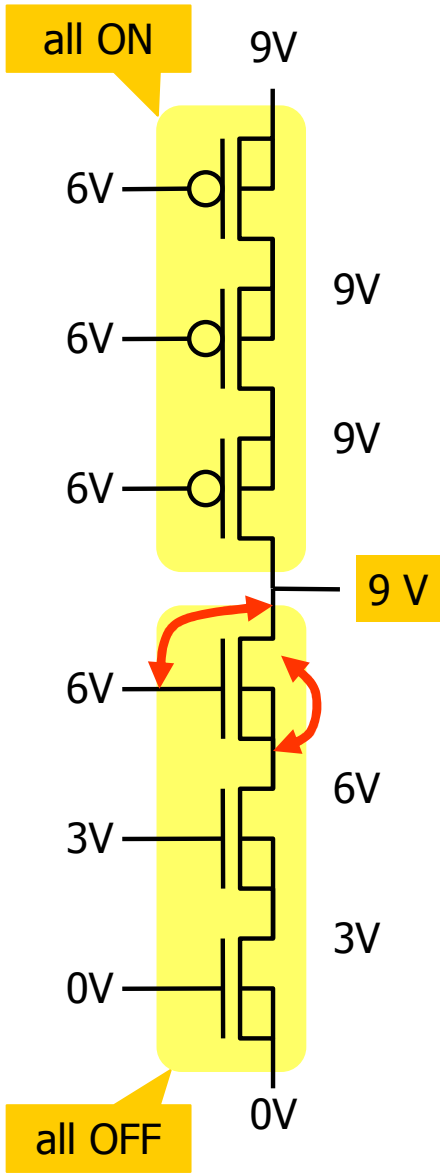
- steering chip for gate- and clear-signals
- high voltage **9V signals**
- **radiation hard** design
  - high voltage technology not suitable because of thick gate oxides
- 20pF matrix capacitance
- **fast** signal edges: <10ns risetime for 20pF load
- 128 channels
- not trivial **switching sequences**
- **bump** pitch of **180 µm, allows pixel sizes down to 24 µm**

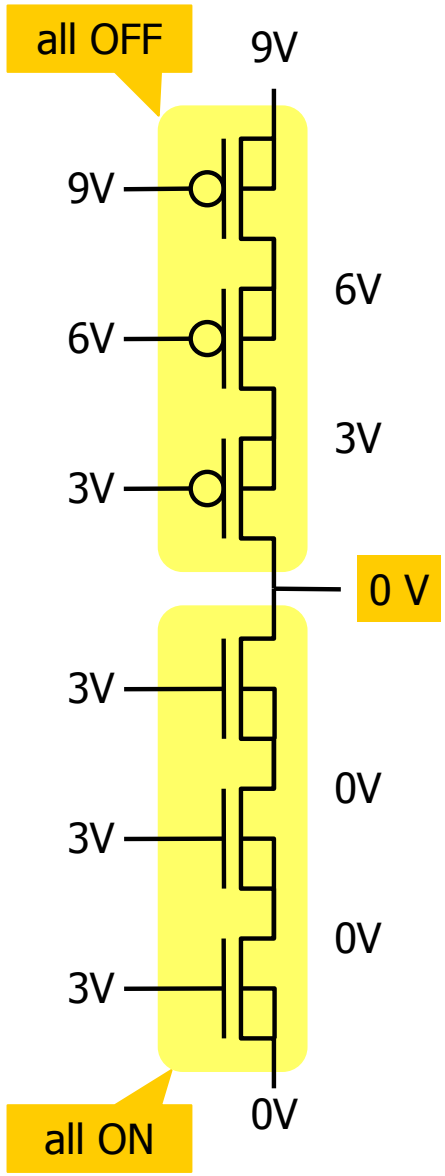
Block Diagram

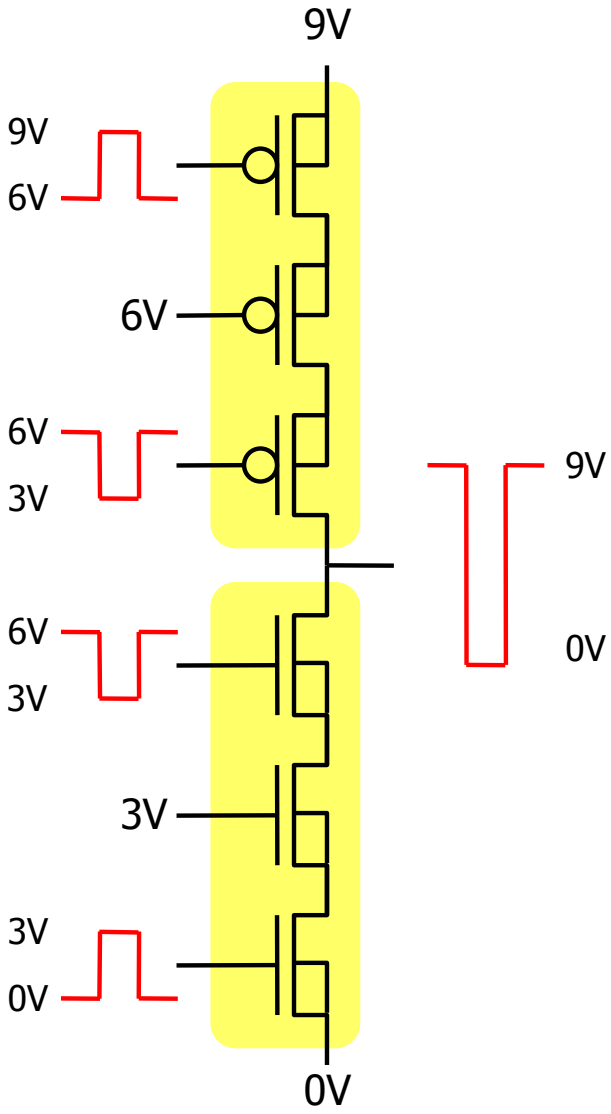


Stacked Transistors

- Use 3 **stacked transistors**. Assume 3V per stage: VDD = 3 x 3V = 9V

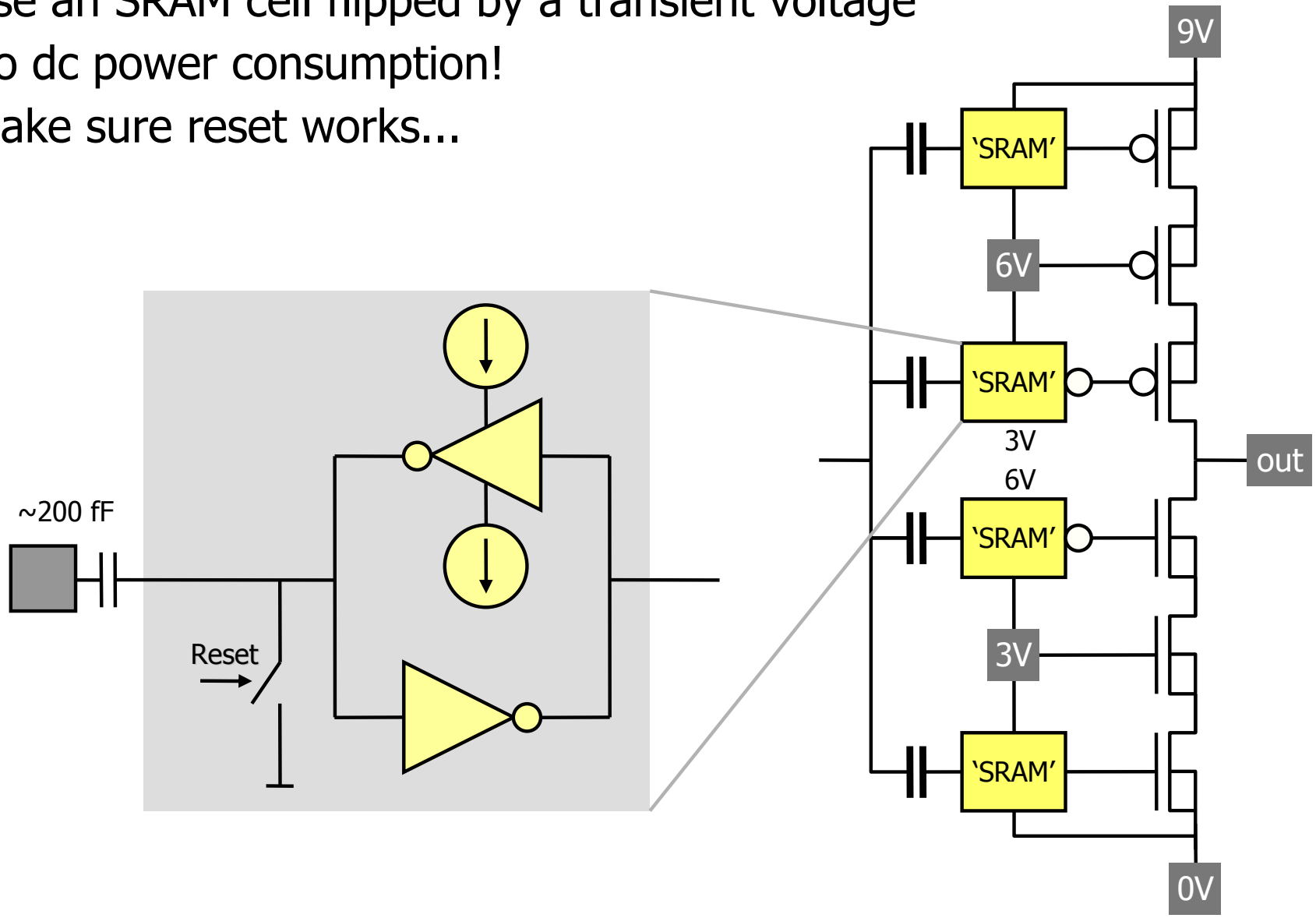




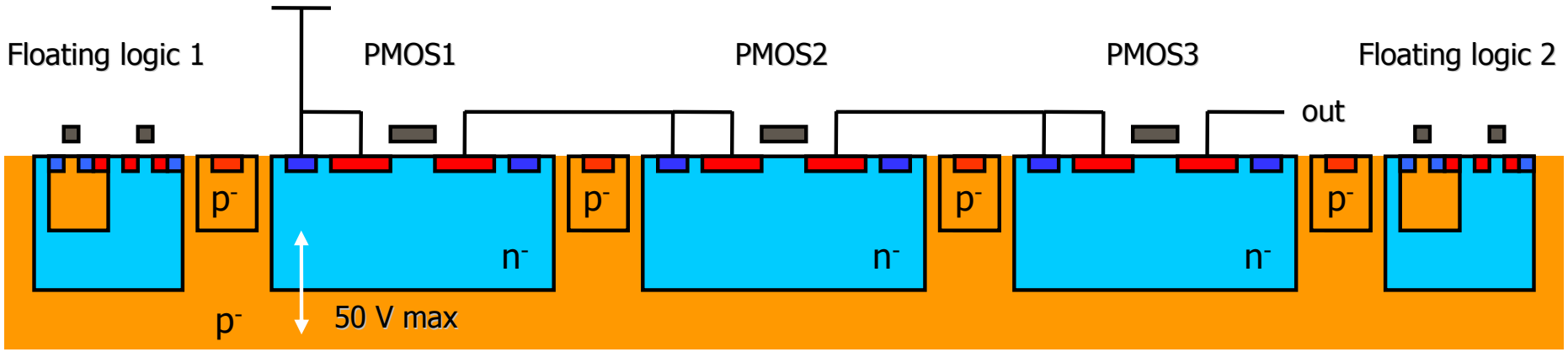


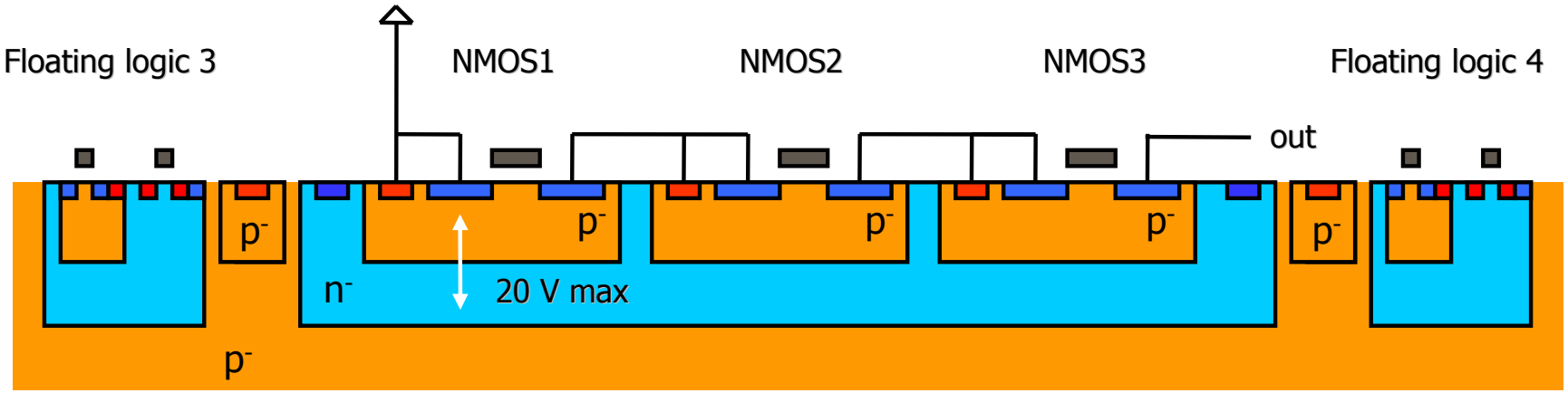
Cap Coupling

- Use an SRAM cell flipped by a transient voltage
- No dc power consumption!
- make sure reset works...



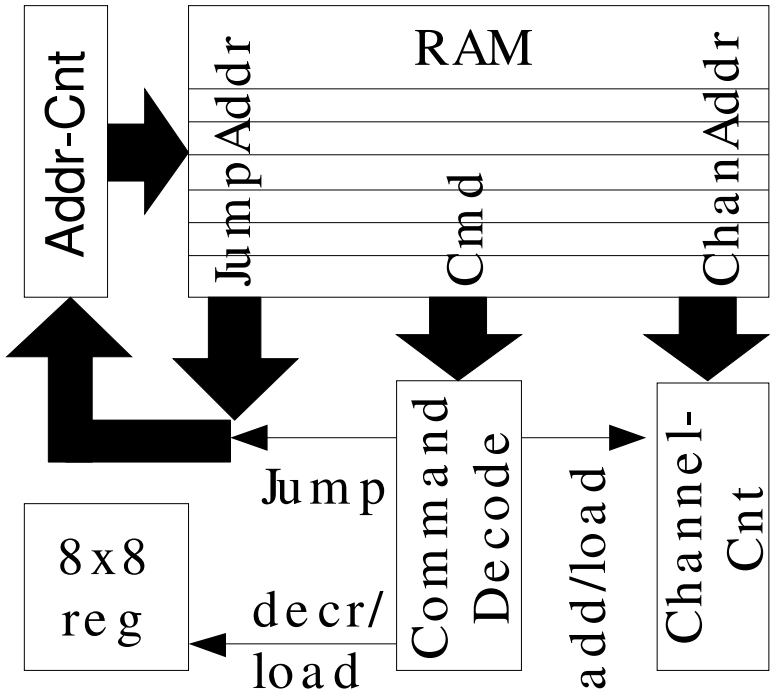
Cross Section – AMS h35b4 Twin Well

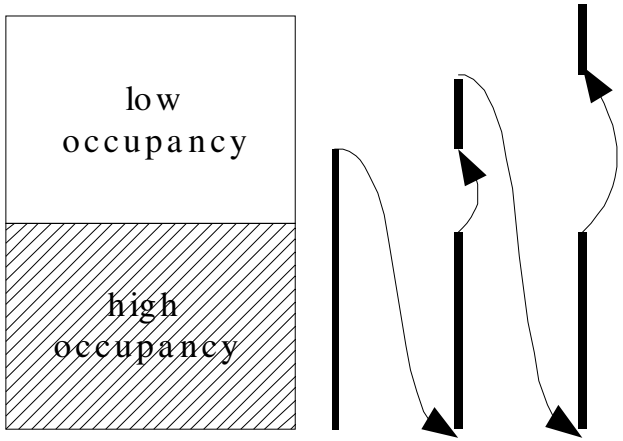




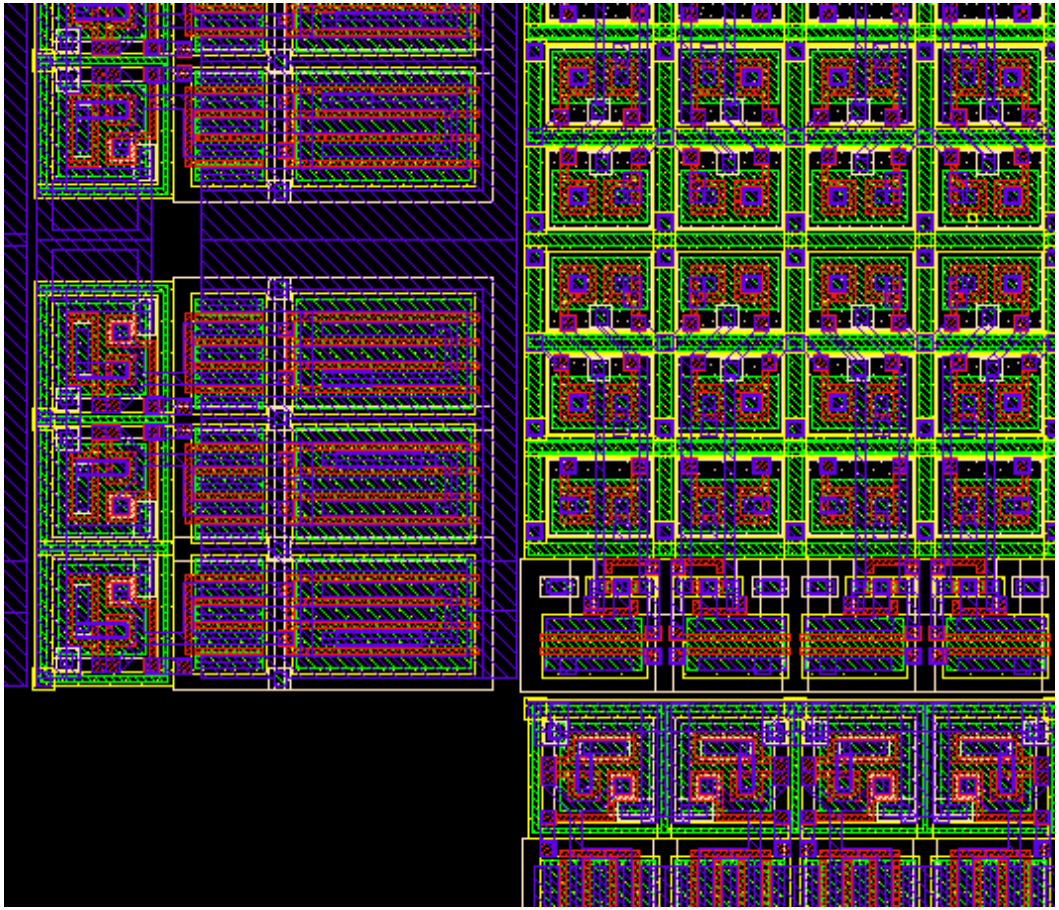
Sequencer

- May need nonlinear scans
  - scan high occupancy more often
- Simple but flexible
  - jumping, looping,
  - absolute/relative channel addressing
- 64 words program length

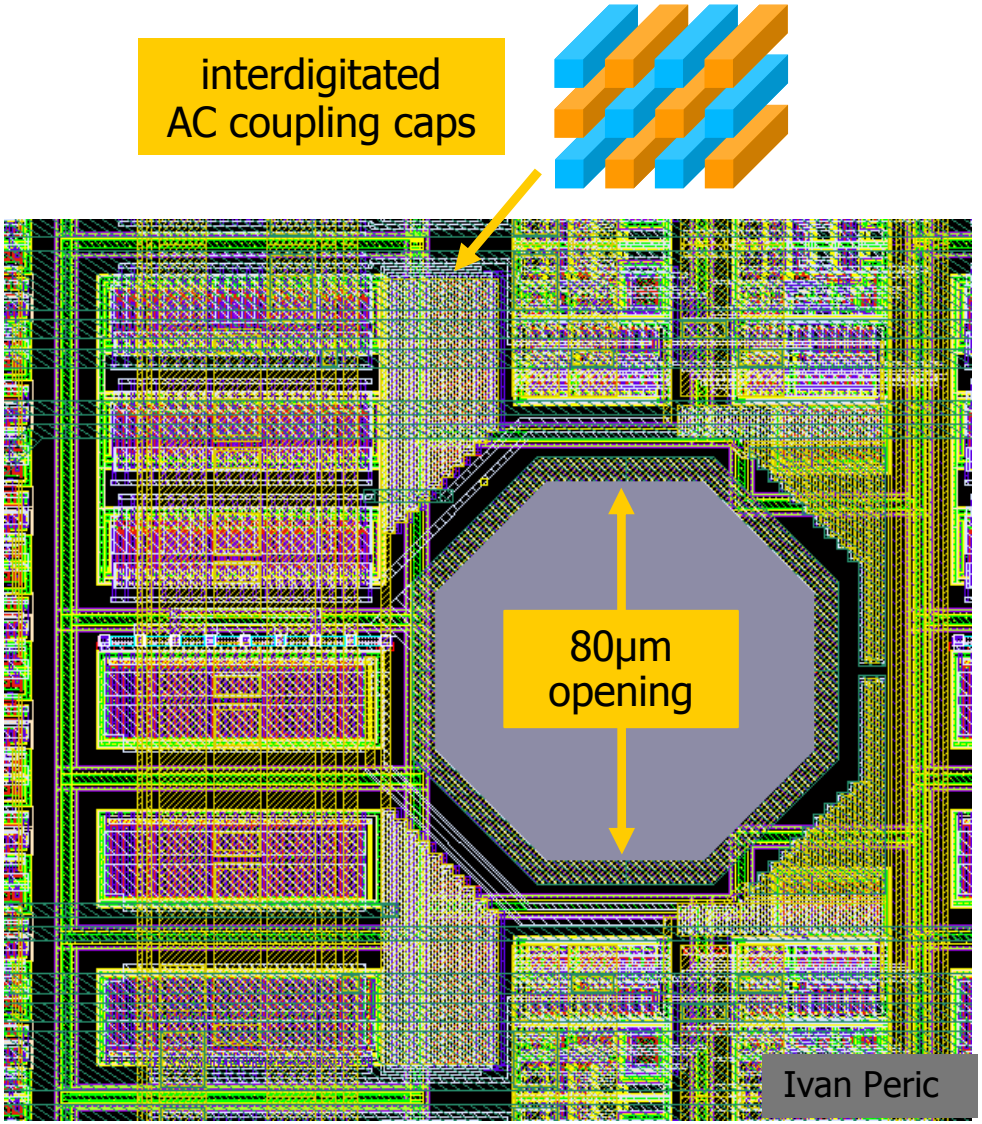




Layout



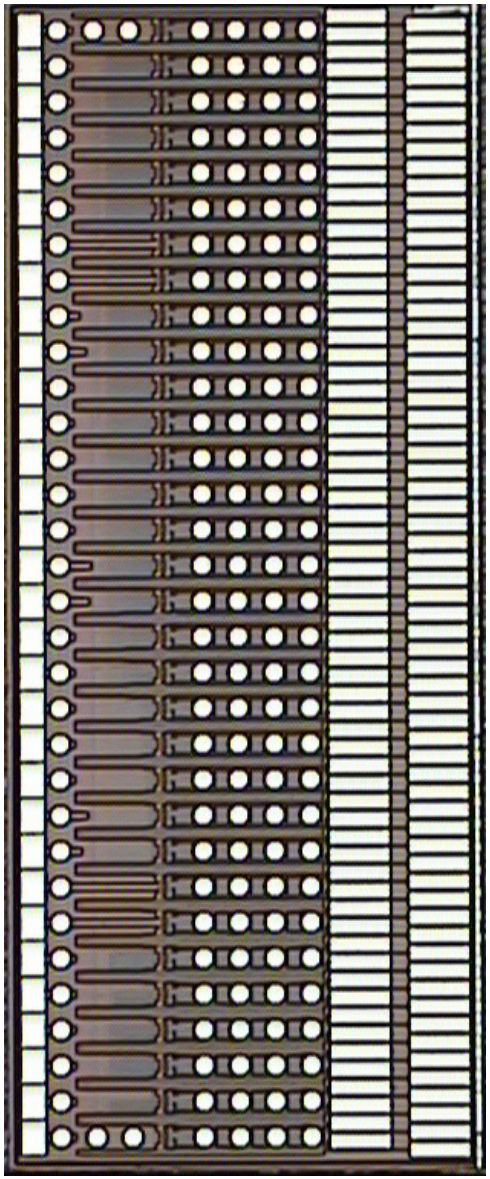
Sequencer RAM, row buffers, readout
(M2-M4 not shown)



HV channel with 3+3 Switch transistors and
4 AC coupling stages (180x180µm, M4 not shown)

Switcher3 features

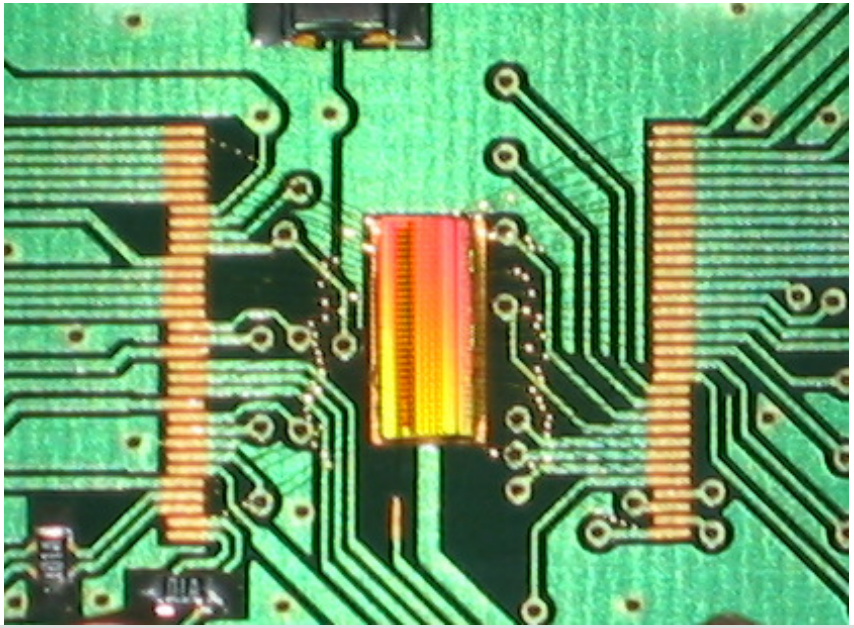
- 9V switching using three stacked 3.3V transistors
  - needs twin-well technology (AMS h35b4)
  - capacitive coupling of digital and analog blocks
- radiation hard design, no HV-transistors
- 128 channels
  - bump bonding, wire bonding for compatibility
- slow control interface
  - serial input, 8x 16bit registers
  - DAC-settings, RAM access, debugging
- sequencer
  - allows non trivial switching sequences
  - 4 commands, 64 lines program code length
- fast LVDS inputs
  - for sequencer clock and channel strobe signal

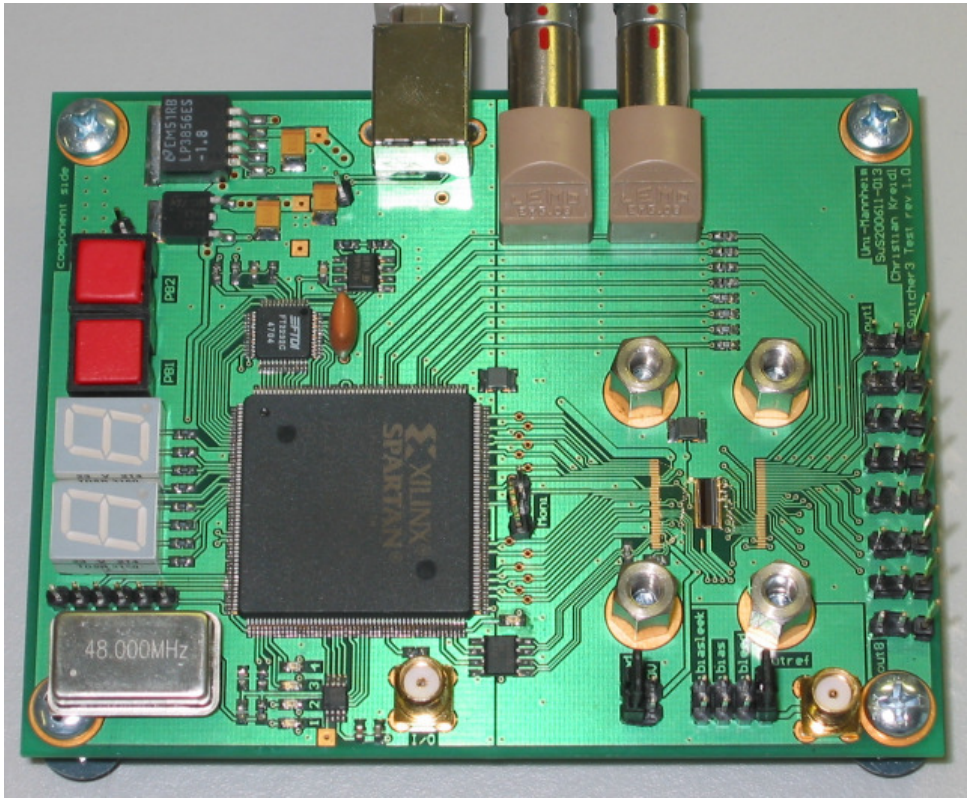


Switcher3
Test Setup

Test Setup - PCB

- 2-layer, gold plated PCB for Au-wire bonding
- Xilinx Spartan2E FPGA, USB-interface
- header for channel measurements
  - 0pF, 10pF, 22pF, 47pF load capacitors, 2 channels each

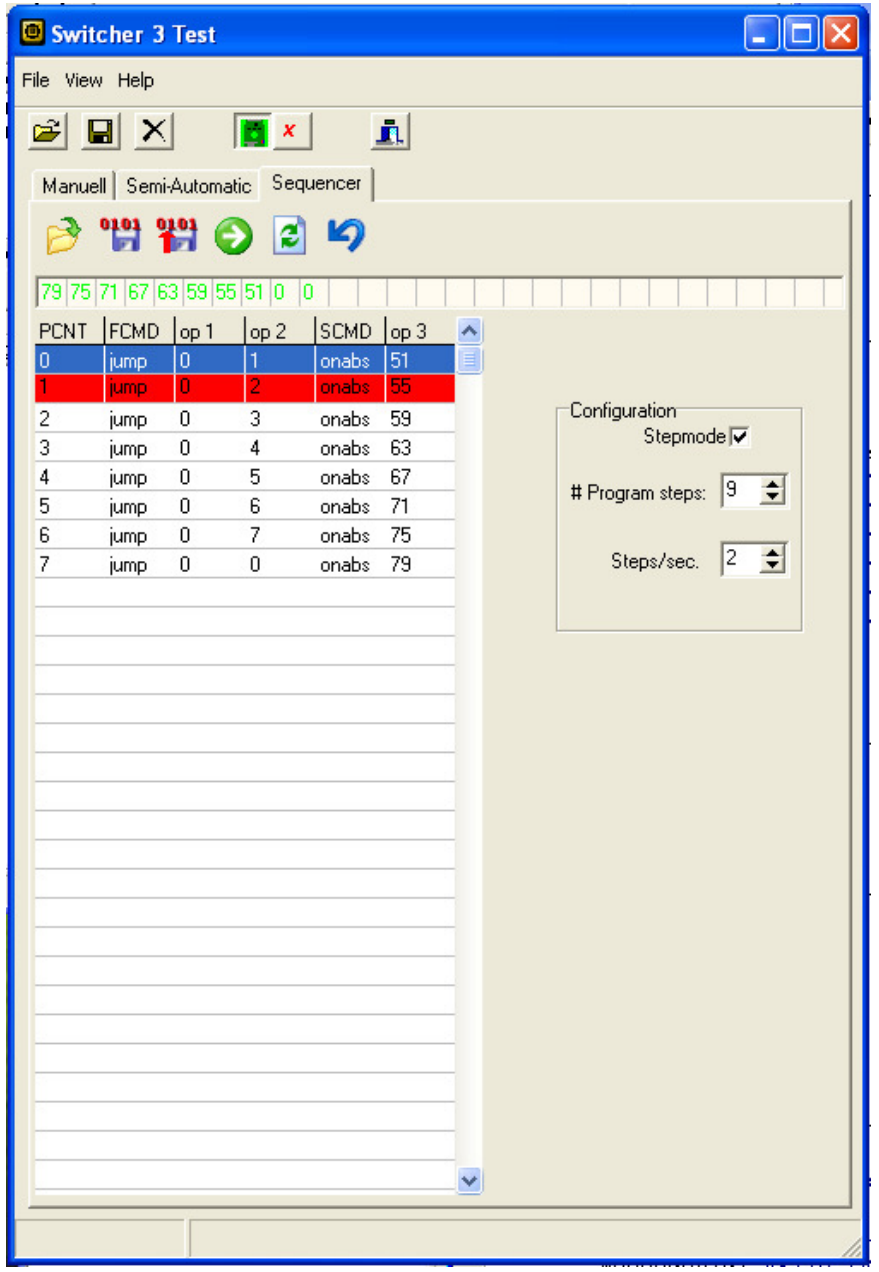




  - power consumption measurements
    - 22pF, 47pF on 8 channels each

Test Setup - Software

- accessing the sequencer
  - loading „assembler" code from file
  - compiling to binary format
  - uploading to Switcher3 RAM
- simulating sequencer code
  - displays selected channel number and status
  - highlights current row

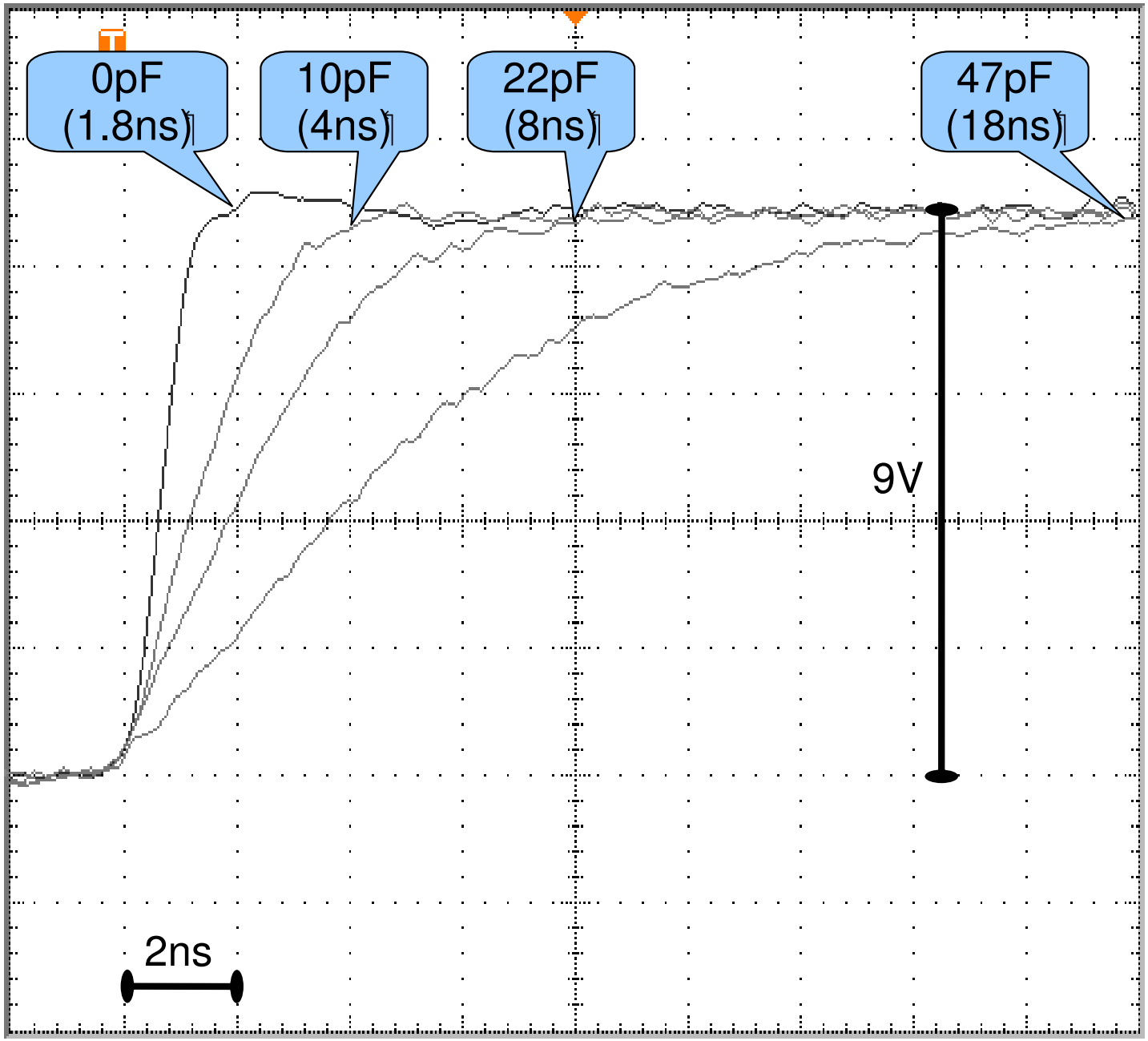


Switcher3
Test Results

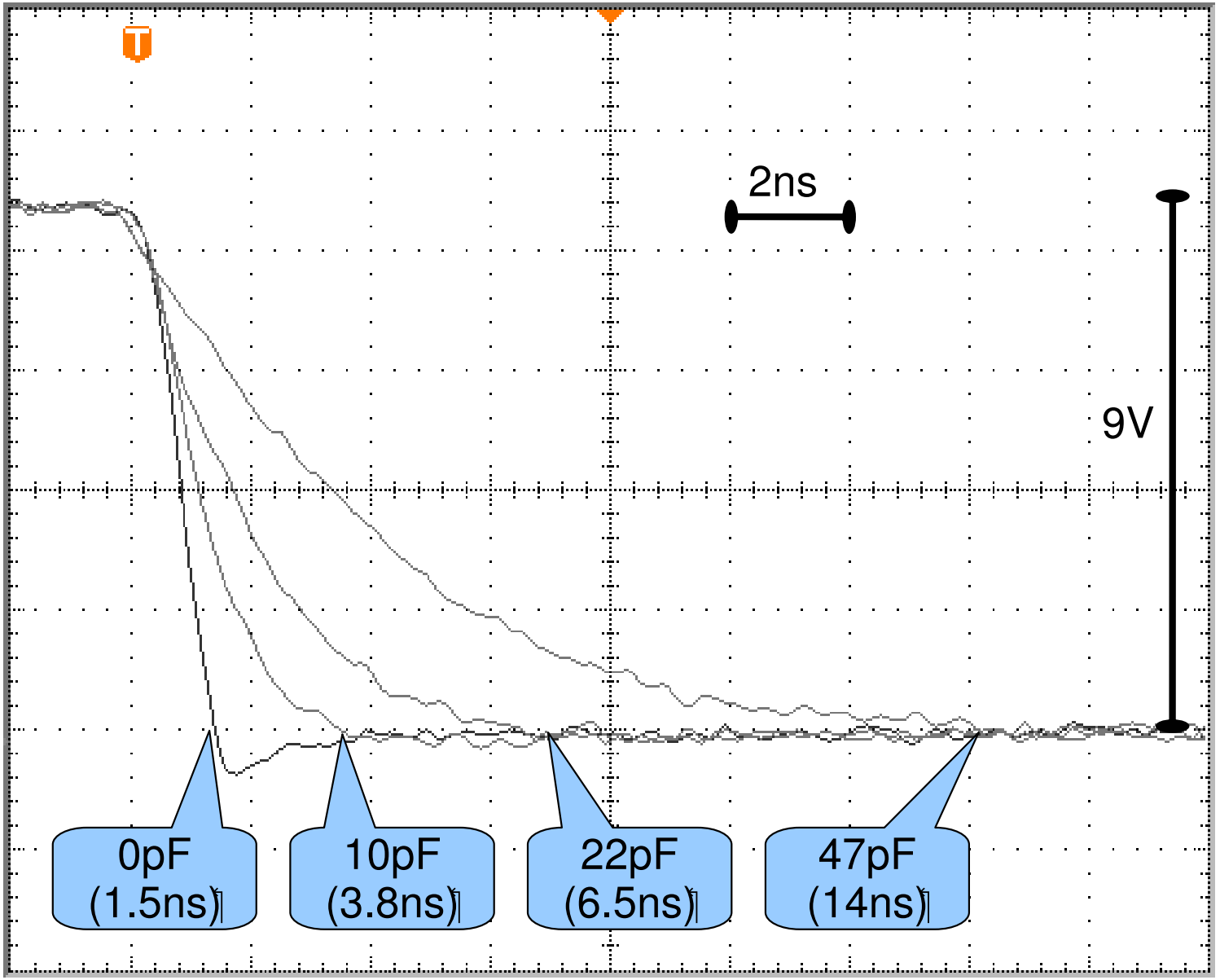
Test Results

- digital part is working
  - RAM, DACs, Sequencer, Slow Control, LVDS are ok
- stacked transistors work
  - full swing between 0V and 9V
  - even 10V are possible
  - fast rising edge
  - slightly faster falling edge, as expected and wanted

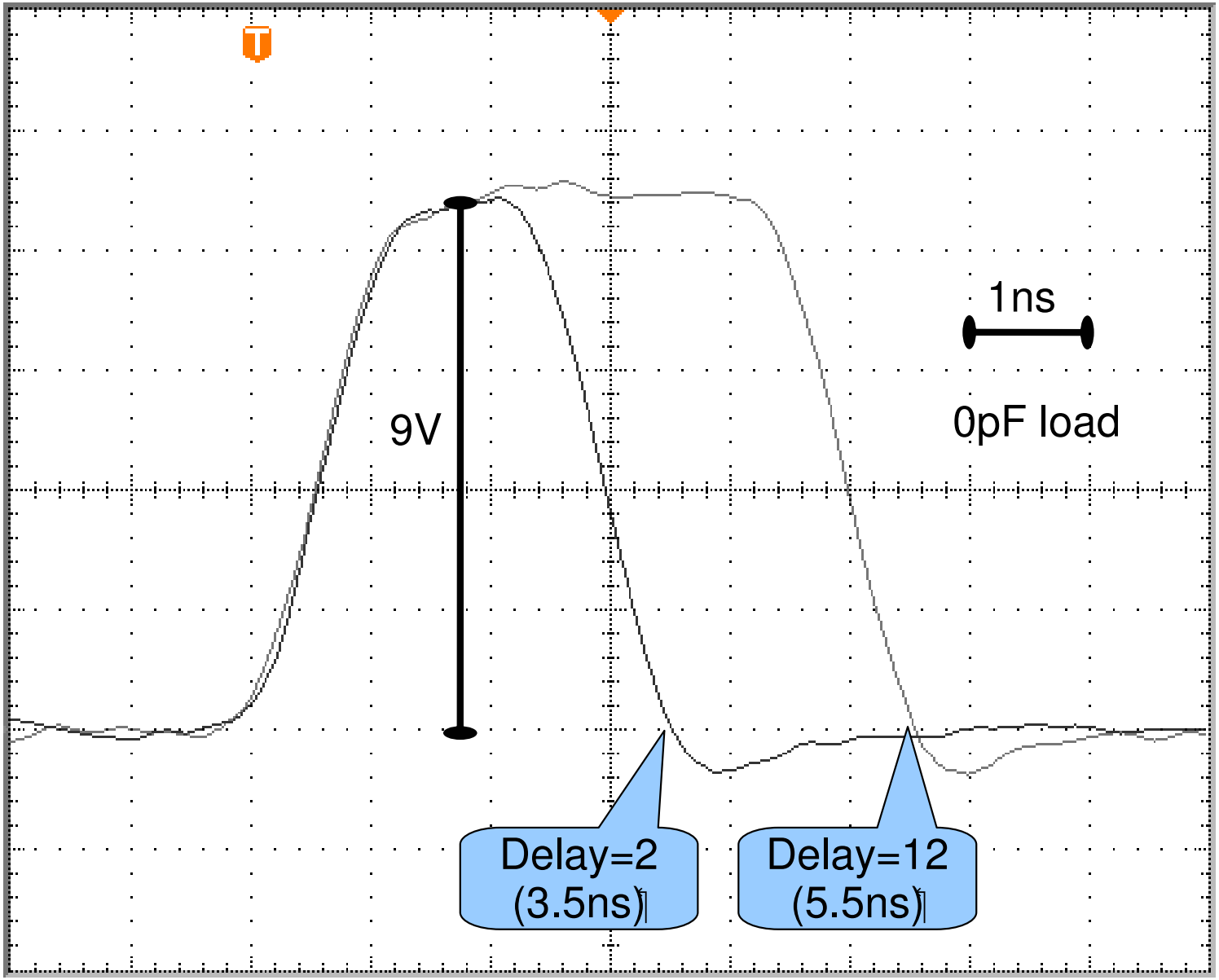
Analog Test - Rising Edge vs. C_{load}



Analog Test - Falling Edge vs. C_{load}



Analog Test – Internal Strobe Generator



Switcher3 Sequencer

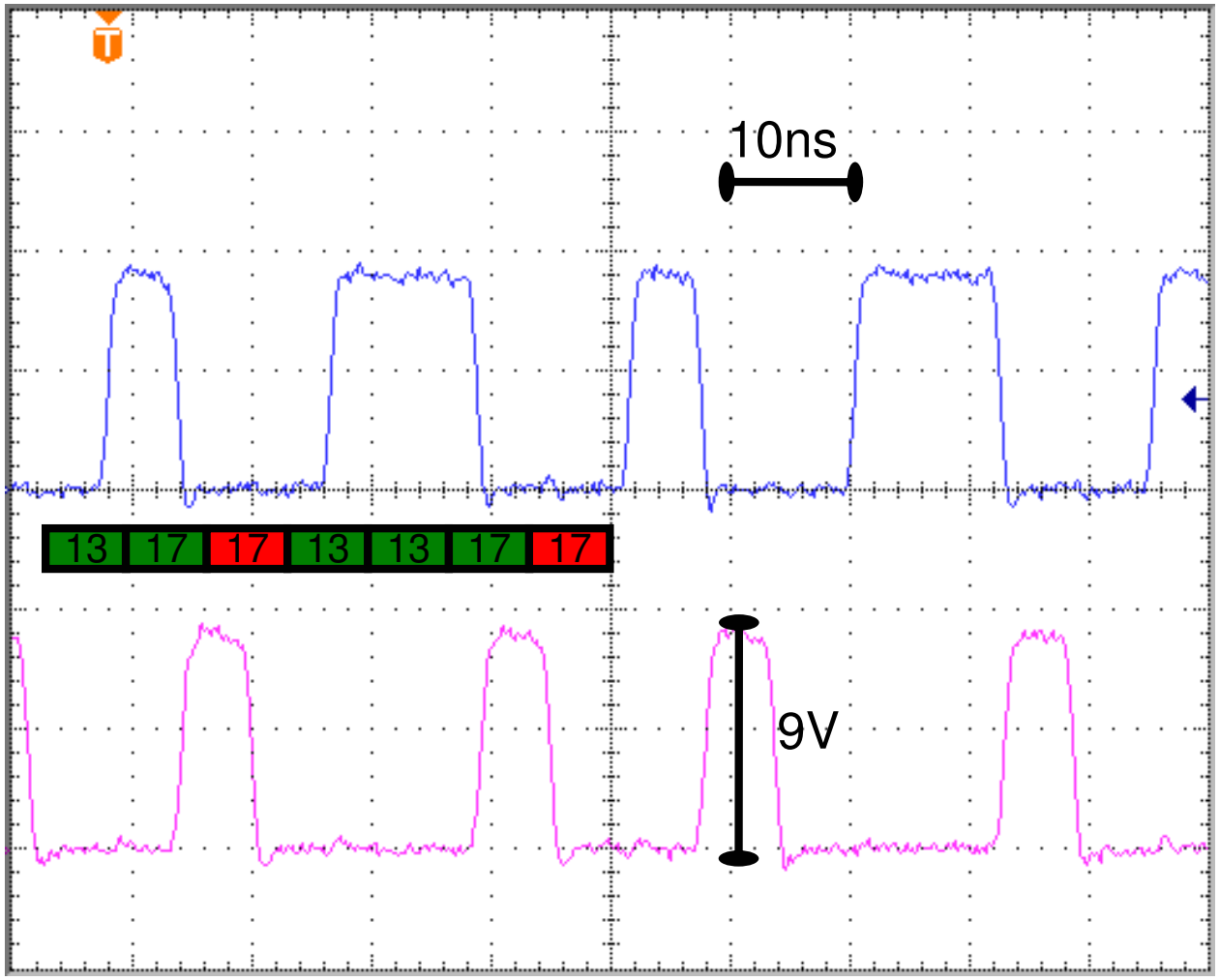
Sequencer - Commands

- 64 RAM lines, i.e. command lines
- 4 commands
  - JUMP: jump <addr> <chanCMD> <chanNr>
  - LOAD: load <reg> <value> <chanCMD> <chanNr>
  - BNZDEC: bnzdec <reg> <jumpaddr> <chanCMD> <chanNr>
  - JMP_COND: jmp_cond <addr> <chanCMD> <chanNr>
- chanCMD
  - switches channel on or off
  - channel addressing can be absolute or indirect
  - on / off: add chanNr to channel counter, negative values allowed
  - onabs / offabs: chanNr is absolute
- 8 registers for looping using BNZDEC command
  - 8bit wide
  - coding done via complicated LFSR

Sequencer - Maximum Speed

150MHz
0pF

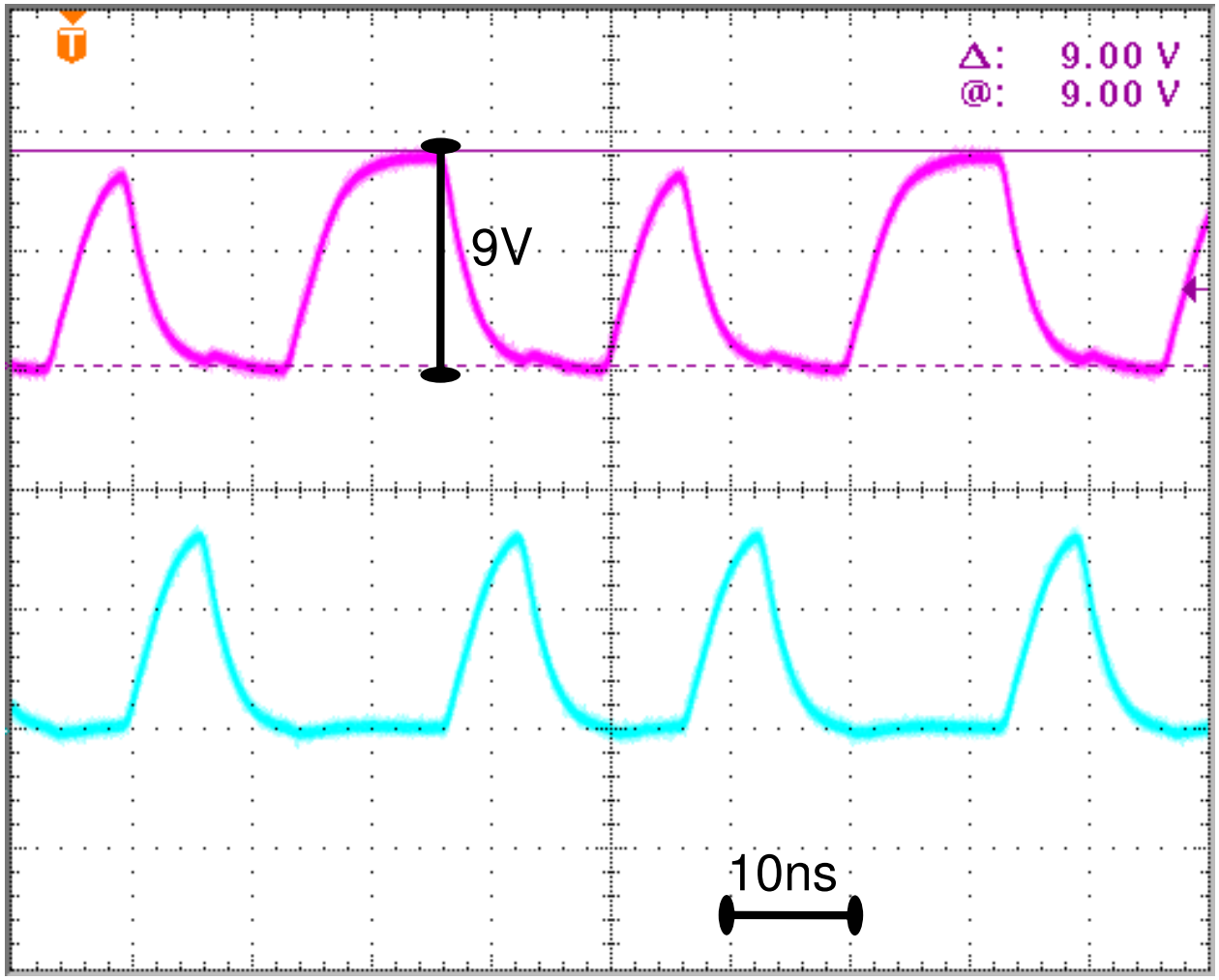
```
0:  jump  1  onabs   13
1:  jump  2  onabs   17
2:  jump  3  offabs  17
3:  jump  4  onabs   13
4:  jump  5  onabs   13
5:  jump  6  onabs   17
6:  jump  0  offabs  17
```



Sequencer - Maximum Speed with C_{load}

150MHz
22pF

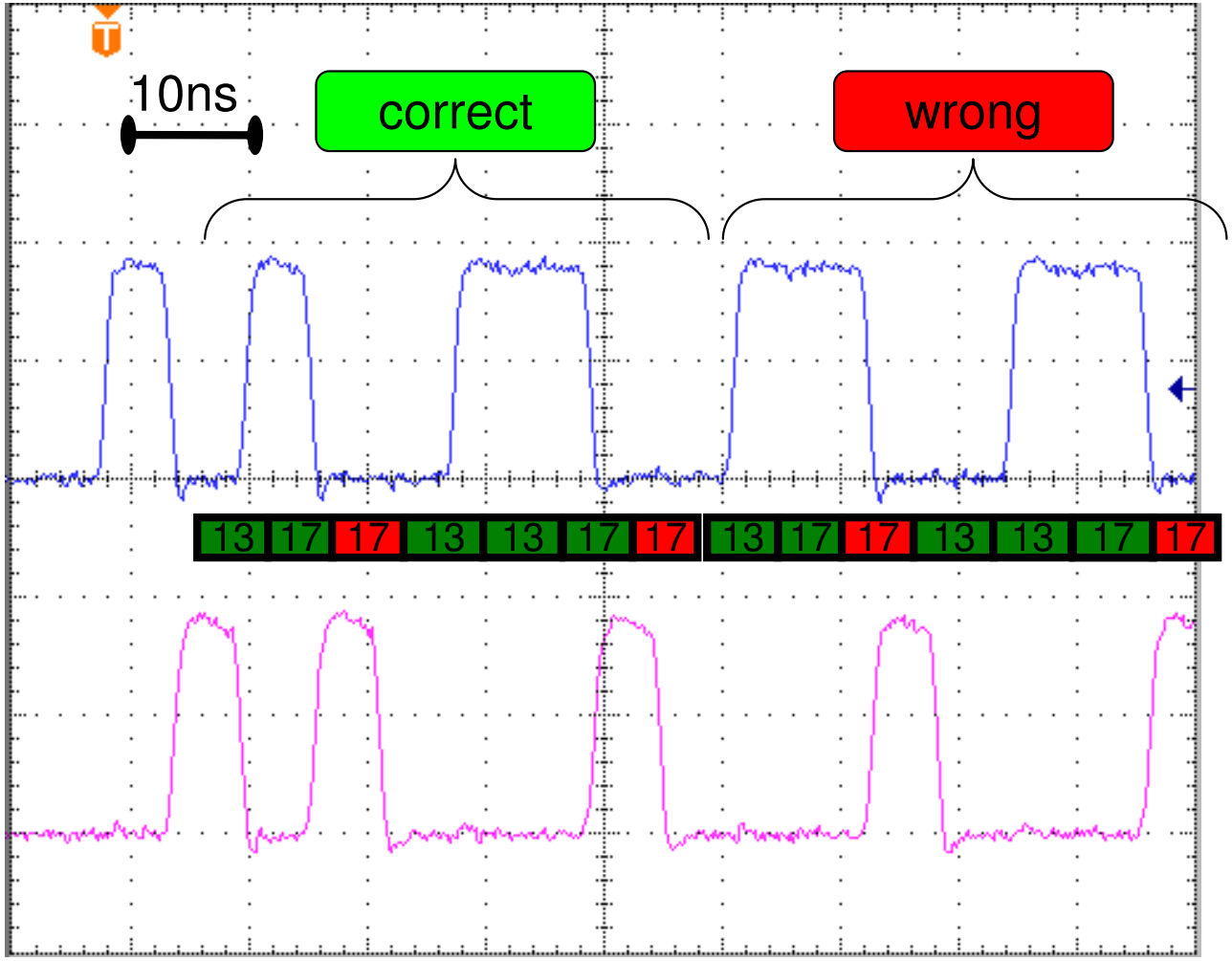
```
0: jump 1 onabs  29
1: jump 2 onabs  33
2: jump 3 offabs 33
3: jump 4 onabs  29
4: jump 5 onabs  29
5: jump 6 onabs  33
6: jump 0 offabs 33
```



Sequencer - Too Fast

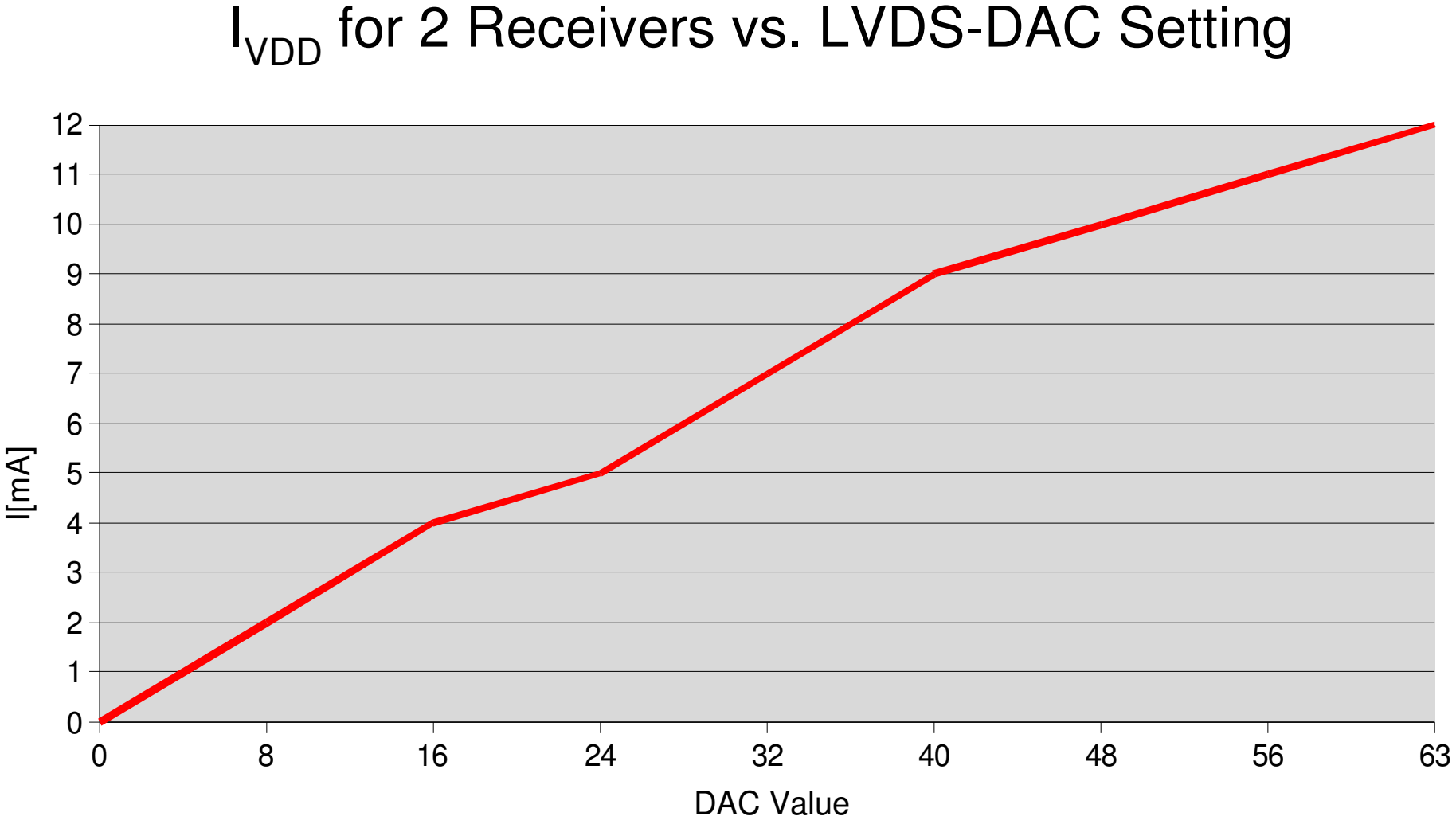
160MHz
0pF

```
0:  jump 1 onabs  13
1:  jump 2 onabs  17
2:  jump 3 offabs 17
3:  jump 4 onabs  13
4:  jump 5 onabs  13
5:  jump 6 onabs  17
6:  jump 0 offabs 17
```

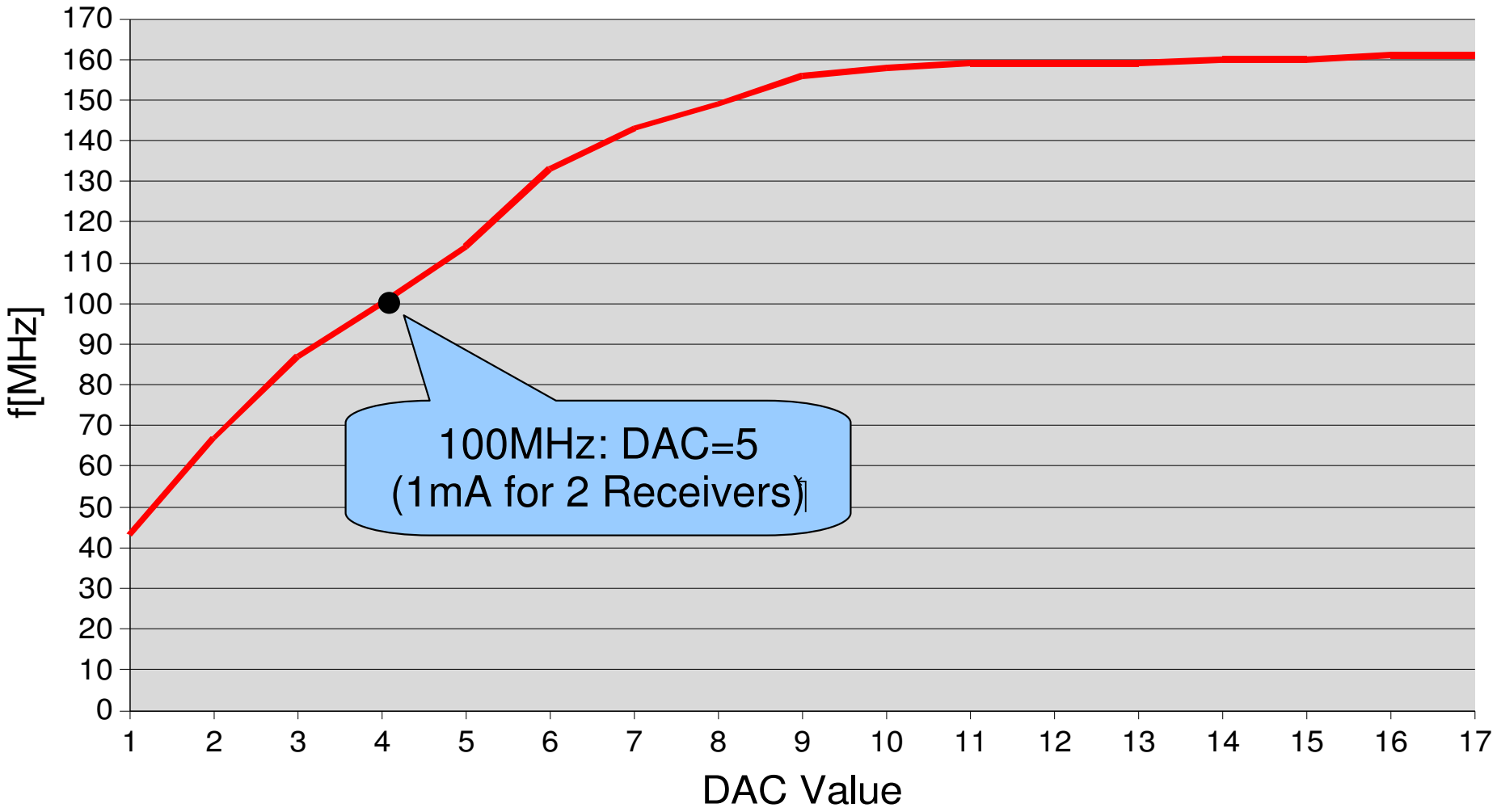


Switcher3
Power Consumption

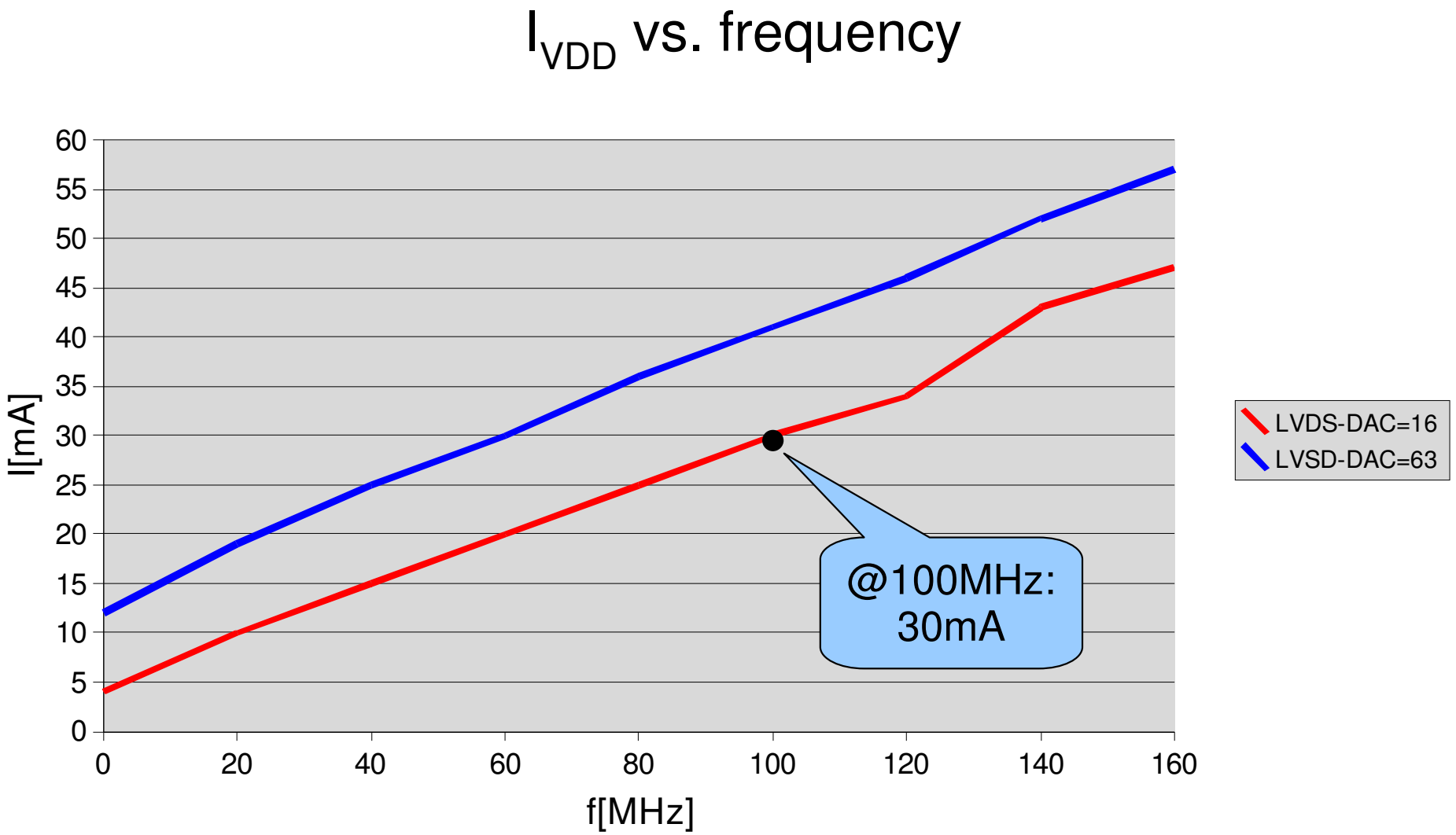
Power Consumption - LVDS Receivers



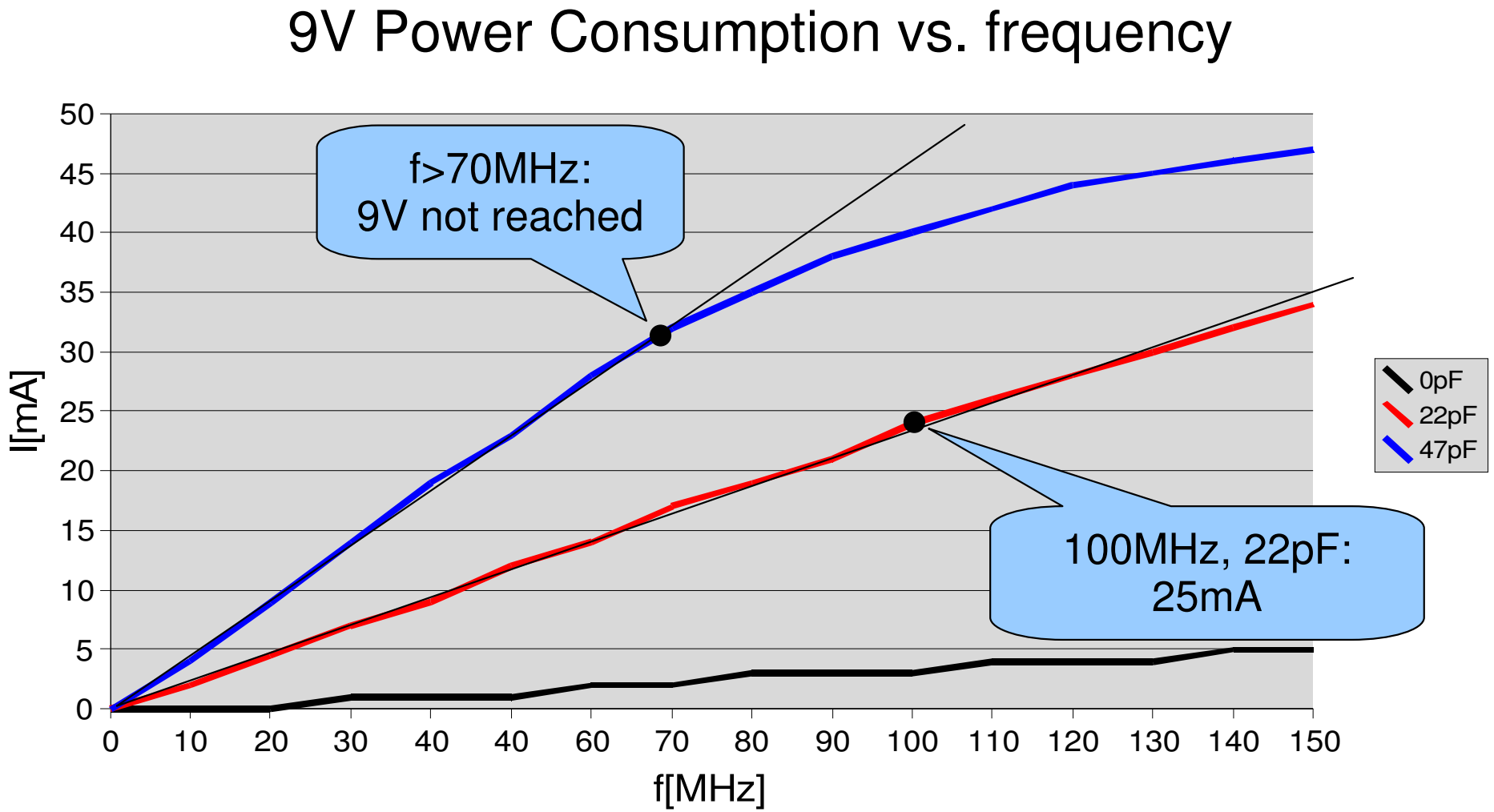
Speed vs LVDS-DAC



Power Consumption - Digital Part



Power Consumption - Analog Part



- no current on 6V and 3V supplies
- sequence cycling through 8 capacitors for each value
- Theory: $I = C \times U \times f = (22pF + \approx 6pF) \times 9V \times 100MHz = 25{,}2mA$

Summary

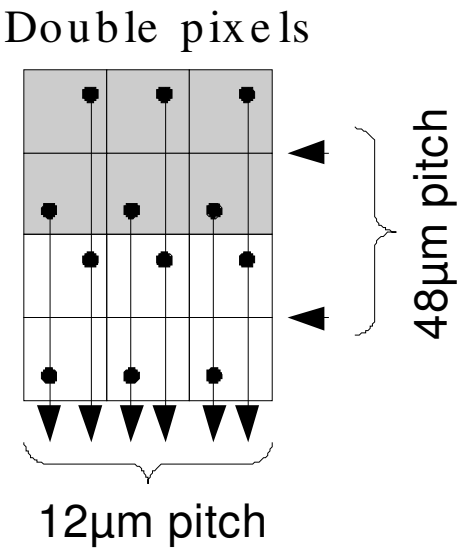
- Summary
  - all parts of chip are working
  - 150MHz max speed
  - 25mA on 9V supply for 22pF load @100MHz
  - 30mA on VDD @100MHz
  - 8ns settling time from 0V to 9V on rising edge
  - 6.5ns settling time from 9V to 0V on falling edge

- Next Steps
  - irradiation (test structures were unaffected by ~1 Mrad)
  - long term stress test (no failures after 6 weeks)
  - operation with DEPFET matrices

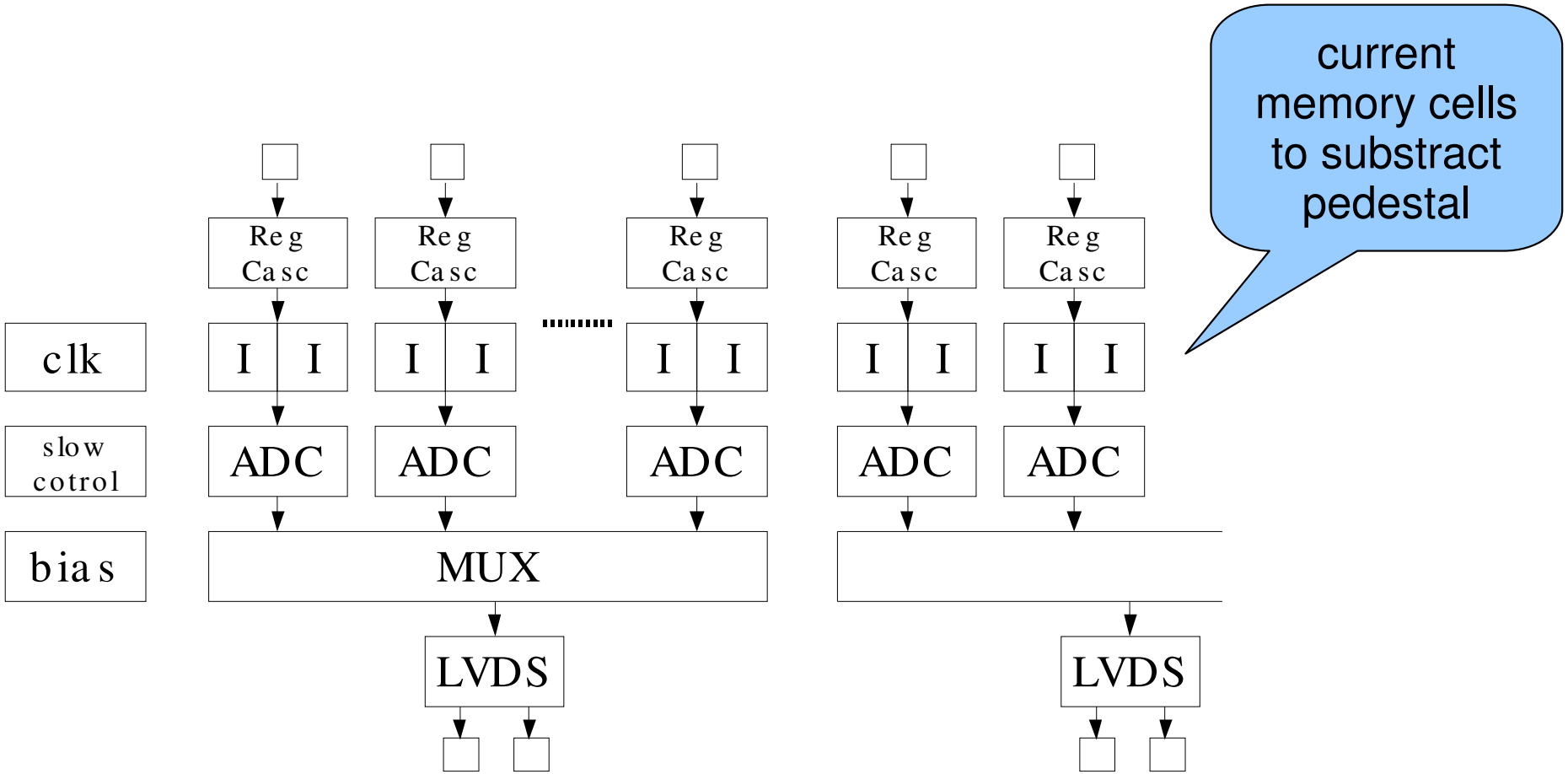
Drain Current Digitizer - DCD1
DEPFET readout chip

DCD1 Requirements

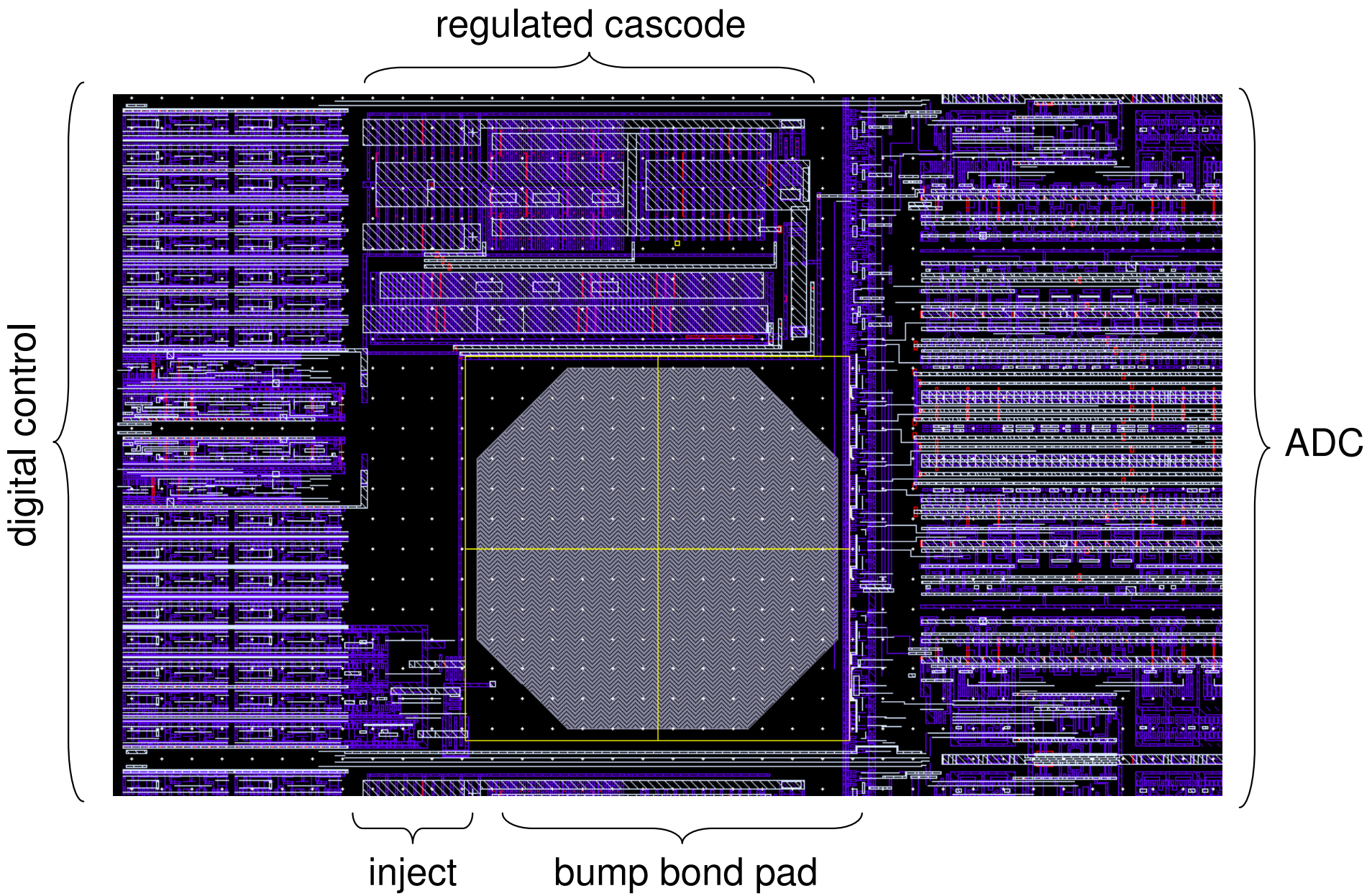
- Matrix organized as double pixels
  - 48µm Switcher steering pitch
  - **12µm** DCD readout pitch
- Iped ~ 30µA
- Isig ~ 6µA
- Large detector capacity ~40pF
  - 2000 pixels + 5cm bus
- Speed goal: 32MHz (16MHz double row rate)



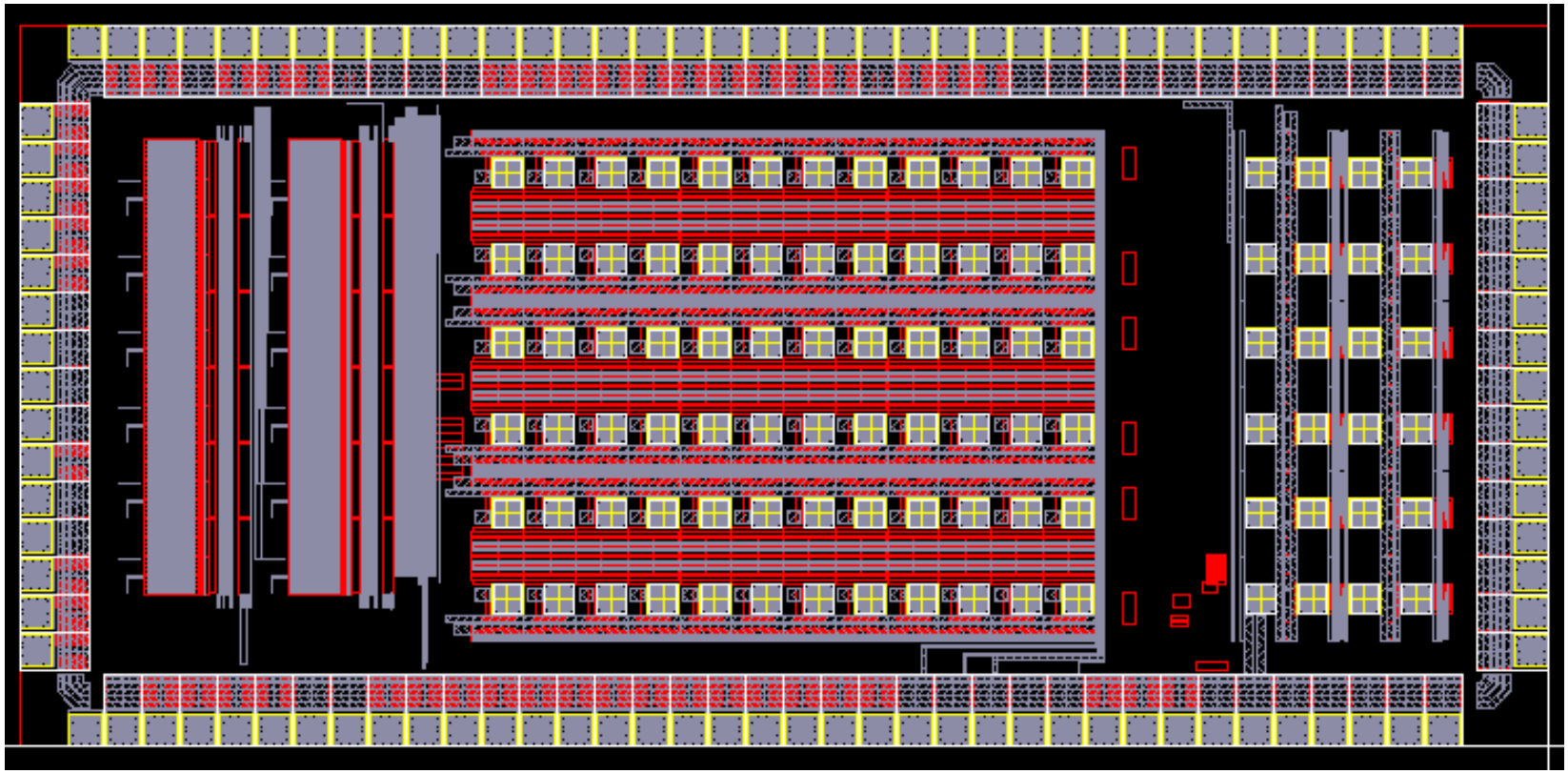
Block Diagramm



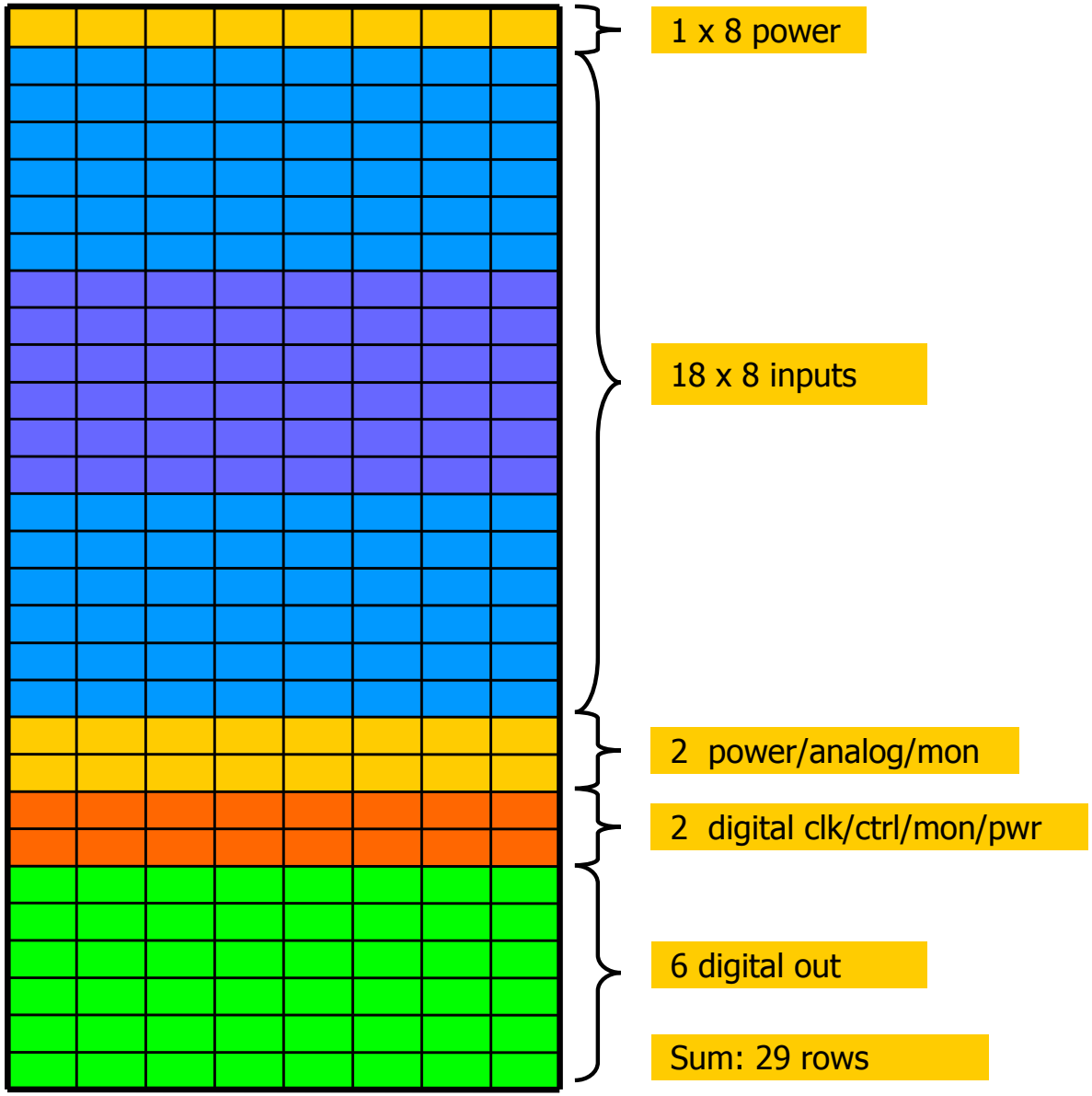
Pixel Layout



Chip Layout



Final Chip View

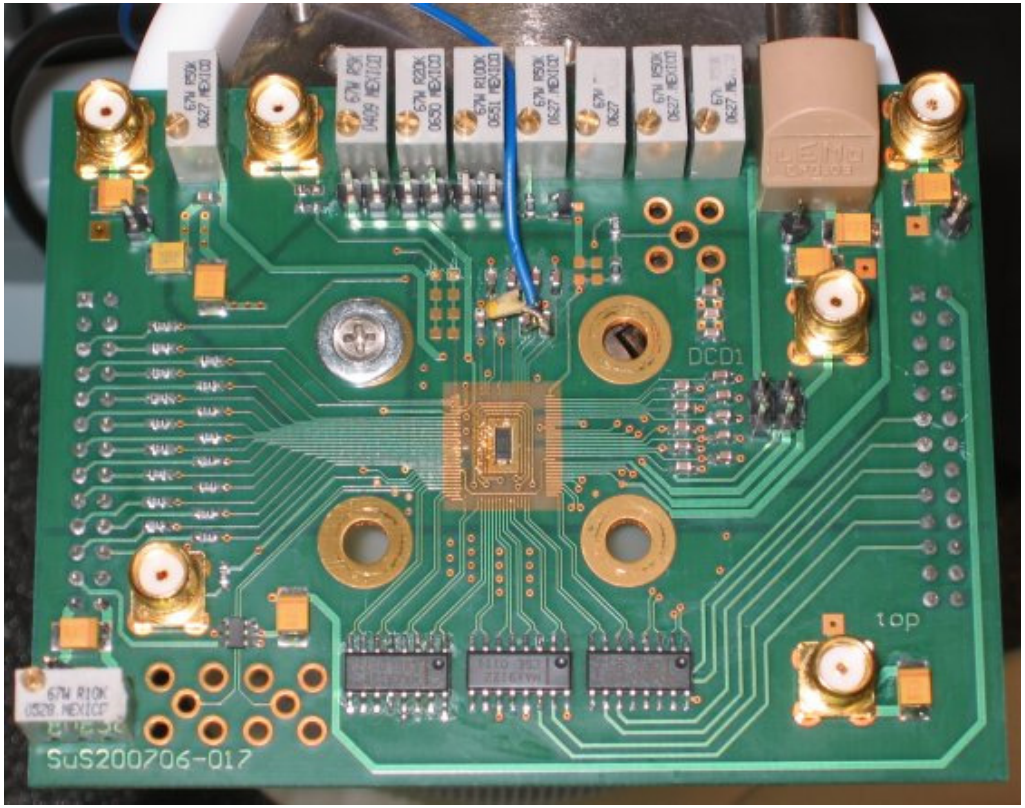


DCD1 features

- UMC 0.18µm 1.8V technology
- regulated cascode
- offset substraction
- one 8bit ADC per channel
  - 144 ADCs on final chip
  - massive parallel high speed output @600MHz LVDS
- consequent current mode signal processing
- no zero suppression
  - occupancy in ILC so high, that benefit of 0-supp too small
- Bump bonding with pixel logic & ADC placed around pad
- Radiation Hard Design
- NMOS in triple Well, guard ring around analog part

Test Status

- Tests just startet
- basic functionality seems ok
- problems with voltage drops on preliminary wire bond connections



Thank You!