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Steering and Readout Chips for DEPFET Sensor Matrices

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The ASICs required to operate DEPFET matrices - a fast analog switch and a drain current readout chip - are presented.

Summary

DEPFET Pixel sensor matrices consist of regular arrangements of DEPFETs. They are read out sequentially by enabling individual gate rows so that the currents in the drain columns reflect the pixel charge. Specialized chips are required to apply voltage steps of up to 10V to gate- and clear rows. The radiation tolerant switcher3 chip has been developed for that purpose. It contains 128 channels, a flexible sequencer and relies on bump bonding. A prototype for the latest drain readout architecture is also presented.

Authors: Dr PERIC, Ivan (Universität Mannheim); Prof. FISCHER, Peter (Universität Mannheim)

Co-authors: Mr KREIDL, Christian (Universität Mannheim); Mr GIESEN, Florian (Universität Mannheim)

Presenter: Mr KREIDL, Christian (Universität Mannheim)

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