SPIROC (SiPM Integrated Read-Out Chip) : Dedicated very front-end electronics for an ILC prototype hadronic calorimeter with SiPM read-out.

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LAL (Laboratoire de l'accélérateur linéaire) is a physics laboratory in Orsay (France), 20 km away from Paris. 350 people including around 100 physicists work on many experiments in cosmology, high energy particle physics and accelerator. Several technology groups such as the mechanics or the electronics group work on applications to achieve physicists expectations.

The LAL electronics group (50 people) is divided in 3 units : digital design unit, analog design unit, and automated equipment design unit. Teams are involved in many large physics experiments such as Atlas, Planck, Auger and FLC. The group can work on project from the manufacturing standard to the production and ensure maintenance.

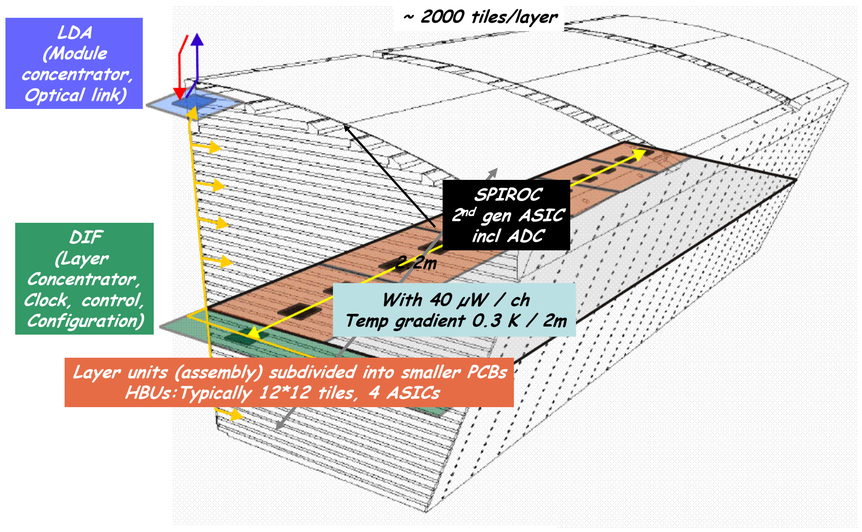
The analog team has acquired a sharp knowledge in full-custom analog ASIC design. Its specialization is focused on low-noise high-speed front-end chip and on high-precision calibration devices. Its know-how is evolving to system-on-chip designs that embed front-end electronic, auto-trigger system, calibration devices and digital converters.

IN2P3 (Nuclear and particle physics French institute) has recently asked for a rationalization of engineering resources in microelectronics and is building competence poles. Omega is the pilot structure. 10 engineers are currently in the Omega team, ensuring the R&D of several complex chips per year to serve particle physics.

Orsay Micro-Electronics Group Associated

Introduction

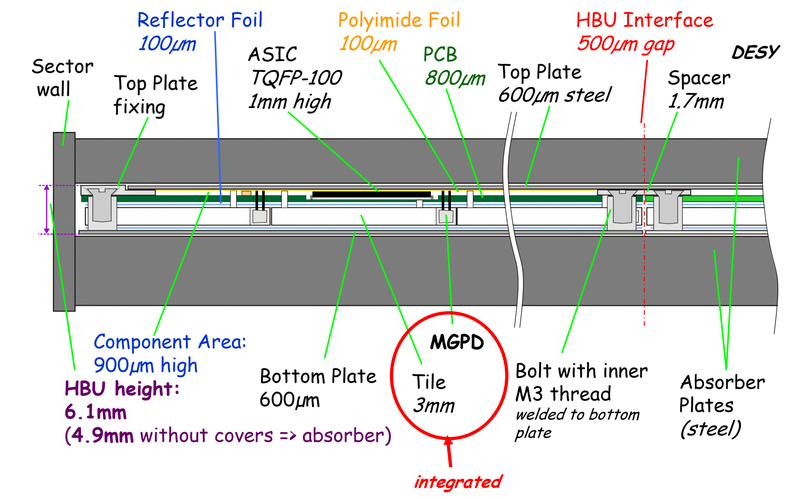
The SPIROC chip is a dedicated very front-end electronics for an ILC prototype hadronic calorimeter with SiPM readout. This ASIC is due to equip a 10,000-channel demonstrator in 2009.
SPIROC is an evolution of FLC_SiPM used for the ILC AHCAL physics prototype.
SPIROC was submitted in June 2007 and will be tested in September 2007. It embeds cutting edge features that fulfil ILC final detector requirements. It has been realized in 0.35m SiGe technology. It has been developed to match the requirements of large dynamic range, low noise, low consumption, high precision and large number of readout channels needed.
SPIROC is an auto-triggered, bi-gain, 36-channel ASIC which allows to measure on each channel the charge from one photoelectron to 2000 and the time with a 100ps accurate TDC. An analog memory array with a depth of 16 for each channel is used to store the time information and the charge measurement. A 12-bit Wilkinson ADC has been embedded to digitize the analog memory content (time and charge on 2 gains). The data are then stored in a 4kbytes RAM. A very complex digital part has been integrated to manage all theses features and to transfer the data to the DAQ.



ILC AHCAL calorimeter

SPIROC main features :

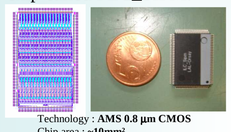
- **36-channel readout chip**
- **Internal input 8-bit DAC (0-5V) for SiPM gain adjustment**
- **Energy measurement :**
  - 2 gains / 12 bit ADC 1 pe → 2000 pe
  - Variable shaping time from 50ns to 100ns
  - pe/noise ratio : 11
- **Time measurement :**
  - TDC (12 bits) step~100 ps
  - pe/noise ratio on trigger channel : 24
  - Fast shaper : ~15ns
  - Auto-Trigger on ½ pe
- **Analog memory for time and charge measurement : depth 16**
- **Low consumption : ~25µW per channel (in power pulsing mode)**
- **Calibration injection capacitance**
- **Embedded bandgap for voltage references and DAC for trigger threshold**
- **Bunch Crossing ID, Hit channels and Gain saved for each column of SCA**
- **Digital part**
  - 2 clocks domains : 40 MHz and 5 MHz for digital part
  - Serial analogue output
  - External "force trigger"
  - 12-bit Bunch Crossing ID
  - SRAM with data formatting 2 x 2kbytes = 4kbytes
  - Output & control with daisy-chain
- **Probe bus for debug :** 939 probe points
- **Very versatile:** 703 slow control parameters



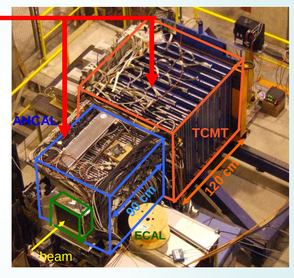
AHCAL integrated layer design

First generation SiPM readout chip : FLC_SiPM

The CALICE collaboration has designed an analogue HCAL prototype using Scintillating fibers read out by SiPM detectors. That 8000-channel physics prototype is currently in test beam at CERN. The read-out of that detector is ensured by an analogue front-end chip called FLC_SIPM.

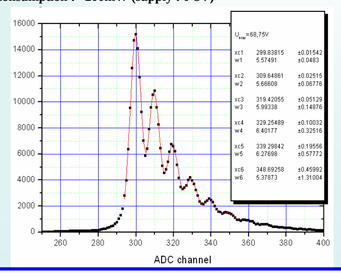


Technology : **AMS 0.8 µm CMOS**
Chip area : **~10mm²**
Package : **QFP-100**



FLC_SiPM chip main characteristics
18-channel 8-bit DAC (0-5V)
18-channel front-end readout :
- Variable gain charge preamplifier (0.67 to 10 V/pC)
- Variable tine constant CRRC2 shaper (12 to 180 ns)

•Track and hold → 1 multiplexed output
Power consumption : ~200mW (supply : 0-5V)

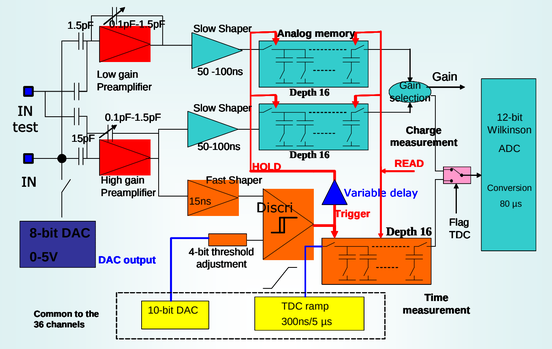


Single photoelectron spectrum

SPIROC Full Chip layout

Technology : AMS SiGe 0.35µm technology
Surface : 32mm² (4.2mm × 7.2mm)
Power supply : 5V/3.5V
Consumption : 25µW per channel (in power pulsing mode)
Package : CQFP240

One channel design



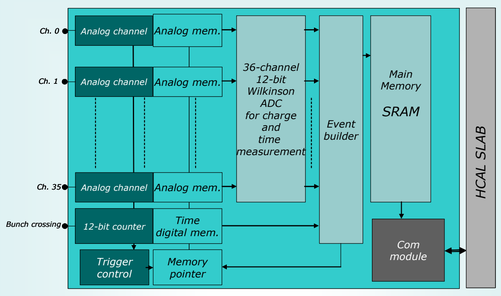
Each channel includes an input DAC which allows to adjust the SiPM high voltage on 5V and consequently the detector gain.
Two variable preamplifiers allow to obtain the requested dynamic range (from 1 to 2000 photoelectrons) with a level of noise of 0.1pe.

Then, these charge preamplifiers are followed by two variable slow shapers and two 16-deep Switched Capacitor Array (SCA) in which the analogue voltage will be stored.

A voltage 300ns ramp gives the analogue time measurement. The time is stored in a 16-deep SCA when a trigger occurs. It is digitized on 12 bits with a resolution less than 1ns.

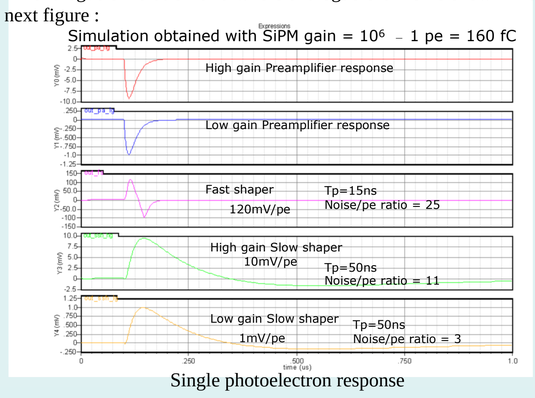
In parallel, trigger outputs are obtained via fast channels made of a fast shaper followed by a discriminator. The discriminator output feeds the digital part which manages the SCA.

SPIROC Block scheme



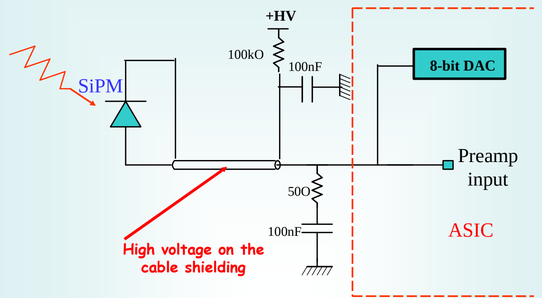
Analogue simulations

An analogue simulation of a whole analogue channel is shown in the next figure :



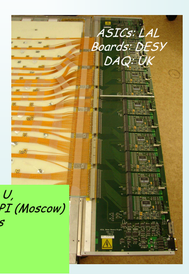
Single photoelectron response

SiPM connection scheme



A 5V rail-to-rail 8-bit Digital-to-Analog Converter, integrated on each of the 36 input lines of the ASIC, allows individual adjustment of the SiPM bias voltage for each channel.

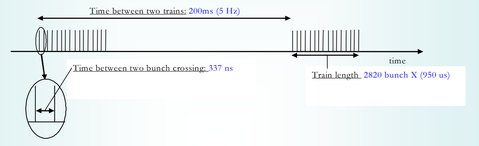
- 1 cubic metre
- 38 layers, 2cm steel plates
- 8000 tiles with SiPMs
- Electronics based on CALICE ECAL design, common back-end and DAQ

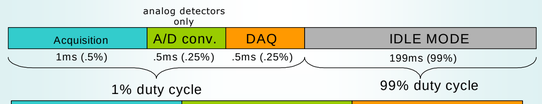


DESY, Hamburg U, ITEP, MEPHI, LPI (Moscow) Northern Illinois LAL, Orsay Prague UK groups

SPIROC running mode

The system on chip has been designed to match the ILC beam structure. The valid data are stored in each front-end chip during the beam train.
Then, the data are converted into digital data before being stored in the chip SRAM.
Finally, the data are sent to DAQ during the inter-train. When all these operations are done, the chip goes to idle mode to save power.



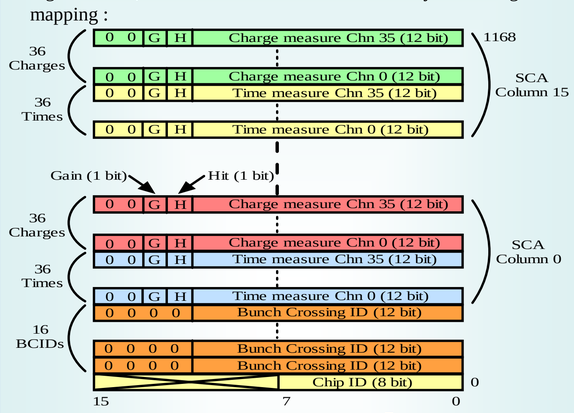


Acquisition	A/D conversion	DAQ
When an event occurs : • Charge is stored in analogue memory • Time is stored in digital (coarse) and analogue (fine) memory • Trigger is automatically rearmed at next coarse time flag (bunch crossing ID) Depth of memory is 16	The data (charge and time) stored in the analogue memory are sequentially converted into digital data and stored in a SRAM.	The events stored in the RAM are readout through a serial link when the chip gets the token allowing the data transmission. When the transmission is done, the token is transferred to the next chip. 256 chips can be read out through one serial link

The management of all the different steps of normal working (acquisition, A/D measure and read-out) need a very complex digital part which was integrated in the ASIC. (See poster from Frédéric Dulucq).

RAM Mapping

During the conversion mode, the analogue data are converted into digital. Then, the data are stored in SRAM by following the mapping :



SPIROC readout

The readout is based on a daisy chain mechanism initiated by the DAQ. One data line activated sequentially is used to readout all the ASIC on the SLAB