Low Power Front End for the Optical Module of a Neutrino Underwater Telescope

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Abstract

A proposal for a new system to capture signals in the Optical Module (OM) of an underwater neutrino telescope is described. It concentrates on the problem of power consumption and the time precision. In particular, a solution for the interface between the photomultiplier (PMT) and the front-end electronics is presented.

I. Introduction

An Underwater Neutrino Telescope uses large area PMTs inside OMs to detect the Cherenkov light from the muons generated by neutrinos in the seawater. The PMTs are put in a 17" glass sphere capable to stand at more than 350 Atm external pressures. The signals at the output of PMTs must be suitably coded and sent on-shore. The OM contains the PMT and its power supply board, the front-end electronics, the data pack and transfer electronics, the slow control interface and a set of environmental sensors.

The work described in this paper is aimed at the development of the low-power front-end for the Optical Modules (OM) of the NEMO submarine neutrino detector [2,3,4,7]. A mini-tower equipped with 16 OMs (NEMO-Phase1 MiniTower) has been successfully deployed in December 2006 in front of the Catania harbour as a first prototype. It uses the front-end electronics described in [1]. The technological solutions adopted for the NEMO MiniTower provide results well in agreement with expectations. In the meantime, we have proceeded in our development of a solution which can fulfil all requirements of a km3-scale detector, in particular for what concerns power consumption, PMTs aging and signal dynamics.

Our work is based on the design of an Application Specific Integrated Circuit (ASIC) for the development of the Trigger, the PMT signal classification and fast sampling of the PMT signal, which is performed according to the signal classification. Moreover, commercial ADCs and a Field Programmable Gate Array (FPGA), provide digital encoding, data packing and then data transfer towards the shore station for acquisition.

A board containing the PMT interface electronics, the ASIC, the ADC and the FPGA constitutes the OM front-end. By means of the FPGA, this board receives the slow control and transmits the measurements of environmental parameters such as temperature, humidity etc., together with the data.

The final version of the chip, named LIRA05[5], has been tested and the single blocks, constituting its architecture, that is, the analog memory, the trigger and single photon classifier and the clock frequency multiplier, have been characterised. The board to test the whole front-end together with the PMT is being prepared.

II. The OM front-end

The design of the front-end board and of the chip, in particular, are based on parameters and specifications that in some cases are not yet definitive, for the performance of the whole detector.

We have used the most recent data coming from simulations of high energy neutrino events produced in a submarine detector in order to define the specifications of the front-end electronics that optimise the detector performance. These simulations describe the signals collected by each PMT in the apparatus in response to particle events, taking into account the optical background due to the decay of ^{40}K, the optical properties of the sea water, the orientation and position of the PMTs.

As a result of this study, a new architecture has been defined for the system that performs the sampling.

This new integrated device, called Smart Auto-triggering Sampler (SAS), will consist of functional blocks very similar to those already designed and successfully tested. This choice will allow us to introduce the performance of each block into the simulations of the whole front-end making their results more significant and realistic [5]. The block diagram of the front-end under design is shown in Figure 1.

One fundamental part is the interface PMT-board. This interface has to allow the de-coupling, amplification, filtering and delay of the signals, with low power dissipation and with the maximum design reliability and compactness.

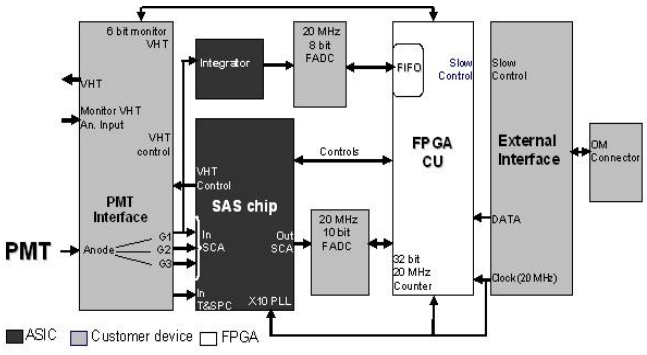

Figure 1: The block diagram of the OM front-end architecture.

The present work concentrates on this part of the front-end, the PMT interface.

III. SIGNAL SIMULATIONS

From the analysis of simulated high energy neutrino events in the NEMO detector we derived several important points:

- Three main pieces of information must be extracted by the front-end:
  - The signal arrival time, with a resolution better than 1 ns;
  - The charge of the signal from the PMT with a good accuracy and a very high discrimination of single- vs. multiple- photoelectron signals;
  - The shape of the signal.
- The front-end must have the following characteristics:
  - Wide input dynamics, since the signals to be sampled have a very wide dynamic range according to the signal time duration, that is up to 1000 photoelectrons (pe) in 500 ns and up to 10000 pe in 10μs;
  - Negligible dead time. The presence of the single pe background due to spontaneous decay of the ^{40}K present in the seawater, with an average rate of 50 kHz imposes a suitable memory channel depth and a precise relationship between the sampling and conversion frequencies.

IV. THE PMT INTERFACE

The considerations and simulations are related to the 10" PMT selected for the NEMO experiment. The selected gain is $5 \cdot 10^7$.

The PMT base is active and provides single pe signals on an anodic load of 50Ω of about 50 mV amplitude with a rise time of about 2.6 ns. The PMT signal amplitude grows linearly with the intensity of incident light up to about 100 pe. Due to the signal frequency spectrum and the resolution required for the measurement of the arrival time we chose to sample the signal at 200 MHz with analog memories. This value is a good compromise between dissipated power and the number of samples taken for every signal.

The conversion of each sample is made by a commercial 10 bit 20 MHz ADC. A consideration must be made on the signal frequency band. It presents components above 100 MHz which can produce aliasing effects. Therefore the PMT signal must be filtered. Furthermore in order to increase the PMT signal amplitude it is possible to use a higher anodic load, for example 800Ω. This allows the gain of the PMT to be reduced, increasing the average life time of the PMT. To cover the wide signal dynamic range in the most linear possible way, a PMT interface is foreseen that provides an input impedance of about 800 Ω, signal filtering. In such a way the components above 100 MHz are reduced to -60 dB at least. Three channels with different gain produces three signals with different amplitudes but identical shapes. The gains have been derived from the simulations in order to use three linear range of 1 volt that covers signals of up to 512 pe. For instance, the first channel is direct, the second is reduced by a factor 8 and the third by a factor 64. Each channel has a suitable buffer to drive the delay lines and the load of the analog memories. The delay is essential and is of the order of 30 ns: from the instant in which the signal crosses a suitable threshold a time interval is required for its classification and the beginning of the appropriate sampling of the signals according to their classification. Integrated delay lines will be used, greatly reducing bulk and having a greater mechanical robustness compared to the classical delay lines made with coaxial cables.

Other specifications are the 3.3 V power supply and the low-power dissipation. As a result of the former each channel has to be protected from PMT signals with amplitude higher than 3.3 V. The second channel, having a gain of 1/8 can, for example, sustain signals of up to 24 V. For this reason a switch has been introduced into every amplification branch with a fast JFET transistor that excludes the amplifiers from the signal setting it to high impedance as soon as the voltage at its input goes over an adjustable threshold. This threshold is related to the threshold voltage of the JFET and to its externally applied gate voltage. The selected JFET introduces very low parasite capacitances making it possible to limit the input signal bandwidth to about 40 MHz at -3 dB, allowing the use of a low power operational amplifier with 3.3 V single supply whose power consumption is about 5 mW.

An additional channel will provide information about the signal charge in the case the three gain channels are saturated.

This channel, called integrator, further extends the signal dynamic range. It basically consists of a low pass filter with a bandwidth of about 4 MHz at -3 dB.

Its output will be continuously converted by a low power 20 MHz 8 bit ADC and then stored in a Fast In Fast Out register (FIFO). Every time the signal is classified by the Trigger and Single Photon Classifier (TSPC) as a very large amplitude signal, the data in the FIFO will be forwarded to data acquisition together with the time stamp. In Figure 2 the circuit schematic of the interface board is shown.

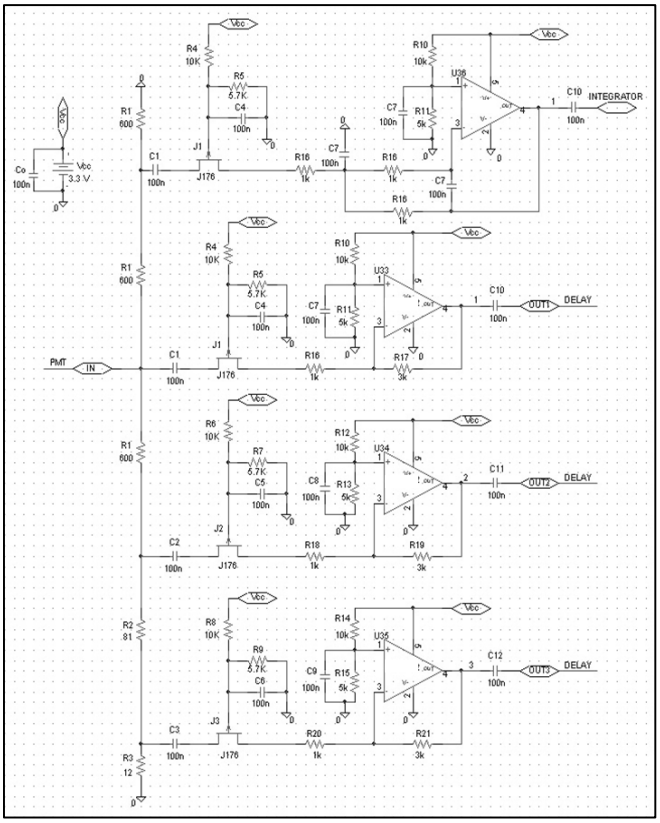

Figure 2: Schematic view of the PMT interface

The PMT interface has been designed and tested with the NEMO selected PMT in a dark box using a laser to produce light. The typical signals of the three channels in the presence of a signal of single pe, with a PMT gain of $5 \cdot 10^7$, are shown in Figure 3.

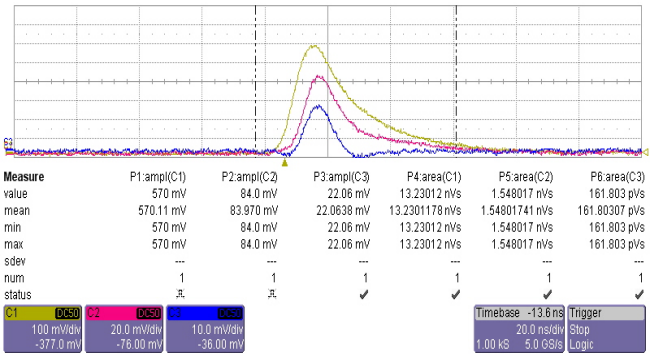

Figure 3: The output signals of the PMT interface board corresponding to a single p.e. input signal.

In Figure 4 the three channels in presence of a signal of PMT of 27 p.e. are shown. There it is shown how the first channel is saturated and the second presents an exact replica of the PMT signal attenuated of a factor of 8 while in Figure 5 the output of the board corresponding to 81 p.e. are shown. In Figure 6 all the three channel are saturated at about 400pe.

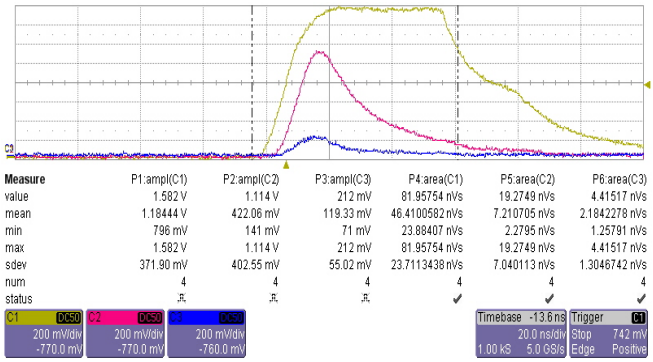

Figure 4: The output signals of the PMT interface board corresponding to the 27 p.e. input signal.

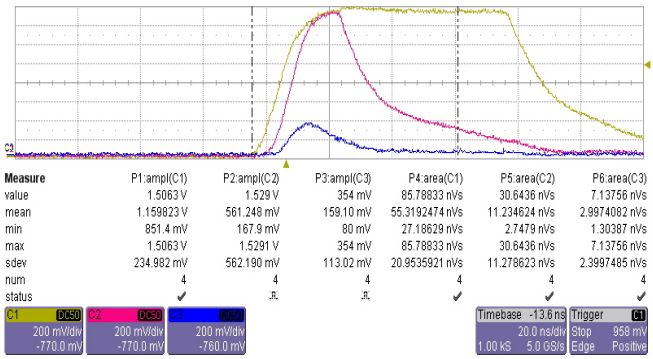

Figure 5: The output signals of the PMT interface board corresponding to the 81 p.e input signal.

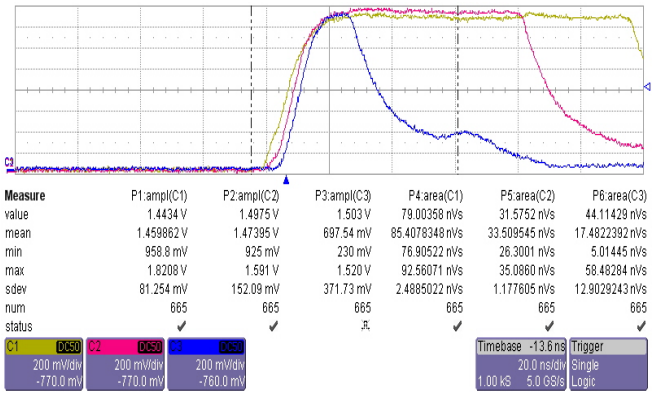

Figure 6: The saturated output signals of the PMT interface board corresponding to the 400 p.e. input signal.

Finally in Figure 7 the output signal of the integrator corresponding to 64 p.e. is shown.

The single photoelectron signal amplitude is about 570 mV and we want to have a voltage dynamic range of 1 V corresponding to 8 p.e.. So the gain of the PMT must be lowered by a factor of about 5 which means $1 \cdot 10^7$, with the effect of reducing the PMT ageing. [8,9]

The rise time of the signals is of about 9 ns as a result of the filtering of the signal. This will avoid aliasing effect in the 200 MHz sampling performed by the analog memories.

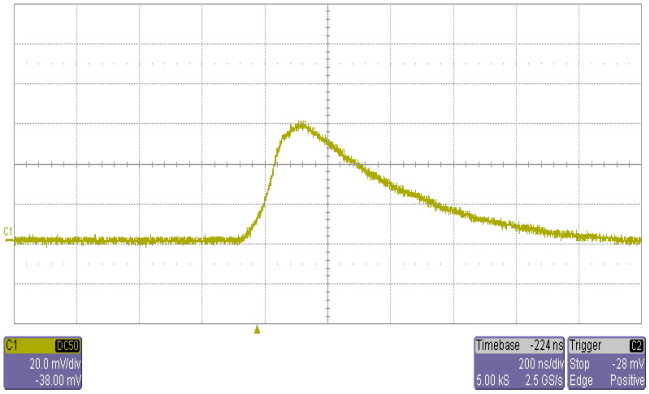

Figure 7: The output signal of the integrator channel corresponding to about 64 p.e. input signal.

The values of gain of the three output channels are easily settable by adjusting the resistor ladder at the input. The power consumption of the PMT interface board is of 8 mA at 3.3 V. The board could also work very well with power supply as low as 2.7 V.

The PMT interface board will, in the meantime, be tested together with the previous version of the front-end.

The DAQ (Data Acquisition)board designed by Bologna University collaborators [6], containing the last version of the LIRA chip, the FPGA, with the function of Control Unit e Data Packing and Transfer Unit, is shown in Figure 8.

The LIRA chip contains two analog memories, 3 channels 256 cells, working in buffer mode, the PLL, and the T&SPC.

This board is under test and is thought to be compliant with the actual Optical Module interconnections and functions.

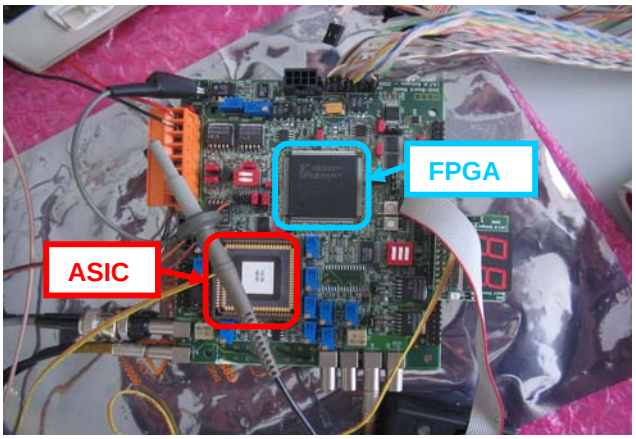

Figure 8: Data acquisition board with the ASIC chip and the FPGA

V. Conclusion

A proposal for a system to capture signals in the Optical Module of an underwater neutrino telescope has been described, with focus on power consumption considerations. All considerations regarding the signals and their acquisition are made starting from the most general hypothesis possible, so that they will be valid for any underwater Cherenkov neutrino telescope.

The development of the PMT interface board to meet the specifications of power dissipation, filtering properties, anodic load and required gain establishes the basis for the definitive design of the SAS chip. As soon as the chip will be available, the whole front-end will be tested together with the PMT.

VI. References

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