Contribution ID: **0** Type: **Oral**

Low Power Front End for the Optical Module of a Neutrino Underwater Telescope

Friday, 7 September 2007 11:25 (25 minutes)

A proposal for a new system to capture signals in the Optical Module (OM) of an Underwater Neutrino Telescope is described. It concentrates on the problem of power consumption in relation to precision. In particular, a solution for the interface between the photomultiplier (PMT) and the front-end electronics is presented.
We have used the most recent data coming from simulations of high energy neutrino events produced in a submarine detector in order to define the specifications of the front-end electronics that optimise the detector performance. As a result a new architecture has been defined for the chip that performs the sampling.

Summary

An Underwater Neutrino Telescope uses large area PMTs inside OMs to detect the Cherenkov light from the muons generated by neutrinos in the seawater. The PMTs are put in a 17"glass sphere capable to stand at more than 350 Atm external pressures. The signals at the output of PMTs must be suitably coded and sent on-shore. The OM contains the PMT and its power supply board, the front-end electronics, the data pack and transfer electronics, the slow control interface and a set of environmental sensors.
The work described in this paper is aimed at the development of the low-power front-end for the Optical Modules (OM) of the NEMO submarine neutrino detector [2,3,4,7]. A mini-tower equipped with 16 OMs (NEMOPhase1 MiniTower) has been successfully deployed in December 2006 in front of the Catania harbour as a first prototype. It uses the front-end electronics described in [1]. The technological solutions adopted for the NEMO MiniTower provide results well in agreement with expectations. In the meantime, we have proceeded in our development of a solution which can fulfil all requirements of a km3-scale detector, in particular for what concerns power consumption, PMTs aging and signal dynamics.
Our work is based on the design of an Application Specific Integrated Circuit (ASIC) for the development of the Trigger, the PMT signal classification and fast sampling of the PMT signal, which is performed according to the signal classification. Moreover, commercial ADCs and a Field Programmable Gate Array (FPGA), provide digital encoding, data packing and then data transfer towards the shore station for acquisition.
A board containing the PMT interface electronics, the ASIC, the ADC and the FPGA constitutes the OM front-end. By means of the FPGA, this board receives the slow control and transmits the measurements of environmental parameters

such as temperature, humidity etc., together with the data. The final version of the chip, named LIRA05, has been tested and the single blocks, constituting its architecture, that is, the analog memory, the trigger and single photon classifier and the clock frequency multiplier, have been characterised. The board to test the whole front-end together with the PMT is being prepared.
The design of the front-end board and of the chip, in particular, are based on parameters and specifications that in some cases are not yet definitive, for the performance of the whole detector.
We have used the most recent data coming from simulations of high energy neutrino events produced in a submarine detector in order to define the specifications of the front-end electronics that optimise the detector performance. These simulations describe the signals collected by each PMT in the apparatus in response to particle events, taking into account the optical background due to 40K, the optical properties of the sea water, the orientation and position of the PMTs.
As a result a new architecture has been defined for the chip that performs the sampling.
This new device, called Smart Auto-triggering Sampler (SAS), will consist of functional blocks very similar to those already designed and successfully tested.

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Session Classification: Parallel session B7 - Systems, Installation and Commissioning 7