Development of an ASIC for reading out CCDS at the vertex detector of the International Linear Collider

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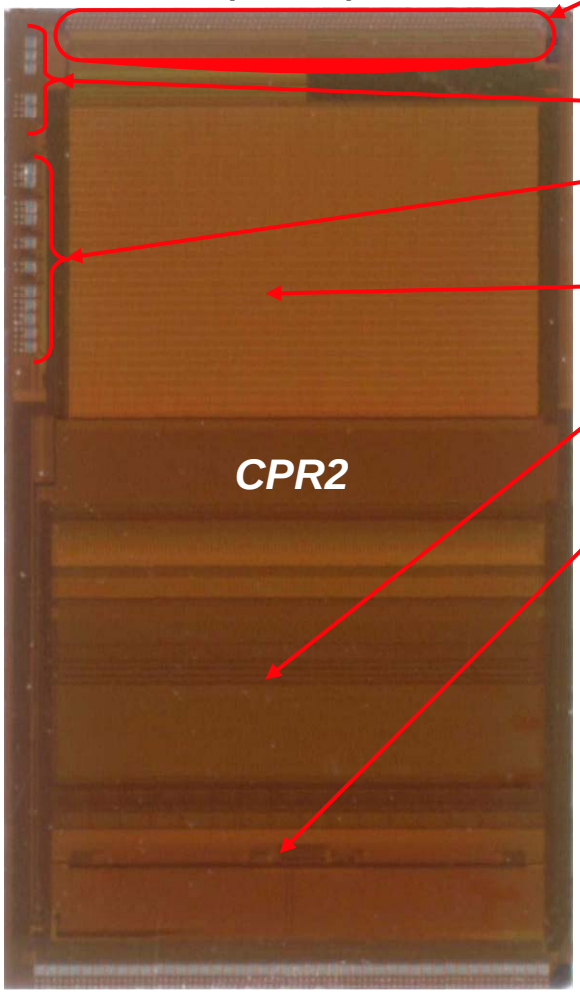
Detector overview

- ILC will collide e+ e- beams at energies up to 500GeV.
- Interactions recorded by 2 detectors, each with a vertex detector.
- Vertex detector resolution < 5 microns, with low power and minimum material.
- Thus CCDs have been selected.
- Need to keep occupancy below 1% means that CCD pixel columns must be read out in parallel at 50Mhz.
- Low occupancy also makes on-chip data sparsification desirable.

Already fabricated CPR chips



Voltage and charge amplifiers
125 channels each

Analogue test I/O

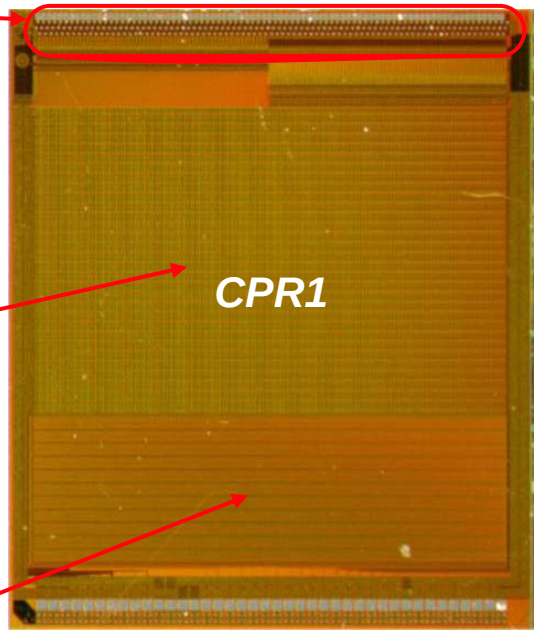
Digital test I/O

5-bit flash ADCs on 20 μm pitch

Cluster finding logic
(2×2 kernel)

Sparse readout circuitry

FIFO



- Designed for readout of Column Parallel CCDs under development for LCFI (Linear Collider Flavour Identification)
- CPR2 Size : 6 mm × 9.5 mm
- 0.25 μm CMOS process (IBM)

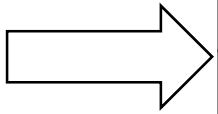
CPR2A Sparsification algorithm

- Chip reads out digitized pixel data only if it exceeds specified threshold.
- Charge from a particle may be shared between several CCD pixels.
- Hence sparsification logic sums data from every 2x2 array of pixels and compares with threshold.
- Chip also reads out data from pixels surrounding the hit pixels which triggered readout.
- Thus all interesting data guaranteed to be read out.
- Because of limited space for the logic the algorithm must be very simple.

Sparsification algorithm

CPR2A readout format – case 1

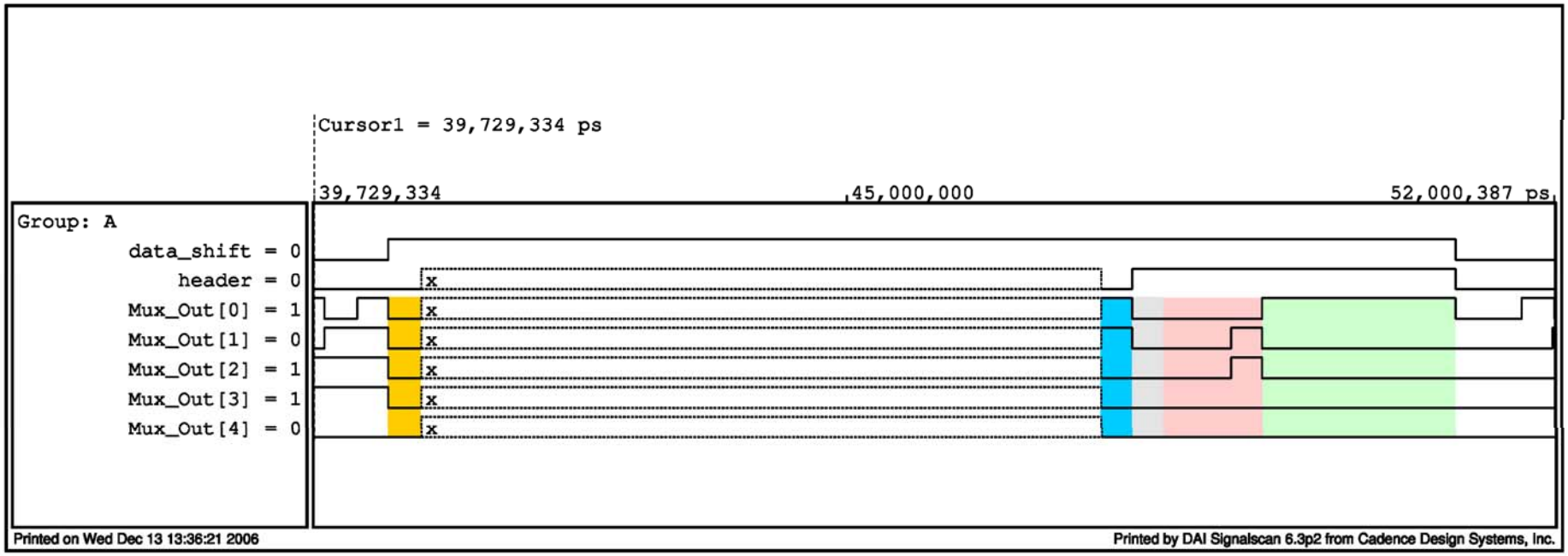
1	1	1	1	1	1	1	1
1	1	1	1	1	1	1	1
1	1	1	1	1	1	1	1
1	1	1	2	2	1	1	1
1	1	1	2	2	1	1	1
1	1	1	1	1	1	1	1
1	1	1	1	1	1	1	1
1	1	1	1	1	1	1	1



1	1	1	1	1	1	1	1
1	1	1	1	1	1	1	1
1	1	1	1	1	1	1	1
1	1	1	2	2	1	1	1
1	1	1	2	2	1	1	1
1	1	1	1	1	1	1	1
1	1	1	1	1	1	1	1
1	1	1	1	1	1	1	1

2 by 2 cluster above threshold : 6 by 4 output data

Output data format



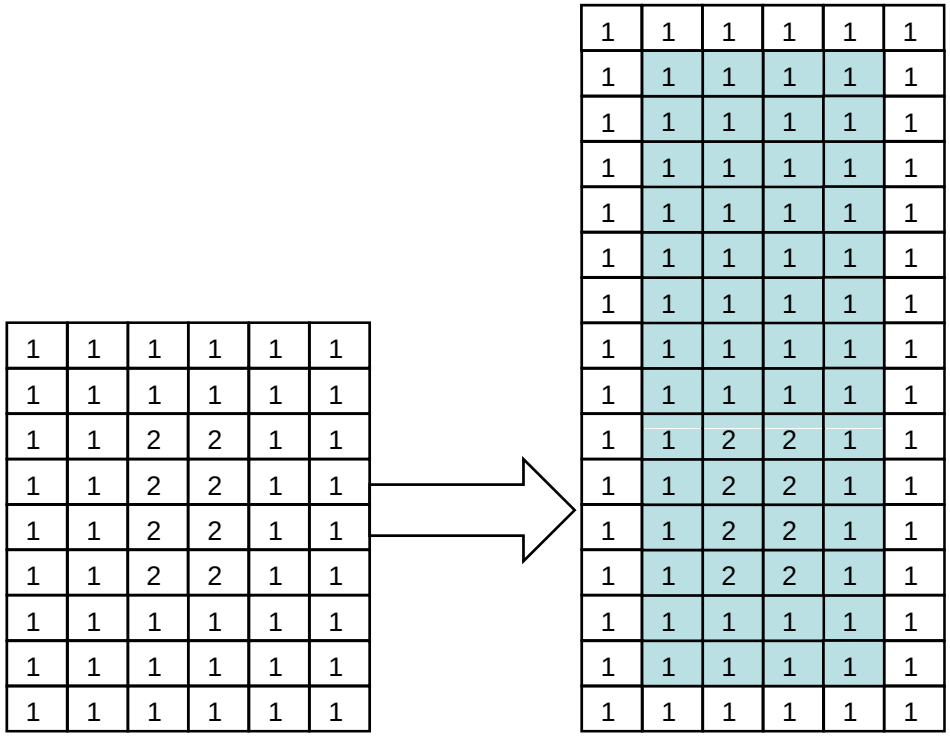
Colour coding:

Address (H) Address(L) Gap (00000) Time-stamp Data

Simplest case: 6 words of 5-bit data

Sparsification algorithm

CPR2A readout format – case 2



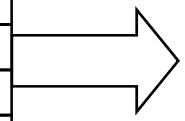
4 by 2 input cluster,

Output data: 6+8 by 4

Sparsification algorithm

CPR2A readout format – case 3

1	1	1	1	1	1
1	1	2	2	1	1
1	1	2	2	1	1
1	1	1	1	1	1
1	1	1	1	1	1
1	1	1	1	1	1
1	1	1	1	1	1
1	1	1	1	1	1
1	1	1	1	1	1
1	1	1	1	1	1
1	1	1	1	1	1
1	1	1	1	1	1
1	1	2	2	1	1
1	1	2	2	1	1
1	1	1	1	1	1



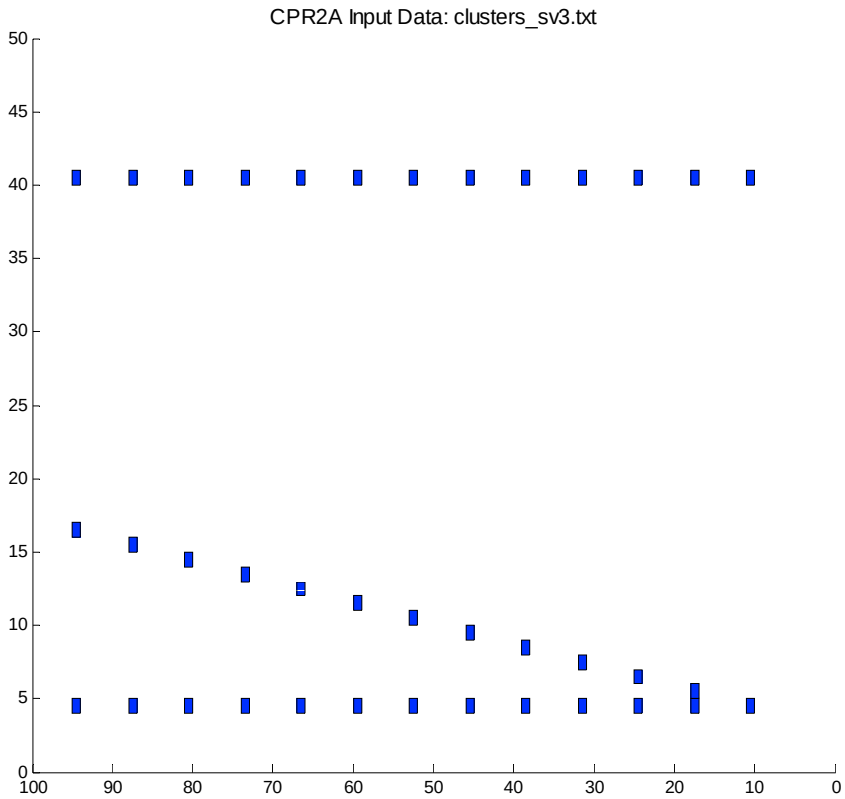
1	1	1	1	1	1
1	1	1	1	1	1
1	1	1	1	1	1
1	1	1	1	1	1
1	1	1	1	1	1
1	1	1	1	1	1
1	1	1	1	1	1
1	1	1	1	1	1
1	1	2	2	1	1
1	1	2	2	1	1
1	1	1	1	1	1
1	1	1	1	1	1
1	1	1	1	1	1
1	1	1	1	1	1
1	1	1	1	1	1
1	1	1	1	1	1
1	1	1	1	1	1
1	1	1	1	1	1
1	1	2	2	1	1
1	1	2	2	1	1
1	1	1	1	1	1
1	1	1	1	1	1
1	1	1	1	1	1

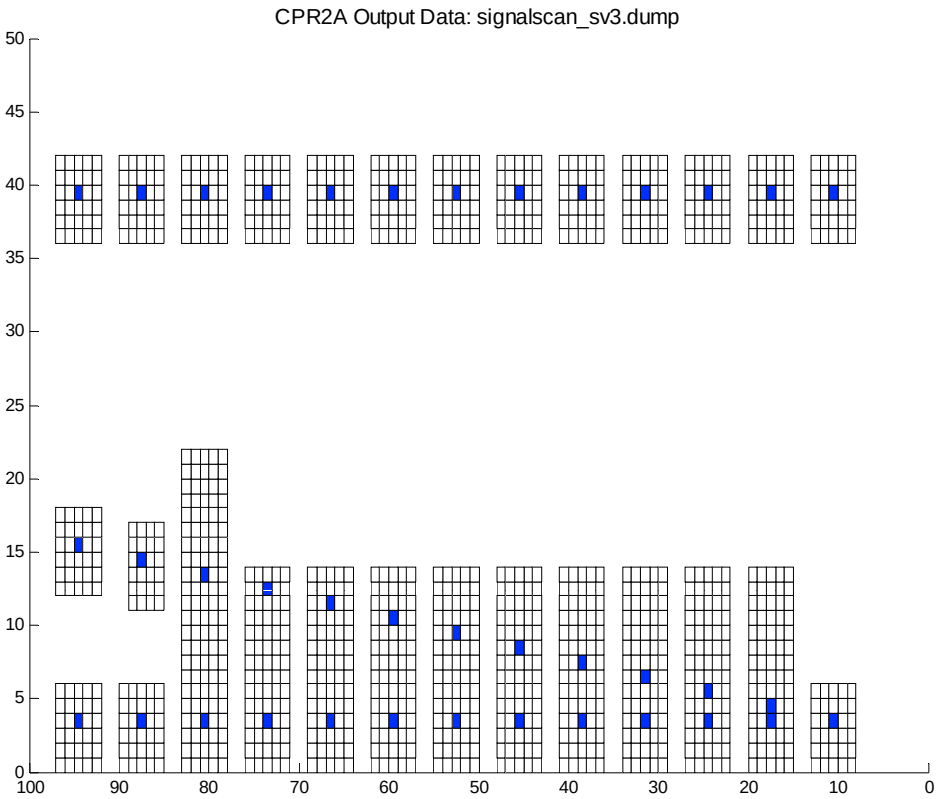
2 input clusters, separated by 9 time steps

Output data: 6+8+8 by 4

Maximum separation that is stored as a single data block

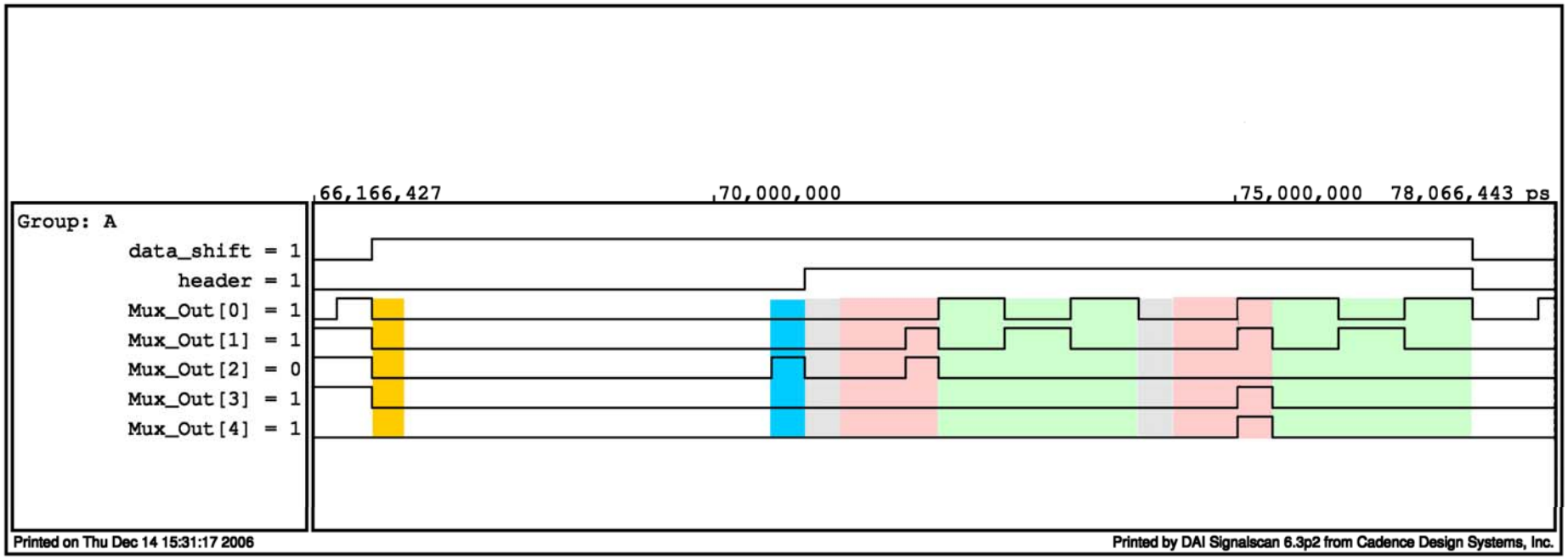
Sparsification algorithm





When vertical cluster separation < 10 pixels data stored in column memory as single data block since only one timestamp needed. When sep>10 data is stored as 2 separate data blocks.

Output data format



Address (H) Address(L) Gap (00000) Time-stamp Data

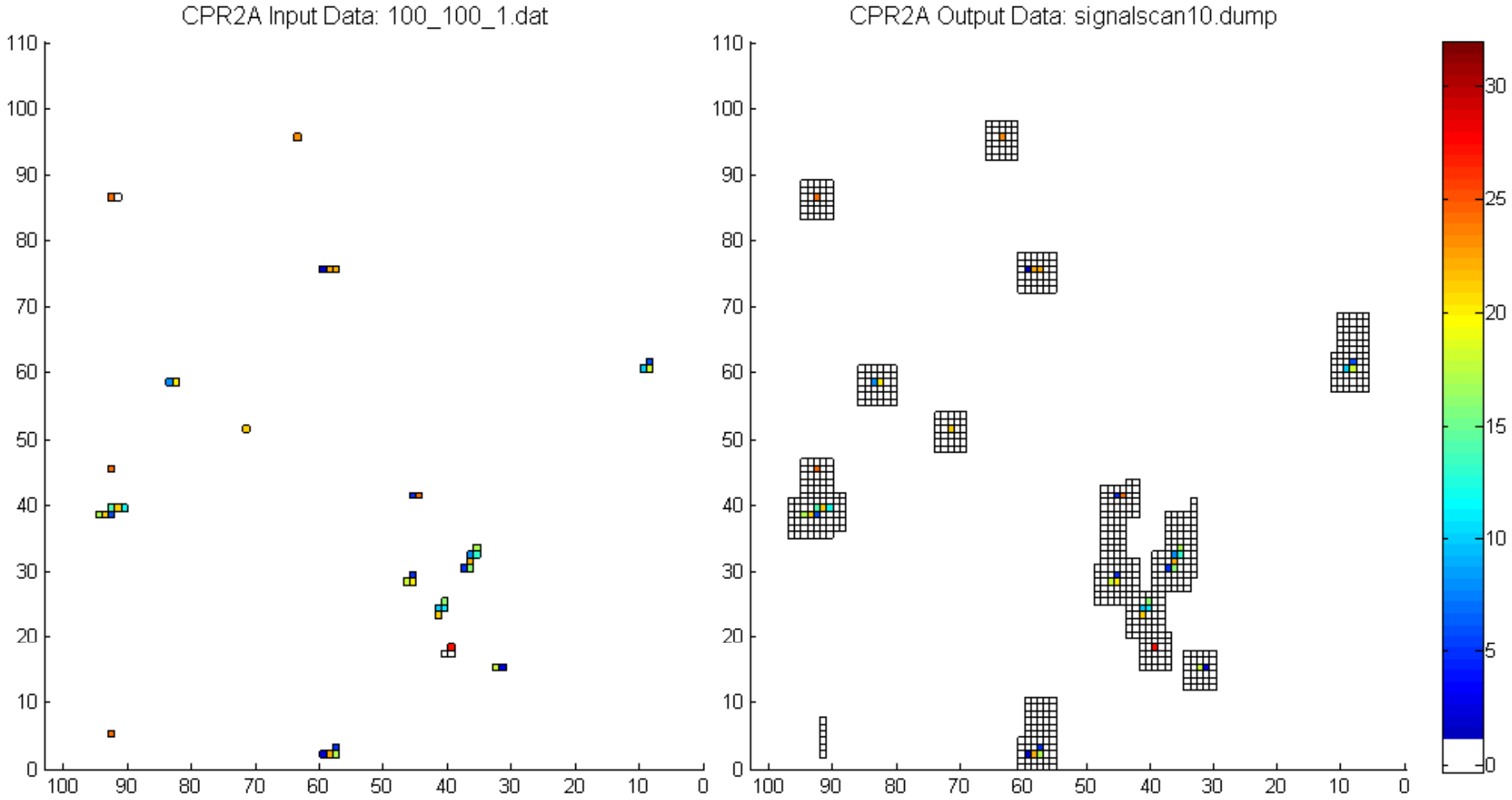
Extended data:

12 words in 2 groups

Time-stamp repeated, no break in header signal

Gap between groups of data, to identify new time-stamp

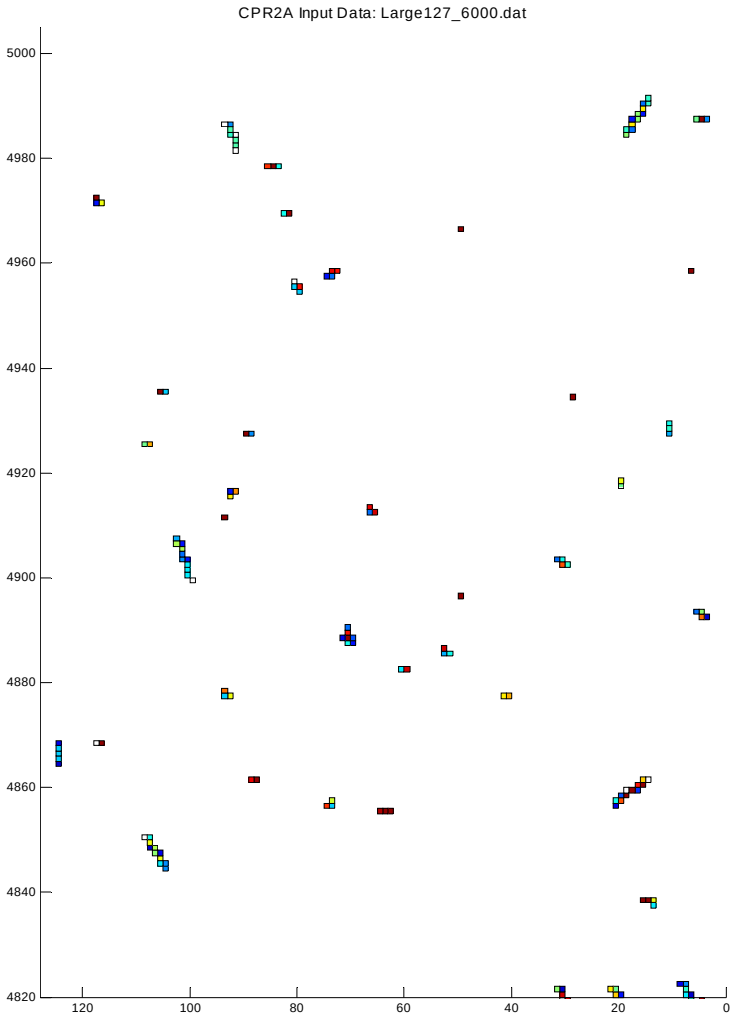
CPR2A Verilog simulations based on physics data (100 channels, 100 time steps)

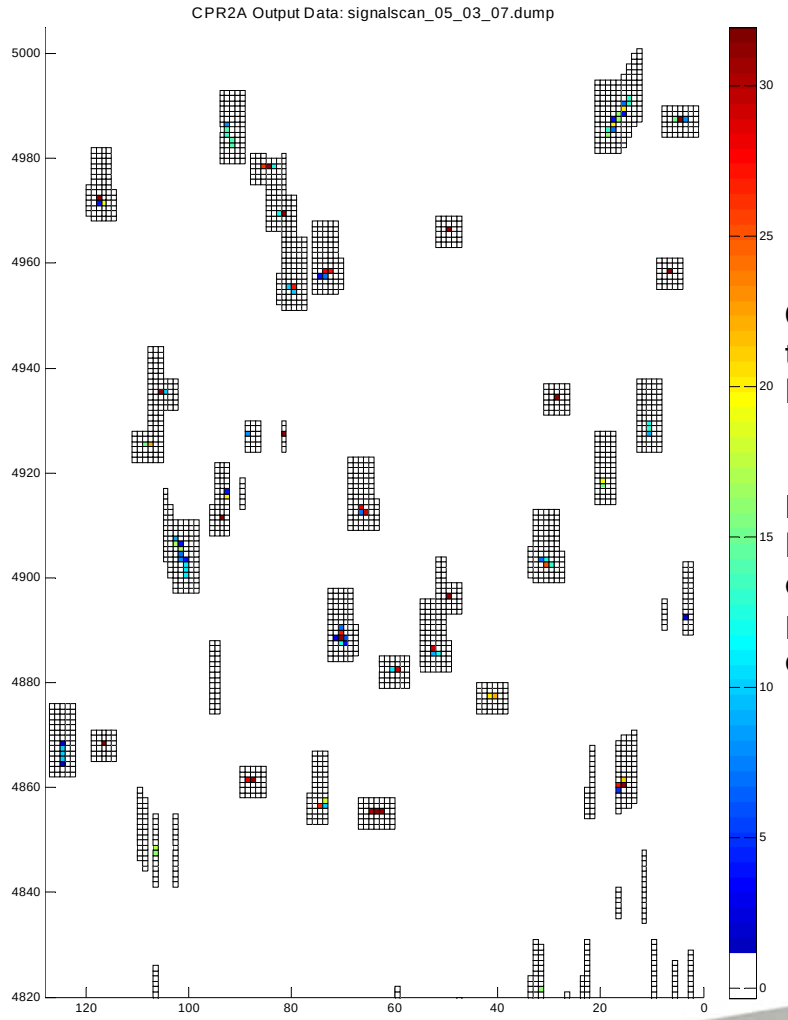


Near-perfect readout over 100 time steps (44 hit pixels, occupancy 0.44%)

One missing data point in the output (channel 92, time stamp 4)

CPR2A Verilog simulations based on physics data (128 channels, 5000 time steps)





Good efficiency for top end of plot : later time stamps

Poor efficiency at bottom end of plot: clusters have lower priority and can be overwritten

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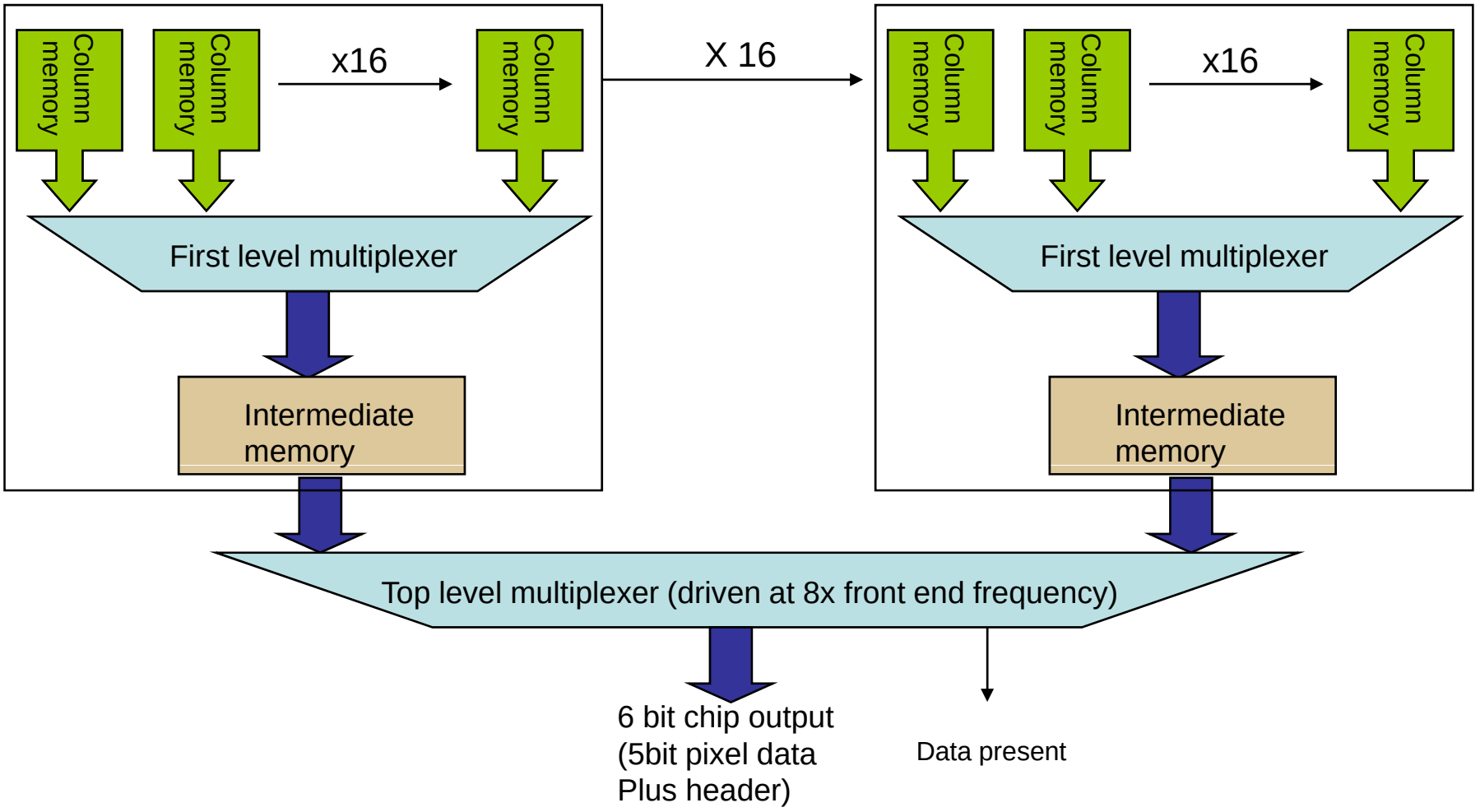
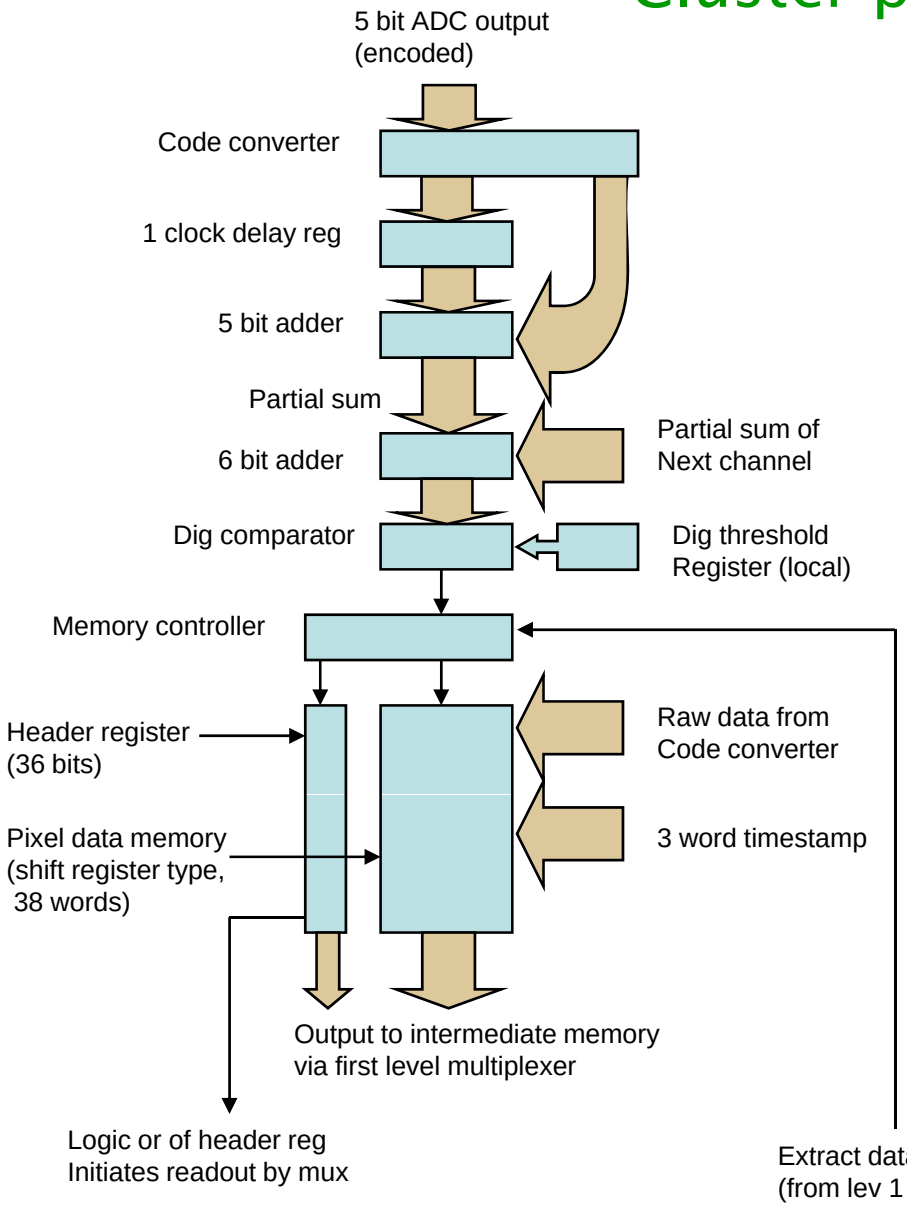
Readout system components

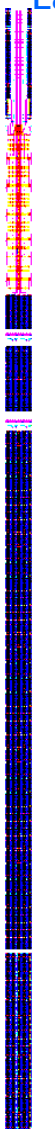


Multiplexers are based on rotating pointers in shift registers. During operation pointer positions become randomised ensuring all parts of the CCD have equal chance of being read out .

Cluster processing



Layout segment 40 microns x1.7mm



State machine

Logic

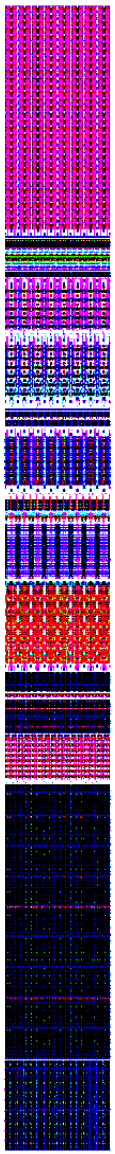
Buffer registers

Time-stamp registers

Memory cells (38 words)

Header memory (38 bits)

Sections of digital layout



Layout of 16 columns:
320 µm x 3.5 mm

Code converter

Logic:

Adders

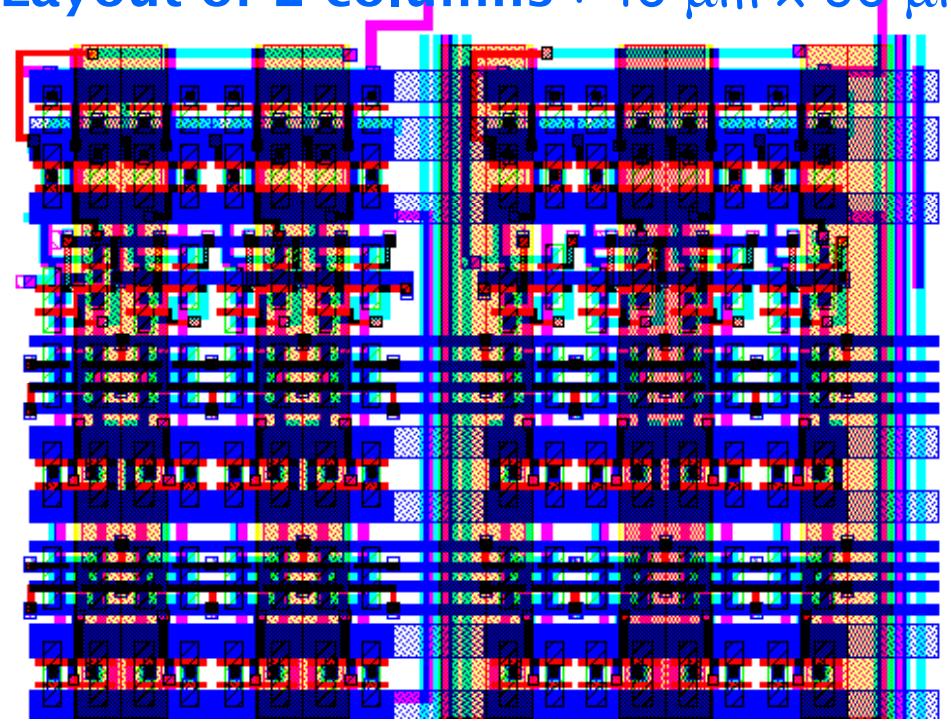
Threshold store

Comparators

State machine (front end)

State machine (back end)

Layout of 2 columns : 40 µm x 30 µm



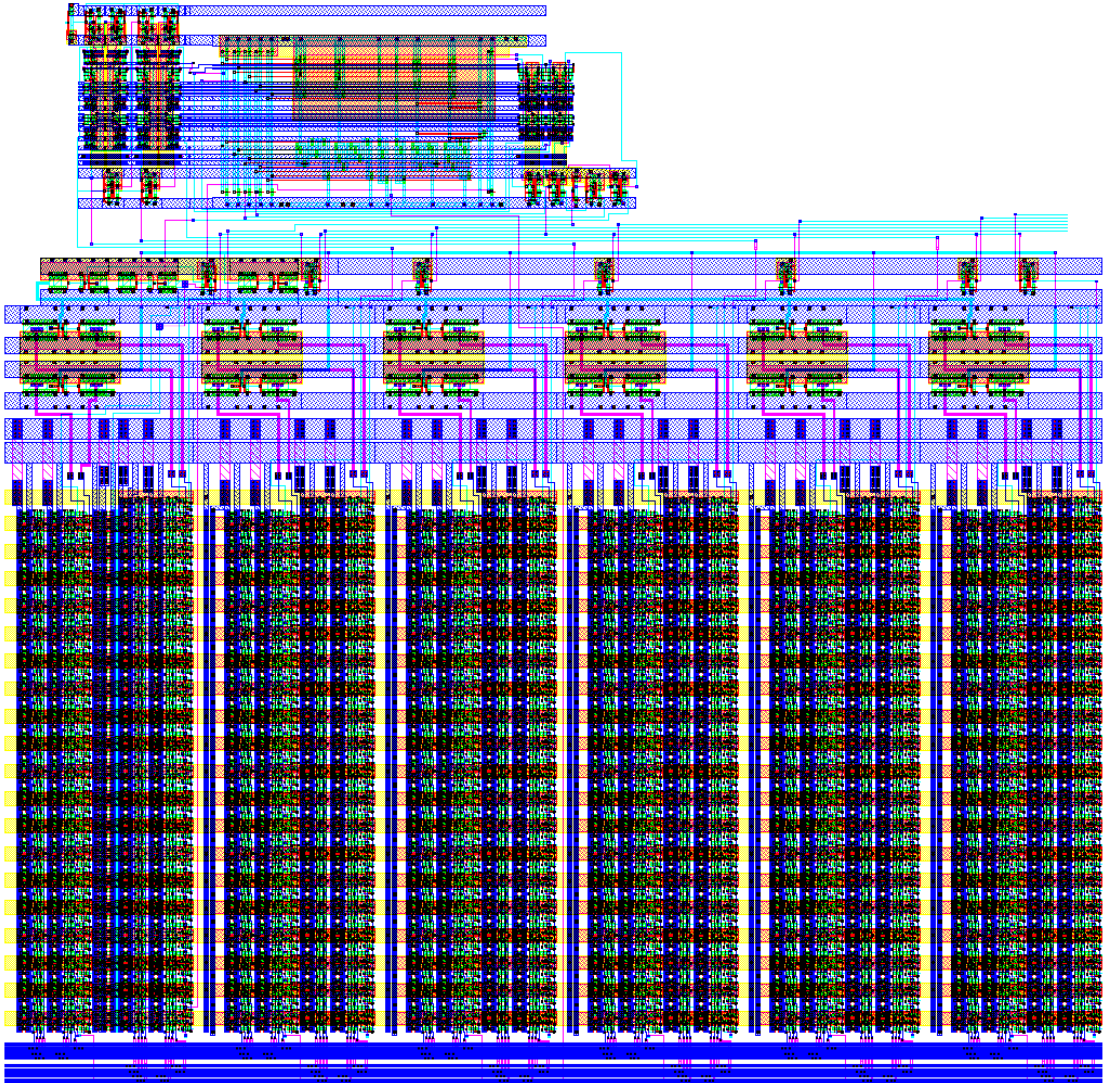
Cell: 1 2 3 4 5 6 7 8 9 10

Register cells on 4 µm pitch

Mirrored layouts : Nwells of adjacent cells are butted together, to minimise transistor separations

Layout is 3 times more compact than CPR2 non-mirrored layout

intermediate memory



Area 320 x 315 μm

- Provides local storage of data and header bits
- Interface between first and second level mux stages
- New compact layouts - 6 bits in separate blocks over 320 microns

Conclusions

Status

- CPR2A chip has been designed to build on the success of the CPR2, but with greater memory depth to reduce dead time problems.
- CPR2A layout largely completed.
- Final verifications with realistic simulated physics data are being performed.
- Submission by October

Next steps

- Plan to realise further versions of the readout chip on 0.13µm technology.
- Next version will have more memory and a more sophisticated sparsification algorithm to reduce dead time problem.