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Development of an ASIC for reading out CCDs at the vertex detector of the International Linear Collider

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The Linear Collider Flavour Identification Collaboration is developing sensors and readout electronics suitable for the International Linear Collider vertex detector. In order to achieve high data rates the proposed detector utilises column parallel CCDs, each read out by a custom designed ASIC. The prototype chip (CPR2) has 250 channels of electronics, each with a preamplifier, 5-bit flash ADC, data sparsification logic for identification of significant data clusters, and local memory for storage of data awaiting readout. CPR2 also has hierarchical 2-level data multiplexing and intermediate data memory, enabling readout of the sparsified data via the 5-bit data output bus.

Summary

The ILC will bring into collision e+ and e- beams at centre-of-mass energies of initially 200 to 500GeV. The products of the resulting interactions will be recorded by two detectors. An important component of each of these is the vertex detector. This is designed to measure very precisely the tracks of charged particles close to the interaction point (IP), allowing the identification of those which originate from decay vertices displaced from the IP. Hence, particles containing b and c quarks and tau leptons can be efficiently detected.

To achieve the necessary precision, the vertex detector sensors must have a resolution < 5 microns and present a minimum of material to the particles which traverse them. The power consumption of the sensors and their associated readout systems must thus be small, allowing gas cooling. These requirements are fulfilled by CCDs, on which the LCFI Collaboration has concentrated its R&D efforts.

The high pair production backgrounds at the ILC require that the CCD pixel columns be read out in parallel at 50MHz if the occupancy is to be kept below the 1% desirable for pattern recognition. This requires a readout chip with a channel for each column of CCD pixels. The low occupancy makes on-chip data sparsification desirable. The CPR2 is a prototype which fulfils this requirement. The 250 channels of the chip are on the same 20microns pitch as the CCD columns. For test purposes, channels are divided into two types, half driven by charge preamplifiers directly coupled to the CCD outputs, the other half by voltage preamps connected to the CCD through source followers.

The amplified voltages are sampled and digitised at 50MHz. The 5-bit ADCs produce a modified Gray code which reduces the effect of single bit digitisation errors. This is fed to the cluster finding logic which computes the (6-bit) sums the data in two vertically separated pixels in the same column. This is added to the same sum produced by the channel to the right to produce the sum of a 2x2 group of pixels (7-bits). The result is compared with a 7-bit threshold. If the threshold is exceeded, nine 5-bit data words are stored in the channel buffer memory with a global, counter generated, 15 bit timestamp word (stored as three 5-bit words). The channel also triggers storage of the equivalent data for 3 neighbouring channels. Thus, the data for a matrix of 4x9 pixels is stored together with the associated timestamps. Since all channels perform the same operations, all possible 2x2 clusters are stored if the associated sum exceeds the threshold. Internal data storage is needed because the chip has only one (5-bit) output bus, the internal memories are continuously read out to the bus by a clock-driven multiplexer at 8 times the front end frequency.

Testing of CPR2 has confirmed its basic functionality. The next iteration (CPR2A)

will incorporate improved digital functionality, with additional internal memory, to increase the efficiency of readout of clusters at occupancies of ˜1% for an increased period of time.

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