Status of the Optical Multiplexer Board 9U Prototype

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Abstract

This paper presents the architecture and the status of the Optical Multiplexer Board (OMB) 9U for the ATLAS/LHC Tile hadronic calorimeter (TileCal). This board will analyze the front-end data CRC to prevent bit and burst errors produced by radiation. Besides, due to its position within the data acquisition chain it will be used to emulate front-end data for tests. The first two prototypes of the final OMB 9U version have been produced at CERN.

Detailed design issues and manufacture features of these prototypes are described. Functional descriptions of the board on its two main operation modes as CRC checking and data ROD injector are explained as well as other functionalities. Finally, the schedule for next year when the production of the OMB will be take place is also presented.

I. INTRODUCTION

TileCal [1] is the hadronic tile calorimeter of the ATLAS-LHC [2] experiment and consists in terms of electronic readout of roughly 10000 channels read each 25 ns. Data gathered from these channels are digitized and transmitted to the Data Acquisition System (DAQ) following a three level trigger system (Fig.1).

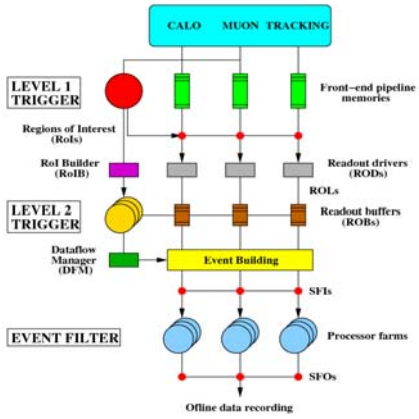


Figure 1: The ATLAS three levels trigger system.

The main component of the back-end electronics of the TileCal sub-detector is the Read-Out Driver (ROD) [3] which is placed between the first and the second level trigger. The ROD has to pre-process and gather data coming from the Front End Boards (FEB) and send these data to the Read-Out Buffers (ROB) in the second level trigger.

TileCal electronics will receive about 2 Gy/year (0.2 Krad/year) of radiation for a total dose of 20 Gy in the experiment lifetime [4]. To measure radiation hardness of TileCal FrontEnd electronics, tests were conducted with proton beams in different areas and with different beam sizes. Thanks to these tests, three non-destructive kinds of errors were found:

- Transient error in the data flow out to the ROD.
- Permanent errors in the data flow requiring reset.
- Latch-up error with an increment in current consumption of 60 mA.

To reduce data loss due to radiation effects, the TileCal collaboration decided to include data redundancy in the output links of the FrontEnd. This was accomplished using two optical fibres which transmit the same data. At ROD system level, data redundancy is used to discard the fibre with errors due to radiation. The checking is based on rightness of the Cyclic Redundancy Codes (CRC) of the data packets on both fibres. This is also necessary as the ROD motherboard is expecting just one fibre per channel. For this purpose a new module, called PreROD or Optical Multiplexer Board (OMB) was conceived (Fig. 2). This board would be able to provide, in case of error in one link, the correct data to the ROD input by analyzing the Cyclic Redundancy Codes (CRC) of the data packets on both fibers coming from the FEB.

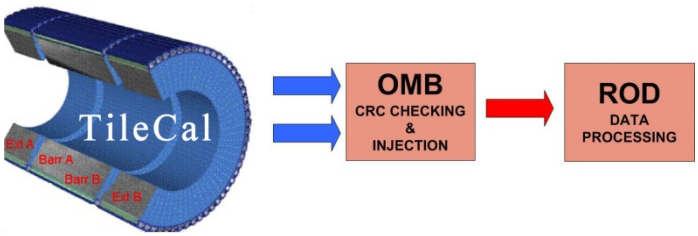


Figure 2: The OMB in the TileCal data acquisition chain.

While the developing of this board a new functionality for OMB was proposed. Because RODs should be tested in production stages and provided that in the first moments of LHC operation data may not always be available from front-end, it was suggested to include a “Data Injector Mode” to use the OMB like data pattern injector for ROD test and verification tasks.

The results of the first OMB 9U prototype are described in this paper as well as the functional description and technical specifications. Finally, the schedule for the OMB 9U production, installation and commissioning which will take place along this year is presented.

II. The OMB 9U final prototype

The final OMB 9U prototype (Fig. 3) is designed from the 6U board experience [5]. This prototype is conceived in a 1 to 1 ratio with respect to the RODs, i.e. each board has 16 input links and 8 output links, setting the final format in a 9U VME standard board.

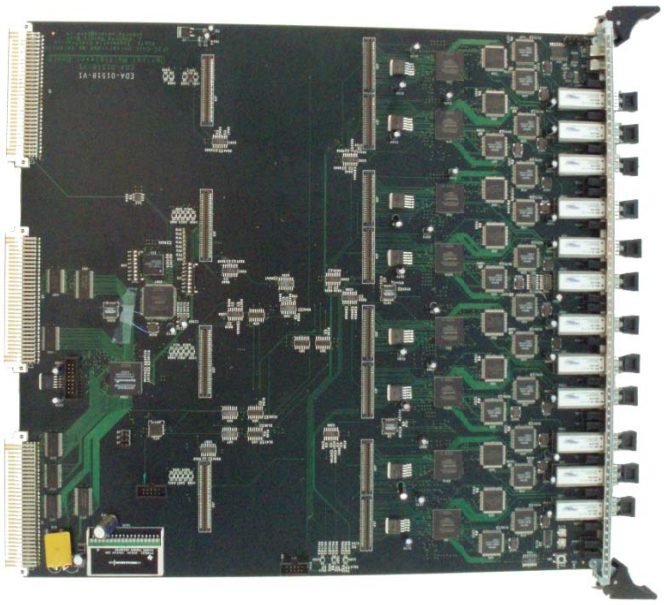


Figure 3: Picture of the OMB 9U prototype board.

From the functionality point of view there are some minor modifications being the most important, the inclusion of the TTC receiver chip. This would lead to the possibility receiving the trigger directly from the TTC system. In view of future upgrades and to increase the functionality the design includes four PMC connectors for mezzanine boards connected to the CRC FPGAs and is designed for 80 MHz operating frequency instead of the nominal 40 MHz of the LHC. This last issue poses some problems related to signal integrity and component placement aspects. Among them, the use of a single JTAG chain for the programming of all the FPGA chips in the board, the bus connecting the VME controller and the CRC controllers and the clock distribution are the main concerns.

III. Operation modes

A. *CRC Checking*

In the CRC checking operation mode the OMB 9U receives 16 fibers from 8 Optical Interface Boards (OIB) and transmits 8 fibers to one ROD (Fig. 4). Each CRC-FPGA must check the CRC of two redundant inputs and decide which one is transmitted to the ROD system. Moreover, the decision has to be taken in real time but a latency time is introduced in the acquisition chain. The algorithm that decides which fiber is transmitted and which is discarded consists of two simultaneous operations. The events received through each input link are stored in two different memories while the CRC is computed. The last word of the event includes the global CRC computed in the Front-End over the entire event. When this word is received the algorithm checks the CRC and decides which memory output is enabled.

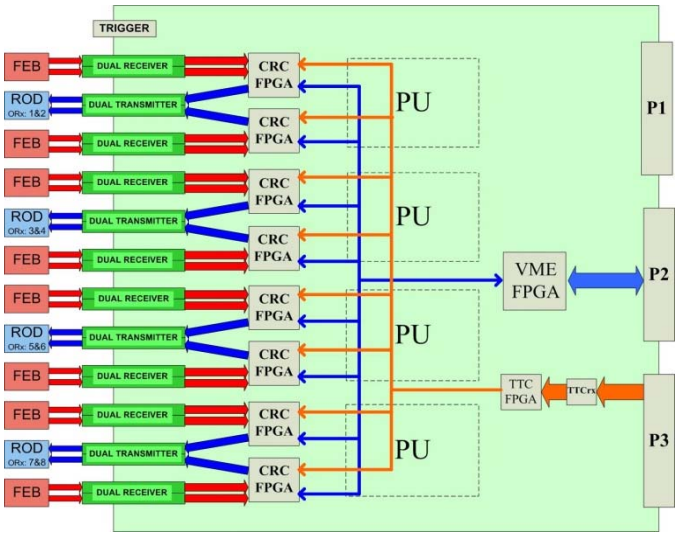


Figure 4: Dataflow of the OMB 9U prototype CRC checking operation mode.

Apart of the global CRC, it is possible to decide which fiber is transmitted to the ROD system by checking the DMU CRC (included in the trailer) or the BCID (included in the header) of each DMU data block (16 per event). All the errors detected are counted and stored in the corresponding internal register.

B. *The Injection Mode*

There are two different injection modes as described above for the previous 6U board: the counter and the memory injection modes. The main differences with the previous 6U version are the number of output channels and the possibility of the injection of data with actual TTC information. With a OMB 9U it is possible to inject data to a whole ROD through its 8 optical outputs (Fig. 5). Furthermore, the TTC feature permits the injection of data with the TTC information received through the backplane. Since this information is also received in the ROD, it is possible to test the TTC synchronization at ROD level with the data generated in the OMB 9U.

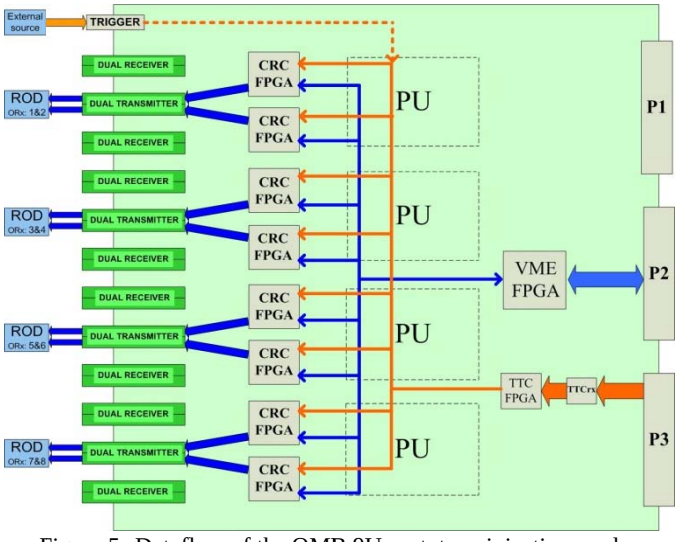
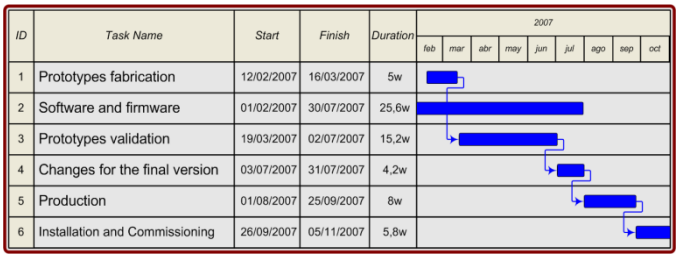


Figure 5: Dataflow of the OMB 9U prototype injection mode

IV. FUTURE WORK

The first OMB 9U prototype board is actually being validated. The conclusions drew during this phase will help us to implement minor changes before starting the production. At the same time, the firmware and control software are being developed to fulfill all the requirements (Fig. 6).



ID	Task Name	Start	Finish	Duration
1	Prototypes fabrication	12/02/2007	16/03/2007	5w
2	Software and firmware	01/02/2007	30/07/2007	25,6w
3	Prototypes validation	19/03/2007	02/07/2007	15,2w
4	Changes for the final version	03/07/2007	31/07/2007	4,2w
5	Production	01/08/2007	25/09/2007	8w
6	Installation and Commissioning	26/09/2007	05/11/2007	5,8w

Figure 6: Schedule for the OMB 9U production.

The production will consist of 38 boards, 32 to be installed at the ATLAS pit and 6 spares. The board production includes the fabrication, assembly and all the validation tests before its installation in the TileCal experiment acquisition chain. Fig. 6 shows the expected schedule for the production, installation and commissioning of the TileCal OMB.

V. REFERENCES

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