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Software environment for controlling and re-configuration of Xilinx Virtex FPGAs

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The Time Projection Chamber (TPC) is one of the sub-detectors of the ALICE detector that is currently being commissioned as a part of the Large Hadron Collider (LHC) at CERN. The Detector Control System (DCS) is used for control and monitoring of the system. For the TPC Front End Electronics (FEE) the control node is a Readout Control Unit (RCU) that communicates to higher layers via Ethernet, using the standard framework DIM (Distributed Information Management). The RCU is equipped with commercial SRAM based FPGAs that will experience errors due to the radiation environment they are operating in. This article will present the implemeted hardware solution for error correction and will focus on the software environment for configuration and controlling of the system.

Summary

In this article the implementation of the DCS for FPGA configuration and error correction in the TPC Front End Electronics (FEE) is introduced. In the field layer the DCS consists of an RCU (ReadOut Control Unit) motherboard with DCS (Detector Control System) board and several Front-End-Cards (FECs) attached. On the RCU an SRAM based Xilinx Virtex-II Pro FPGA is essential for the read-out chain. Since the Front-End-Electronics operates in a radiation environment single event upsets can occur. The Xilinx Virtex-II supports a feature called Active Partial Reconfiguration. This allows for reconfiguration of the FPGA without interrupting operation. There is also radiation tolerant 8 MB of Flash memory and a Flash based Actel FPGA on the RCU motherboard. The Actel FPGA communicates with the DCS Board, the Flash Memory and the configuration memory of the Xilinx Virtex-II. This hardware solution has three different modes of operation: initial configuration, scrubbing (continously overwriting the configuration memory) and frame by frame readback verification and error correction. The last mode reads back every frame one by one and if an error is found this one frame is overwritten in the configuration memory. It is also possible to count the number of errors that occured using this mode.

The DCS board drives a Linux Operating system which provides a communication system called the FeeServer (Front-End-Electronics Server). The FeeServer is in charge of publishing values and status information as well as receiving commands from the upper layers. To provide a remote way for configuring the Xilinx a Linux device driver is used and functions in the FeeServer have been implemented to access the Xilinx device through the standard communication channels. The FeeServer consists of a device independent core and the so called ControlEngine (CE) to support the use in different detectors. Finite State Machines (FSM) for each mode of operation have been introduced in the Control Engine of the FeeServer. In case of a frame by frame readback verification and error correction it is also possible to publish the number of occurred errors to the higher layers.

Configuration files are stored in the Configuration Database and are transported by the DCS communication software to the FeeServer. Since error tolerance and robustness are mandatory checksums are used to check the data integrity. This article focuses on the software part of the configuration and error correction modes.

Although the presented remote configuration functionality was developed for the RCU and the Virtex-II, it is possible to use this solution in other parts of the detector as well. In these parts the devices to be configured are Xilinx Virtex-4s, which are also supported by the device driver.

Primary author: Mr FEHLKER, Dominik (University of Bergen)

Co-authors: Mr SCHOCKERT, Benjamin (University of Applied Sciences Worms); Ms GONZALEZ GUTIERREZ, Carmen (CERN, European Organization for Nuclear Research); Mr LARSEN, Dag (University of Bergen); Prof. RÖHRICH, Dieter (University of Bergen); Prof. HELSTRUP, Håvard (Bergen University College); Mr ALME, Johan (University of Bergen); Mr RØED, Ketil (Bergen University College); Prof. ULLALAND, Kjetil (University of Bergen); Mr MUSA, Luciano (CERN, European Organization for Nuclear Research); Mr RICHTER, Matthias (University of Bergen); Prof. KEIDEL, Ralf (University of Applied Sciences Worms); Mr CAMPAGNOLO, Roberto (CERN, European Organization for Nuclear Research); Mr BABLOK, Sebastian (University of Bergen); Prof. BEIERLEIN, Thomas (University of Applied Sciences Mittweida); Mr KRAWUTSCHKE, Tobias (University of Applied Sciences Cologne); Mr ALT, Torsten (University of Heidelberg); Prof. LINDENSTRUTH, Volker (University of Heidelberg)

Presenter: Mr FEHLKER, Dominik (University of Bergen)

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