DT Sector Collector electronics design and construction

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Abstract

The CMS detector at LHC is equipped with *Drift Tubes* (DT) chambers for muon detection and triggering in the barrel region. The *Sector Collector* (SC) modules collect the track segments reconstructed by on-chamber trigger electronics. Data from different chambers are aligned in time and sent to the subsequent reconstruction processors via optical links. Several FPGA devices performing the processing of the data were designed in VHDL, including spy features to monitor the trigger data flow. A test jig was set up with custom hardware and software in order to fully validate final production boards. Installation and commissioning in CMS provided first experience with the synchronization and monitoring tools.

I. DRIFT TUBES DETECTOR AND TRIGGER

A. DT muon detectors

The aim of the muon system [1] is to provide a robust trigger, with bunch crossing (BX) assignment, identification and momentum measurement of the muons produced in the p-p collision in a wide transverse momentum (Pt) range. The system is embedded in the return yoke of the magnet, and the bending given by the magnetic field inside it is used to provide a Pt assignment for muon tracks. Drift Tubes (DT) detectors are used in the barrel region. The DT system is segmented in 5 wheels along the z direction, each about 2.5 m wide and divided into 12 azimuthal sectors, covering 30° each. Cross sections are shown in Fig. 1: DT chambers are arranged in 4 concentric cylinders – called stations – within each wheel, at different distance from the interaction point, and interleaved with the iron of the magnet yoke.
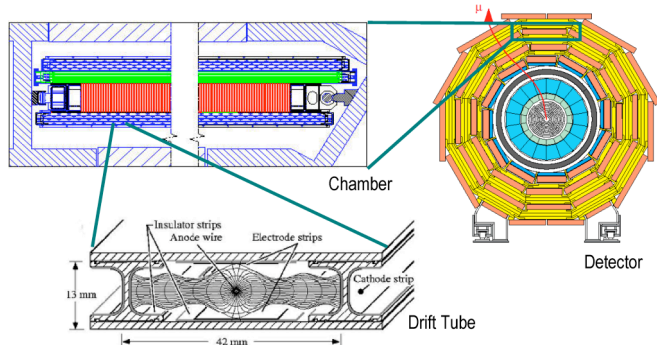

Figure 1: DT layout overview: cell, chamber, wheel cross sections.

Each DT chamber is instrumented with staggered layers of Drift Tubes. A group of four DT planes is called *superlayer*;

chambers are intrumented with two spaced superlayers in the transverse (r,ϕ) plane and one in the longitudinal (θ, z) plane.

B. DT Trigger

A *Local Trigger* system is installed on DT chambers [2]. It consists of trigger boards, assembled together with readout electronics in *minicrates* that are mounted on each chamber. A pipelined architecture of ASIC devices (running synchronously with LHC BX frequency) is able to recognize track segments crossing the chamber, after a fixed latency. The meantimer property derived from geometry of the staggered DT planes is used to recognize the alignment of hits after a fixed time that is equal to the cell maximum drift time [3]. Thus, the originating BX is identified and position and impact angle are assigned to the segments.

Local trigger data of each chamber, consisting at each BX of two segments in the ϕ view and hits in the θ view, are output using serial LVDS running at 480 Mb/s on two FTP cables, up to 40 m long [4]. Cables are routed out of the detector and reach crates on crates located in structures surrounding the detector, called towers.

Tower crates host trigger and readout boards receiving data from the minicrates. The *Trigger Sector Collector* (SC) board collects and synchronizes the trigger information from one sector (4 or 5 chambers) [4]. Tools to monitor the data flow allow the timing of the different data paths to be spied in order to apply correct transmission delays [5]. Optical links are used to transmit data to the underground counting room (about 60 m long path) where optical receiver boards fan out the trigger data to the *Drift Tubes Track Finder* (DTTF).

The DTTF is a system of custom processors that performs a further correlation of the track segments delivered by the local trigger of different chambers. An extrapolation algorithm is used in the ϕ view, while a pattern matching method is implemented for the θ view. The process is efficient only if the track segments from the chambers are received at the same BX. Thus, the synchronization at the SC level is fundamental for the regional trigger operation.

II. SECTOR COLLECTOR HARDWARE DESIGN

The SC boards were developed according to a modular design. The data I/O and processing are implemented on mezzanine cards, hosted by a VME 9U motherboard that provides connections and a VME interface.

The custom processing units are based on FPGAs, designed in VHDL. Flash-based FPGAs (ProAsicPlus from Actel) were chosen for the electronics installed in the cavern

for their higher immunity to functionality interruptions due to ionization events that are mainly induced by low energy neutrons in the area outside the yoke [6]. The risk is that one single event flipping one bit of the FPGA configuration memory may lead to unpredictable behaviour of the device. The ProAsicPlus chips do not use S-RAM to retain the device configuration bits, but Flash cells. These cells are more robust against low energy ionization events in the silicon, ensuring an interruption-free operation [7,8].
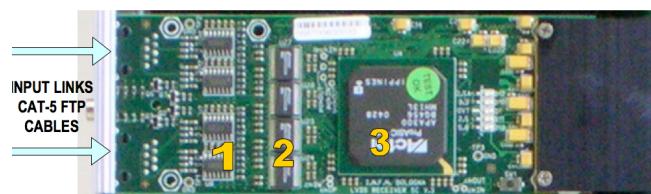

Figure 2: The LVDS-RX mezzanine.

A. Receiver mezzanines (LVDS-RX)

In Figure 2, the LVDS-RX mezzanine is shown. It receives data from one minicrate. On the left side two connectors for FTP cables are placed; numbers show the devices handling the data flow: (1) cable equalizers (2) deserializers and (3) FPGA. The FPGA monitors the deserializers lock status and the parity of the received data. It includes also embedded RAM that is implemented as a spy buffer with JTAG readout. The full chip I/O can be spied, with a depth of up to 256 BXs. The FPGA design includes a sorting block to compare the information between the two cables and perform a selection based on the quality of the track candidates. At the output, a pipe of configurable length can be used to add a delay to data paths, and test patterns can be generated.

B. Optical transmission mezzanine (OPTO-TX)

Data from the four LVDS-RX mezzanines connected to the minicrates of the DT sector are delivered to a single OPTO-TX mezzanine (Figure 3). Six GOL chips [9] are used, in 1.6 Gb/s gigabit-ethernet mode with a clock filtering and fan-out circuit based on a QPLL [10]. On the left edge of the board, six 850 nm VCSELs from Honeywell are placed. GOL chips configuration and status registers are accessed through both JTAG and I2C interface, the latter is used also to read an ADC that monitors the light emitted by the lasers.

Figure 3: The OPTO-TX mezzanine.

C. Motherboard

The motherboard (see in Figure 4 a fully equipped motherboard) provides connections between the mezzanines, feeds clocks to all synchronous devices and hosts one FPGA. This device (number (1) in the picture) has been designed with a VME interface and control logic that permits access to all programmable resources of the board. In the picture the following details are also underlined: (2) the J1 connection to the VME bus, (3) the phase control devices for the board clocks, (4) connection to the near readout board (ROS, [13]) via a custom J3 backplane.
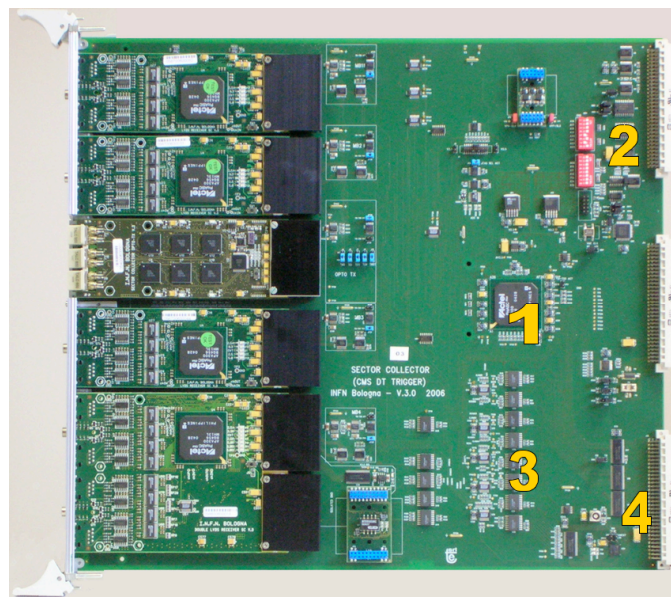

Figure 4: The Trigger Sector Collector board.

LVDS-RX mezzanines also send a subset of the trigger data flow to the control device. This information includes quality of the local segments (i.e., the number of hits that are aligned). Using a RAM-based buffer embedded into the control chip, blocks of data words can be spied at the triggering BX to verify the alignment of track segments delivered by the different stations. Data can be read out via VME or injected into the event data through the J3 connection to the ROS board. More details about the synchronization features of the design are given in section IV.

D. Optical Receiver card (OPTO-RX)

Multimodal optical fibers driven by the OPTO-TX mezzanine are routed to the underground counting room, where OPTO-RX cards are plugged into the backplane of the DTTF crate. In Figure 5 a picture of the OPTO-RX card is shown: on the leftmost edge the 6 receiver diodes can be seen, serial data are then routed to the central FPGA (an Altera StratixGX) that embeds the gigabit deserializers and checks the link status and the trigger data parities.

The optical link can also be fully tested setting on the GOL chips a test mode. The generated patterns are automatically checked on the OPTO-RX FPGA, at full speed,

allowing faster BER tests. The status and configuration registers on the FPGA are accessed through a JTAG chain [11] that is driven by the corresponding DTTF module.
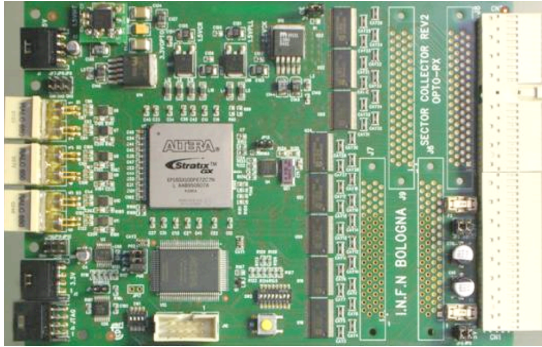

Figure 5: The Optical Receiver board.

III. TEST-BENCH

All the electronics parts that were produced were exhaustively tested to verify all the functionalities before the installation in CMS. This was done to reduce to the minimum the possible problems during the installation and commissioning phase.

A. Connectivity test and full-test concepts

A preliminary connectivity test bench was set up at the firm that produced the mezzanine cards. This was a complete boundary scan test [11] using JTAG resources that allowed all lines between chips to be verified. In this way, problems in soldering (in particular concerning the devices in a BGA package) can be found before the final assembly and FPGA programming.
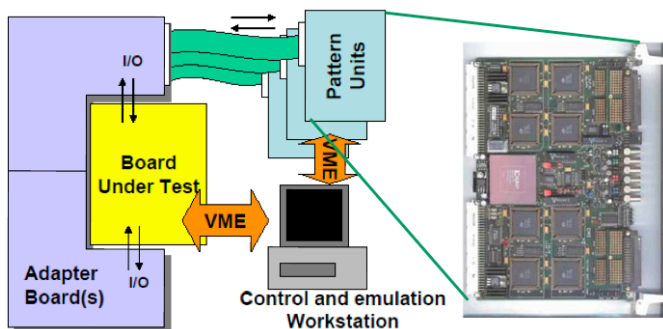

Figure 6: Dynamic test bench schematic view.

A full test bench was set up in INFN Bologna laboratory to finally assembly and validate each SC module. The purpose of the test bench is to check the behaviour of the modules in "real life" conditions. This means that the full I/O of the board must be run with 40 MHz data. In Figure 6, the test concept is shown: the device under test is connected through adapter boards to modules, called *Pattern Units*, developed by the CMS-Bologna group [12]. The Pattern Units are VME testing

devices, providing up to 128 I/O running up to 100 MHz speed. A set of synchronously controlled Pattern Units is used to inject data into the system and to read the device under test output. C++ programs were developed to generate random data and to emulate the board logic. The test software controls directly also the SC under test through VME and JTAG connections. This allows also the spy and self-test features of the hardware to be verified and compared with the trigger I/O.

B. Sector Collector production test

In Figure 7, a picture of the test setup is shown. Under test are a fully equipped SC motherboard connected to the OPTO-RX board. Numbers show (1) the SC motherboard under test (2) the OPTO-RX card plugged to an output adapter (3) the input adapter board, with FTP cables routed to SC board (4) the custom J3 backplane for clock and spy data, (5) the 6U VME crate hosting the VME interface, the Pattern Units and TTC modules.
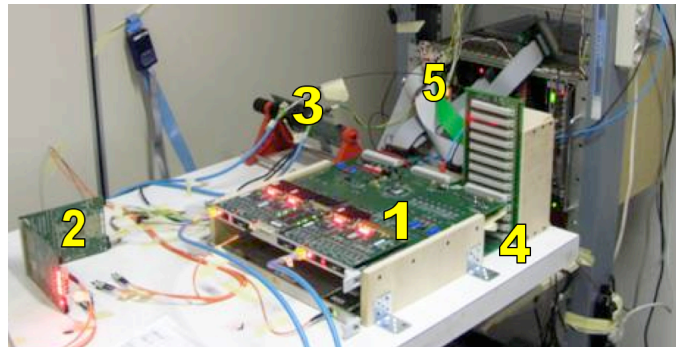

Figure 7: The TSC full test setup.

The test procedure starts with the SC motherboard without mezzanines installed. The firmware of the FPGA is loaded through the VME interface and the chip is tested in stand-alone. This test verifies the VME access to the spy resources, the connection to board sensors and also the clocks of the board. The control FPGA monitors also the mezzanine clocks and the control of clock phases is verified.

When the motherboard is equipped with the mezzanines, the LVDS-RX firmwares are loaded. The mezzanines are checked injecting data on LVDS cables and reading the FPGA outputs with the spy registers embedded in the designs. The spy data connections to the control FPGA are checked.

The OPTO-TX/RX connection is also stand-alone tested. The RX card is controlled through the JTAG interface to check the link locking. GOL chips are set to send test patterns recognized in the Altera FPGA firmware and the stability of the connection is checked while scanning the VCSELs bias currents. Finally, a full chain test from LVDS inputs to OPTO-RX outputs is run with random patterns.

The information from all test steps is stored by the test program in a log file, together with temperature, current drawing, voltages and laser light measurements obtained by on-board sensors and ADCs.

IV. COMMISSIONING

A. Installation and commissioning

The produced boards were installed on the detector tower racks together with readout boards (ROS, [13]). The final connections of trigger, readout, clock (TTC) and control paths were set up. Commissioning operations were staged following the connection of each sector of the DTs. A data taking procedure with several kinds of runs was followed.

Noise runs use random triggers to read out the chambers and check the noise level in all the cells.

In test pulse runs, pulses emulating vertical tracks are injected on the front-end electronics. A test pulse event is shown in Figure 8. At each event, the position of the pulses is shifted by one cell to scan all electronic channels. The local trigger will deliver tracks to the SC boards so that the pulsing can be used to verify the synchronization of the trigger chain.
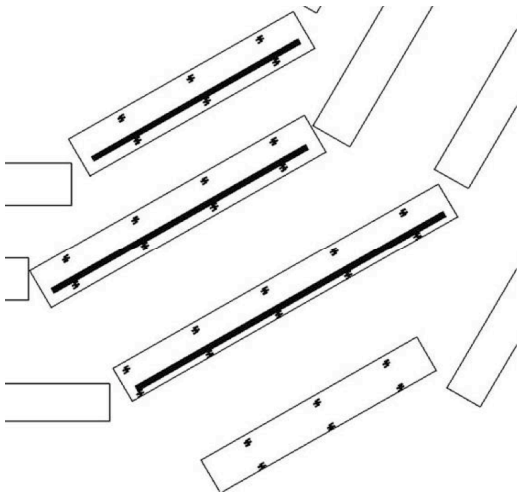

Figure 8: A test-pulse event in one sector (phi-view).

Finally cosmic muons are triggered and a set of data is taken for each sector. Data are used to evaluate the performance of the detectors and of the trigger electronics. For cosmics data taking, a special *Technical Trigger* can be used. A single chamber delivering a track segment with a quality above a threshold can trigger the event readout. The multi-chamber correlation performed by the DTTF is not used in this case. This is particularly useful in taking data with cosmics: the trigger rate can be increased in sectors where the overlap of the stations for nearly vertical cosmic muons is very small.

B. Trigger synchronization

The synchronization of the trigger links from the chambers during the commissioning phase provided experience with the monitoring and control tools designed in the SC devices.

In Figure 9 a schematic view of the trigger data paths in the Sector Collector board is shown. One LVDS-RX mezzanine is shown, but the same structure is implemented for all the data paths.
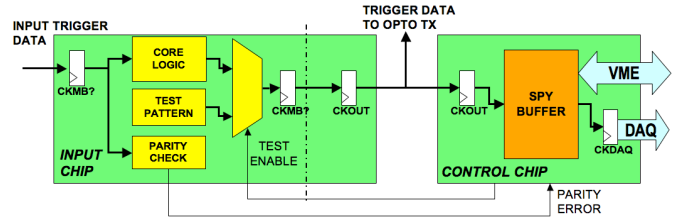

Figure 9: The timing of the trigger data is checked at the hardware level (shown for one chamber data only).

Trigger data from the chambers are sampled into the FPGA using an independent, phase adjustable clock for each mezzanine (CKMB? in the picture). The FPGA compares the parity of the received data with the included parity bit. The resulting parity error bit is delivered to the control FPGA where it is retained while a scan of the input clock phases is performed. In this way a clear picture of the data phase on the input links is obtained, and a good sampling phase for each chamber is chosen.

The four LVDS-RX mezzanines have a common output clock (MBOUT in the figure). This ensures the data from all chambers are aligned on a single phase at this point. To verify the transition of data bits from the input to the output registers, the mezzanine FPGA generates test patterns that follow the same path of real trigger data. The test patterns are spied on the control FPGA and another phase scan produces the information on valid phases for the output clock.

The control FPGA spy is then set to monitor the coarse synchronization information from the chambers. In fact, all the minicrates receive a synchronous *Bunch Crossing 0* (BC0) signal, once per orbit. This signal is used to start BX counters on all minicrates. The least significant bits of the counters and the BC0 signal are output with data. Thus, the control FPGA can verify any misalignment of the counters and apply a correction by adding clock-cycles delay to the output stage of the LVDS-RX FPGAs. At this point, the trigger data are aligned at the same BX and to the same clock phase and can be sent to the optical links. Up to this stage, the synchronization process used only VME access to the SC board and pulsing of the front ends.

C. Trigger data spy

The control FPGA spy buffer can also deliver the spy data to the neighbour readout board. The quality of the ϕ track segments, θ hits and other information are stored in a 128 BX long buffer. At each L1A, the buffer is frozen and data concerning a configurable number of BXs around the one that generated the L1A are transferred to readout board. Thus the trigger spy information is embedded in the readout data and can be monitored via the Data Quality Monitor tools available during data taking.

In Figure 10, the histogram of the trigger timing as spied by the SC is shown. For each chamber of the sector, the plot shows the number of track segments found at each BX inside the spied window. It is clear that the four chambers are triggering mainly at the same bunch crossing (19 in the scale used). This is a proof of the synchronization, when the technical trigger is used, since each chamber can independently generate the L1A. The width of the distribution

is mainly due to the fact that the muons arrive at the detectors at any time, without any bunched structure. At LHC, a fine synchronization of each chamber clock with respect to the BX will be tuned, as it was demonstrated in a test beam [14, 15]. Furthermore, the histogram shown accumulates entries made of track segments of any quality, while their timing behaviour strongly depends on the number hits they are based on.
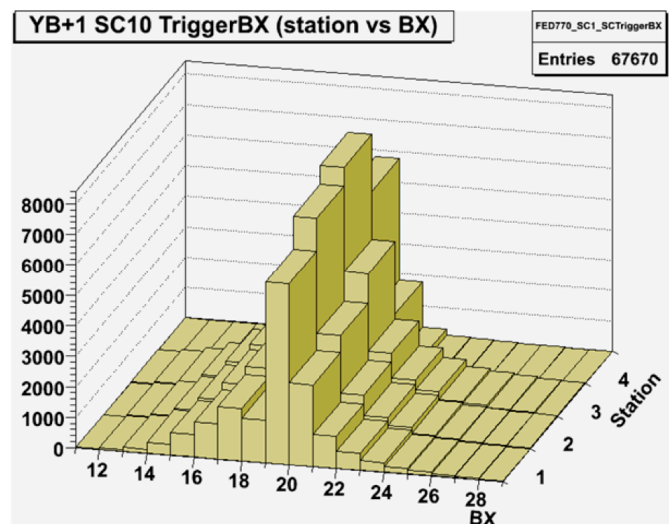

Figure 10: Number of triggers vs bunch crossing number for each station within a given sector. The timing can be easily checked.

This is shown in Figure 11, where the track segments are divided by quality – from 3 hits segments (L) up to 8 hits segments (HH) built with both superlayers – and the number of segments found at each BX is represented by the area of the boxes. It can be noticed that the L segments have a broader distribution in time, as it is easier to find a *ghost* alignment of 3 hits in the bunch crossings preceding and following the right one, where a higher quality track is usually found. The L segments can be found also *before* the trigger BX (19 in the plot) because they were not accepted as L1A sources, applying a threshold on the quality that required at least one H segment.
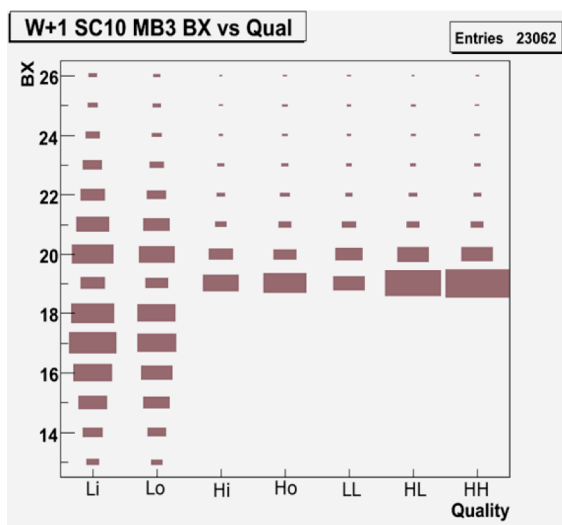

Figure 11: Bunch crossing number versus quality of the trigger primitives.

V. SUMMARY AND CONCLUSIONS

A general overview of the CMS DT muon detectors and trigger system was given. The main tasks and design features of the trigger Sector Collector modules were described with some implementation details. The electronics is based on custom FPGA designs, implementing the trigger algorithms and useful test and data spy features. The modules were tested in their working conditions using a test bench based on custom I/O units. The installation and commissioning phase proved the electronics behaves as expected. Monitoring and spy resources implemented into the FPGA designed were successfully used in the synchronization of the trigger links on the Sector Collector board. The injection of the spy data into the readout stream allows the timing of the local trigger to be monitored on-line. The experience accumulated with cosmic muons in the commissioning phase will be used at the LHC startup, when the DT trigger will be synchronized to machine collisions.

VI. REFERENCES

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