Contribution ID: **54** Type: **Oral**

DT Sector Collector electronics design and construction

Friday 7 September 2007 10:10 (25 minutes)

The CMS detector is equipped with Drift Tubes chambers for muon detection in the barrel region. The Sector Collector modules collect the track segments reconstructed by on-chamber trigger electronics. Data from different chambers are aligned in time and sent to the subsequent reconstruction processors via optical links. Several FPGA devices performing the processing of the data were designed in VHDL, including spy features to monitor the trigger data flow. Prototypes of the boards were operated in the CMS "cosmic challenge". A test jig was set up with custom hardware and software in order to fully validate final production boards. First experience with installation and running in CMS will be shown.

Summary

The CMS detector at LHC is equipped with Drift Tubes (DT) chambers for muon detection in the barrel region. Local Trigger electronics, installed on the chambers, processes the hits and reconstructs local track segments within a fixed latency time. Local trigger data, comprising position, impact angle and reconstruction quality, is routed out and collected by Trigger Sector Collector (SC) modules, installed on the towers near to the detector.
Each SC board handles redundant links from the DT chambers of a 30 degrees sector of the detector, performing reduction and synchronization of the data. The correct synchronization of data from different chambers is crucial in order to allow the track segments to be further correlated by the following stage of the trigger system (Track Finder). Spy features on the SC modules allow the status of the links and the trigger data flow to be monitored, both through local access to the board (VME interface) and through the injection of part of the trigger data into the DAQ stream. Each SC module can also return a "sector trigger", generated as a Boolean function of the local segments, to the chambers of the sector and to the corresponding readout module. Thus, a sector-level trigger and readout system devoted to commissioning and system debugging is implemented.
The SC modules are built by several units: a VME 9U motherboard, hosting a board controller device that provides the VME interface, the interconnection with the readout modules and the sector trigger generation; four mezzanine cards, receiving data from the chambers of the sector, performing data reduction and spying; and a fifth mezzanine card, hosting serializers (GOL chips at 1.6 Gbit/s) and optical drivers for the fiber connection to the counting room, where optical-receiver modules deliver trigger data to the Track Finder boards.
The hardware implementation of the system profits of custom processors implemented on FPGA devices using VHDL programming. The modules installed on towers near to the detector are based on flash-FPGAs, ensuring high fault immunity in a moderate radiation environment. The optical receiver modules are operated in the underground counting room, with no radiation issues, thus they are built with sram-FPGAs that provide embedded gigabit-deserializers and more computational resources. Prototypes of the boards were installed and operated during CMS Magnet Test and Cosmic Challenge: three sectors of the DT detector were synchronized and provided cosmic triggers to the global DAQ. The magnet test allowed also the fringe field to be measured in the tower racks to estimate the required magnetic field tolerance of critical components used in the modules. The components were further tested in a controlled field to optimize their design before launching the final production. In order to validate each board before installation, a test jig was set up using VME

custom general purpose I/O modules (Pattern Units). The custom test software accesses the VME bus and it allows patterns to be injected and outputs to be read out at 40 MHz, while checking the status and the spy registers of the board under test.

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Session Classification: Plenary session P4