A low power and low signal 4 bit 50MS/s double sampling pipelined ADC for Monolithic Active Pixel Sensors

M. Dahoumane [a], D. Dzahini [a], J. Bouvier [a], E. Lagorio [a], J.Y. Hostachy [a], O. Rossetto [a], H. Ghazlane [b], D. Dallet[c]

[a] LPSC, 53 Av. Des Martyrs 38026 Grenoble, France.
[b]CNESTEN, BP 1382 RP 10001 Rabat Morocco
[c] IXL, 351 Cours de la Libération, 33405 Talence Cedex, France.

mokrane.dahoumane@lpsc.in2p3.fr

Abstract

A 4 bit very low power and low incoming signal analog to digital converter (ADC) using a double sampling switched capacitor technique, designed for use in CMOS monolithic active pixels sensor readout, has been implemented in 0.35µm CMOS technology. A non-resetting sample and hold stage is integrated to amplify the incoming signal by 4. This first stage compensates both the amplifier offset effect and the input common mode voltage fluctuations. The converter is composed of a 2.5 bit pipeline stage followed by a 2 bit flash stage. This prototype consists of 4 ADC double-channels; each one is sampling at 50MS/s and dissipates only 2.6mW at 3.3V supply voltage. A bias pulsing stage is integrated in the circuit. Therefore, the analog part is switched OFF or ON in less than 1µs. The size for the layout is 80µm*0.9mm. This corresponds to the pitch of 4 pixel columns, each one is 20µm wide.

I. INTRODUCTION

In the next generation of linear colliders required for future high energy physics experiments such as the International linear collider (ILC), precise vertex detectors will be necessary to study the Higgs mechanism. To build this high performance detector, three options are possible: Charge coupled Devices (CCD), Hybrid pixel Detectors (HPD), and Monolithic active pixel sensors (MAPS). Fabricated in standard CMOS technology, MAPS are an attractive alternative for the other detectors. They have several potential advantages like Low power, Low fabrication costs, high spatial resolution, flexibility, radiation hardness, compactness, random access and fast read-out.

The use of MAPS in particle physics will strongly depend on a successful implementation of an on-chip read-out electronics. This is not a trivial task because of different factors:

- Very small signal amplitudes, in the range of millivolts, which are the same order of magnitude as transistor threshold variations of a CMOS process;
- The technology process used has to be chosen according to the particle detection performances (e.g. epitaxial layer thickness);
- The layout has to be adjusted to the (small) pixel pitch;
- The number of metal layers is modest (only 4 layers);
- And the power budget is a critical issue, the consumption of pixel column ADC must be less than 500µW.

In this paper, a double sampling analog to digital converter (ADC) is described. It is designed according to the requirements of pixel arrays developed at IPHC-Strasbourg in collaboration with DAPNIA-Saclay, in perspective of the Linear Collider vertex detector [1]. Figure 1 shows the global architecture of the planned MAPS chip comprising the pixel array with its associated read-out and A/D conversion stages.

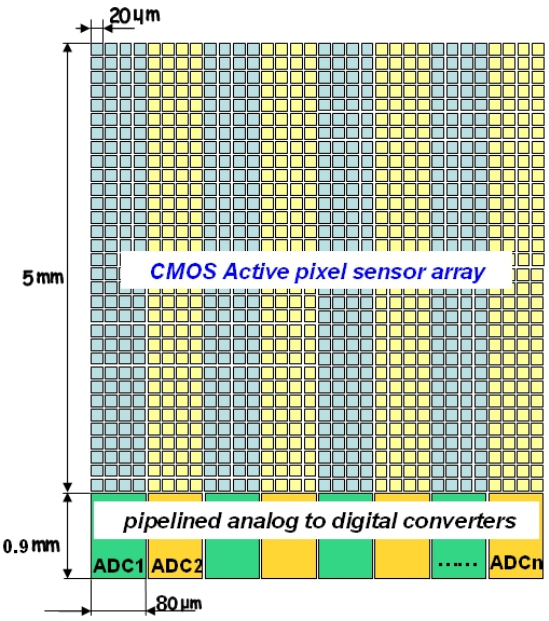

Figure 1: Global MAPS planned architecture

These MAPS are currently being developed and characterized at IPHC/Strasbourg in collaboration with CEA/Saclay and manufactured by TSMC through MOSIS [2], [3]. They are based on DC pixel architecture which comprises in-situ a first conditioning micro-circuit. The signal at the analog output is the difference between a reference level (calibration) and the readout signal (read). This leads the signal extraction and a reduction of the output pedestals (offsets). The pixel columns are read in parallel with a frequency in excess of 10 kHz. Each column is presently ended with a discriminator, which will be replaced in future by an ADC.

The pixel's columns width amounts to 25µm at present, but it should become 20 microns in the next prototypes. The minimal signal delivered by each column is typically on the order of a mV, which translates into a first challenge for the read-out circuit design. Next comes the fast sampling rate ambitioned (10 MS/s). Finally, the power budget should remain as low as about 500 µW/column.

The pixel common mode voltage fluctuation, the small value of the Least Significant Bit (LSB ~1mV), and the offsets make the design of the first stage of this converter very critical. With a sampling rate beyond 10 MHz, pipelined architecture provides the best deal between speed, consumption and area. An overview block diagram of a 4 bit pipelined ADC is shown in figure 2 [4], [5], [6] [7].

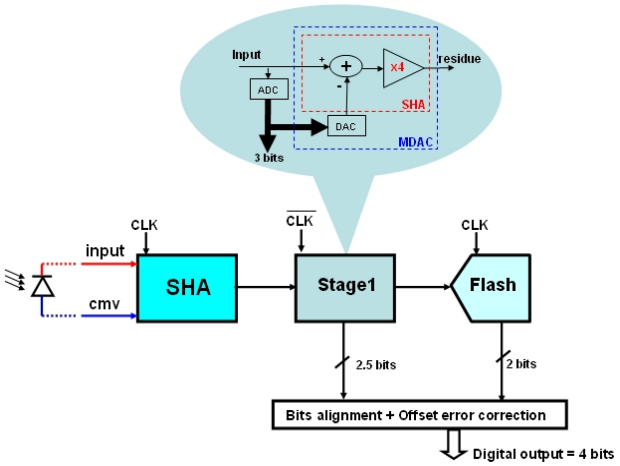

Figure 2: General block diagram of a 4 bit pipelined converter

The SHA stage samples, holds and amplifies the analog input signal. It is followed by a 2.5 bit pipelined stage and a 2 bit flash stage. The pipelined stage produces a digital estimate of an incoming held signal, then converts this estimate back to the analog, subtracts the result from the held input. This residue is then amplified before being transferred to the next flash stage which determines the least significant bits (LSB). The successive digital results from the ADC stages are appropriately delayed throughout a bit alignment network. Then a digital error correction stage is added to leave room for the comparator offsets correction. Therefore, comparator constraints are relaxed and the power consumption is reduced.

This paper describes hereafter each stage of this converter and we present some testing results.

II. THE SAMPLE AND HOLD AMPLIFIER (SHA)

A charge redistribution non-inverting architecture is used. Figure 3 illustrates the sampling phase (phi2 is ON). "vee_SH" is the name for the virtual ground. The signal is stored onto the set of 4 sampling capacitors (C37...C40). Then during the HOLD (phi1), the charge is transferred to the feedback capacitor C23. This results to amplification by 4 of the differential signal between the reference (dark level) and the intensity level. Each capacitor unit in this scheme is 127 fF. these capacitor values are chosen in function of the surface limitation and kT/C noise factor.

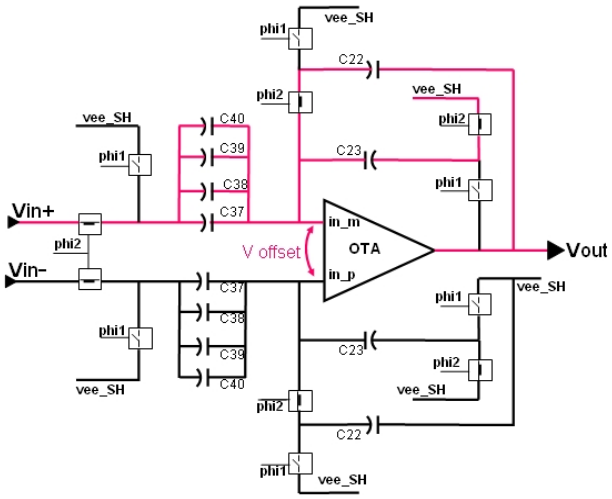

Figure 3: Sample and Hold Amplifier (SHA) scheme

A. The OTA architecture

Telescopic cascode architecture of the amplifier implemented is shown in figure 4 [8]. This amplifier is used in both SHA stage and pipelined stage.

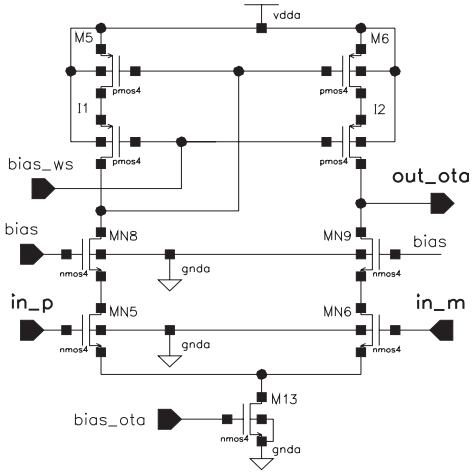

Figure 4: A wide swing telescopic OTA

The current mirror load is a so called "wide swing cascode" [3]. It improves the dynamic range better than a basic cascode and makes the design robust for future low voltage version. The Bode diagram simulations results on a 2 pF load capacitance and 177µA current consumption are shown in figure 5. It achieves a 40dB open loop gain and 100 MHz unity gain frequency with 80° phase margin.

The digressive power dissipation technique through the successive stages is implemented. Thereby, the amplifier of the pipelined stage dissipates only 85 µA.

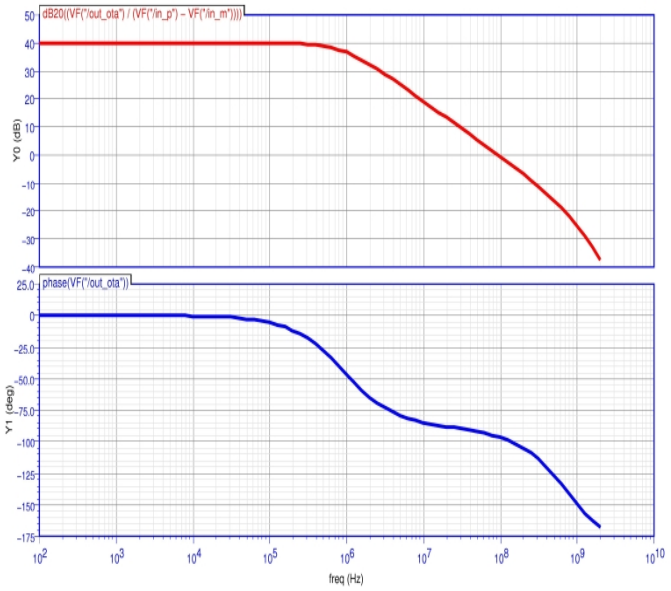

Figure 5: Bode diagram

B. *The SHA performances*

The architecture used for this first stage is not full differential because of the budget restriction in term of power and surface. This pseudo differential architecture compensates the offset errors coming from different sources.

1) *Compensation of the amplifier input offset:*

The amplifier offset is the voltage difference between the two inputs of amplifier. It is due to the process dispersion and layout mismatches. This offset is stored onto the feedback capacitor C23 during the sampling phase (phi2). During the hold phase (phi1), the charges are transferred from the sampling capacitors to the feedback capacitor C23 annulling the offset error and leading to an amplification in the ratio of the capacitors. Figure 6 shows the gain variation according to the input signal. It stays close to the optimal value of 4, when the OTA's offset parameter varies from -10 mV up to 10 mV.

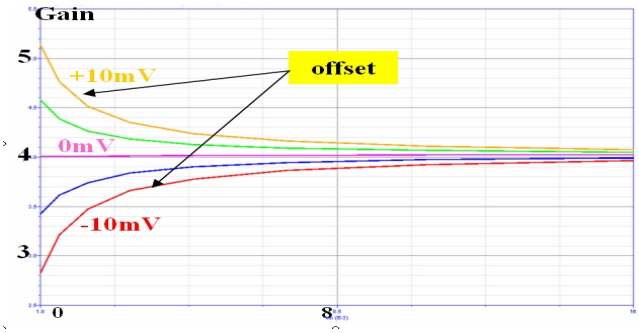

Figure 6: SHA gain according to the input signal, with the OTA offset as a second parameter

The gain error is more important for the smallest input values, but it is not an absolute error. The figure 7 shows the regularity of the SHA output error independently of the input signal amplitude which is easily corrected with an auxiliary input.

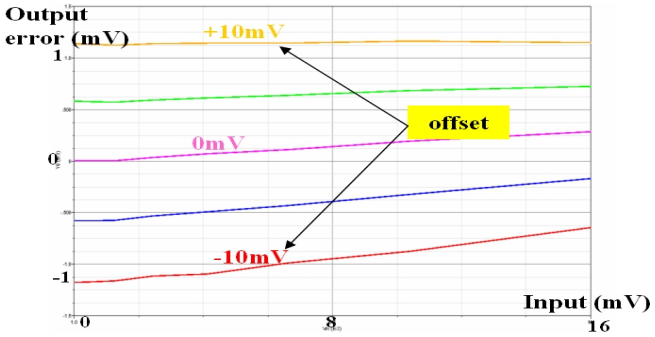

Figure 7: SHA output error according to the input signal, with the OTA offset as a second parameter

2) *Compensation of the charge injection offset:*

The charge injection offset is one of the most redundant problems of the switched capacitor architectures. When the switches go to the "OFF" position, the charges coming from the transistor channels will create an offset which is critical here since the capacitors are very small. This offset is controlled using "non overlapping 4 phase clocks" which are not detailed in the figure 3 scheme for ease of read.

3) *Compensation of the pixel common mode voltage fluctuation:*

The positive and the negative branches of the SHA scheme are perfectly symmetric and the amplifier inputs are floating. This feature leads the cancellation of the common mode voltage fluctuation effect. Figure 8 shows the SHA linearity when the common mode voltage varies from -50 mV up to +50 mV.

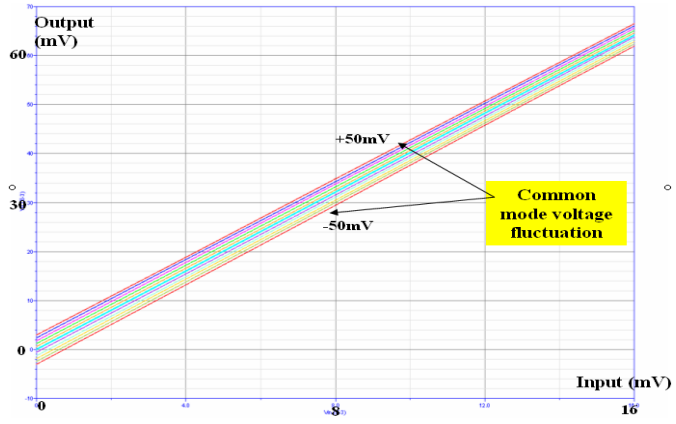

Figure 8: SHA linearity according to the common mode voltage fluctuation

III. THE PIPELINE A/D CONVERTER

Double sampling switched capacitor architecture is used in this design. This technique consists of sharing the active components between two adjacent ADC channels.

1) 2.5 bit pipelined stage:

Figure 9 illustrates the implementation of a 2.5 bit pipeline stage. The A/D block consists of six comparators. The D/A conversion, subtraction, amplification, and S/H functions are performed by a switched capacitor circuit with a resolution of 2.5 bit per stage and an interstage gain of 4. Hence the transfer function of this stage is Vs = 4*Vin - 3* $Vref_i$ where $Vref_i$ are the reference voltages selected by the DAC depending on the sub-ADC output code (b2b1b0).

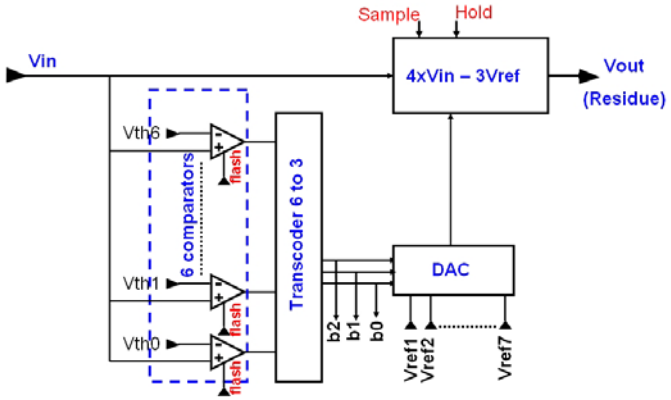

Figure 9: Bloc diagram of a 2.5bit pipelined stage.

The transfer function for a 2.5 bit stage is shown in figure 10. The expression "2.5 bit" is used to point out that only 7 combinations out of the 8 are acceptable for the output codes. The (1, 1, 1) code is avoided, thereby the interstage amplifier should not saturate and this leaves room for the digital error correction.

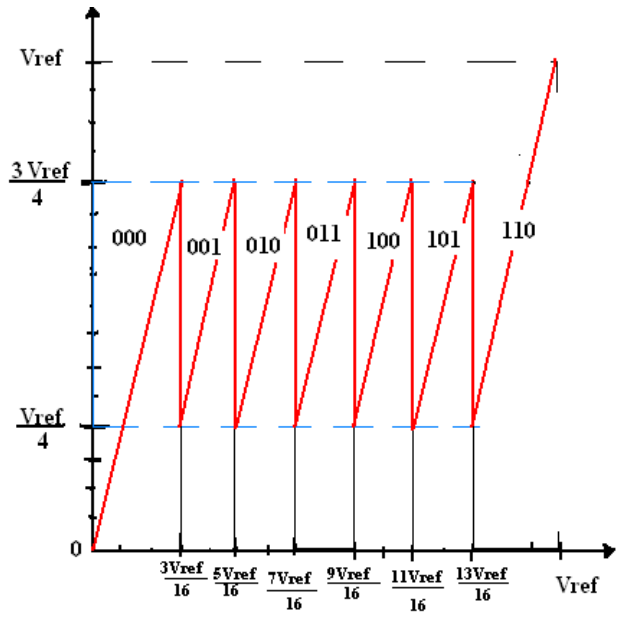

Figure 10: 2.5 bit residue transfer curve.

The maximum comparator offset value tolerated is Vref/16 = ±4 mV. Vref is the full range dynamic of this converter (Vref = 64 mV). A simplified schematic of the comparator is given in figure 11. It consists of a low gain and low offset differential preamplifier followed by a latched folded cascode comparator [9].

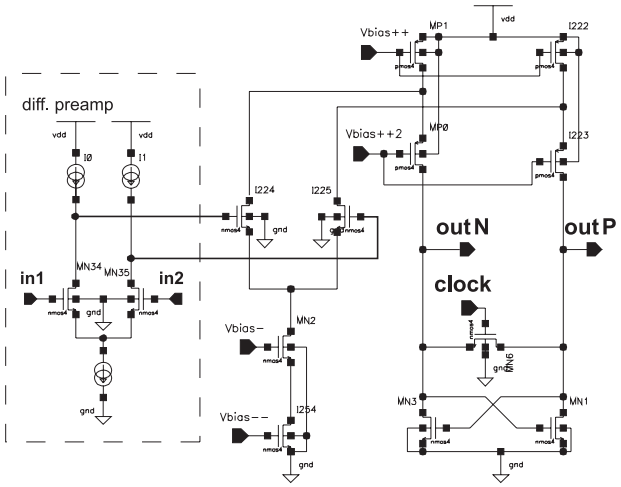

Figure 11: Simplified comparator scheme.

The residue transfer curve is obtained by a precise multiplier sample and hold switched capacitor circuit shown in figure 12.

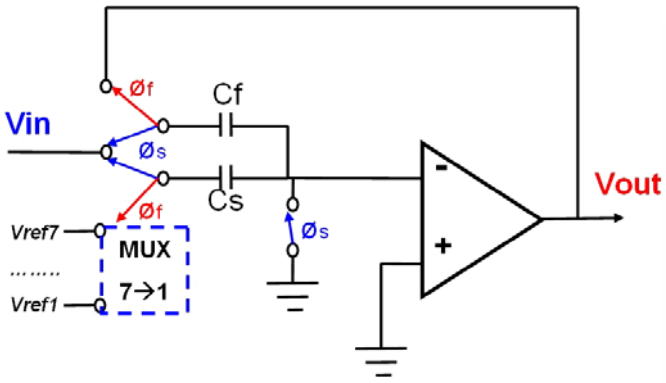

Figure 12: The switched capacitor multiplier sample and hold scheme

The incoming signal is sampled during phase "$ø_s$". It is amplified by charge redistribution during phase "$ø_f$". During this amplification phase, the bottom plate of the sampling capacitor (Cs) is connected to a reference voltage $Vref_i$ which will be subtracted from the amplified signal. The residue resulting from this operation is transmitted to the next stage. The value for $Vref_i$ is respectively 0, Vref/6, Vref/3, Vref/2, 2Vref/3, 5Vref/6, or Vref depending on the comparators outputs (see figure 9). Vref is the dynamic range of the converter, with reference to the virtual ground.

2) Double sampling:

In the final design of the MAPS, at the bottom of each pixel column of the matrix there will be an ADC. So, the ADCs are disposed in parallel. This feature can be exploited in the double sampling architecture.

The property of the successive ADC stages working in opposite clock phases can be exploited by sharing the operational amplifier, the comparators and the all the logic part between two parallel component ADCs. This approach uses the well known double-sampling concept of switched capacitors circuits. By using double-sampling, the equivalent sampling rate is doubled, but still the power dissipation remains almost the same as for an ADC having traditional single sampled pipeline stages with a half sample rate. The surface is reduced by 40%. In contrast, the complexity of the pipeline stage is increased and more clock signals with different phases are needed.

Scheme of the double sampling multiplying D/A converter is shown in figure 13. The capacitors of two parallel channels working on opposite clock phases share the same amplifier. Due to the very low incoming signal, each ADC channel has its own SHA stage. While the pipeline1 samples the Vin1 signal onto the Cs and Cf capacitors independently of the amplifier, the pipeline2 switches to the amplification phase.

Two important side effects are caused by the amplifier sharing. First, the amplifier load capacitance is increased and affects its bandwidth. Second, the amplifier input offset is never reset; this can be tolerated by an adequate amplifier open loop DC-gain. The second one is very critical in this design because of the non differential architecture used here, and thereby no symmetric compensation is possible.

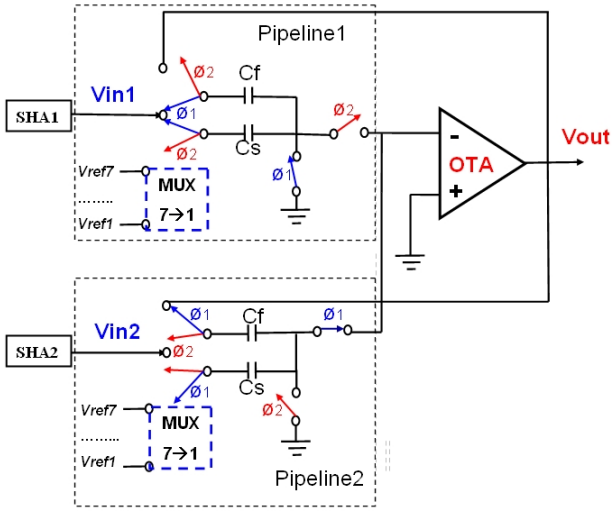

Figure 13: A double sampling principle scheme

3) Performance limitations:

The conversion speed is limited by the settling time of the operational amplifier used in the S/H circuits. The use of double sampling and parallelism introduces several limitations traduced by errors. These errors include offsets, gain and timing mismatches of the parallel channels. In this design the threshold and reference voltages are generated out side of the prototype circuit. The large number of pipeline stages using the common reference voltages increases the capacitive load in the reference nodes. To guarantee that the reference does not limit the settling speed, its output impedance has to be very low (couple of tens of ohms).

A prototype has been designed in a CMOS 0.35µ process from Austria Micro System. It includes 4 channels of the double sampling ADC described. A photo of the chip is shown in figure 14. The dimensions of one full channel including the sample & hold amplifier stage are 80µm*0.9mm. One may notice also that the surface occupied by the first stage (SHA) is about 1/4 of the full channel.

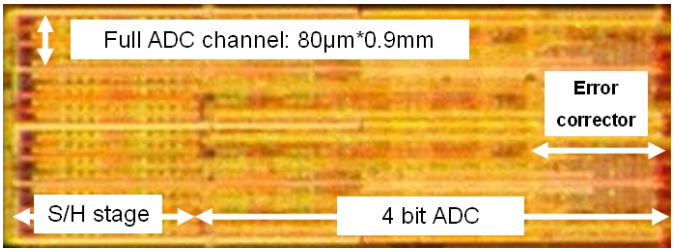

Figure 14: Photo of the Prototype with 4 ADC channels

IV. Testing Results

The circuit has been tested successfully at 50 MHz; double-sampling concept is taken in count. The full double sampling ADC dimensions are 80µm*0.9mm. Its power dissipation at 3.3 V power supply is 2.6 mW this corresponds to the consumption of 4 pixel columns ADCs.

The signal to noise ratio (SNR) of the ADC can be obtained by the fast Fourier transform (FFT). In figure 15 is shown the FFT spectrum for a 1 MHz sine wave input signal. The dynamic range is in the order of 20dB.

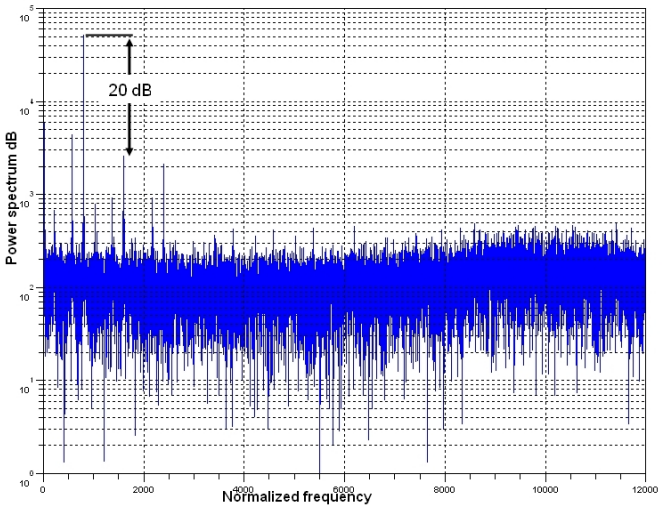

Figure 15: FFT spectrum

For the next ILC experiment, the beam duty cycle will be very low (~1%). It is therefore worthy to switch on the analog part of the circuit only when used, thus making the total power dissipation directly proportional to the beam duty cycle. This circuit includes such fast and efficient “power ON” capability. The analog bias settling result is given in figure 16. This bias pulsing circuit has already been integrated

and tested in our precedent version of ADC published last year (San Diego IEEE NSS 2006).

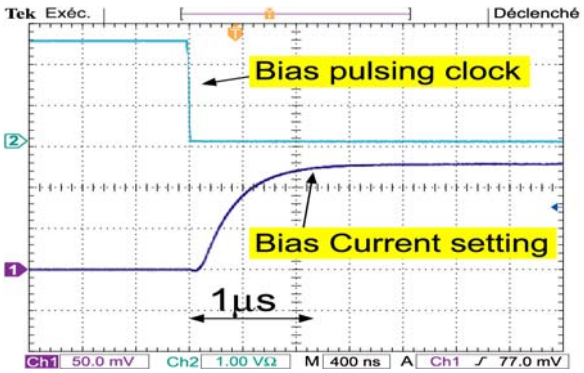

Figure 16: Analog bias switching results

From the falling edge of a pulsing clock, the bias current is settled after only 1µs. In the standby idle mode (pulsing clock at high level), the full analog part of the converter is switched OFF and the analog power dissipation is reduced to a ratio better than 1/1000.

V. Conclusion

For Monolithic active pixel sensors, a 4bit 50 MHz double-sampling A/D converter has been fabricated in CMOS technology. It achieves 20dB of dynamic range with a typical DC dissipation of 2,6mW per 4 pixel columns; this corresponds to 0.6 mW/column. It is designed in perspective of the next linear collider (ILC). The full ADC includes an amplification sample and hold stage. A 2.5 bit/stage architecture is used for the converter in a non differential configuration. The size for one channel layout is 80µm*0.9mm. A very efficient fast power pulsing is integrated with this circuit to reduce the total DC power dissipation according to the beam low duty cycle.

VI. Acknowledgment

We would thank Marc Winter, Christine Hu, Isabelle Valin, and Claude Colledani from the IPHC / IN2P3 laboratory in Strasbourg for this useful collaboration with them and many discussions on their MAPS design constraints.

VII. References

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