MAPS read-out electronics for Vertex Detectors (ILC)

A low power and low signal 4 bit 50 MS/s double sampling pipelined ADC

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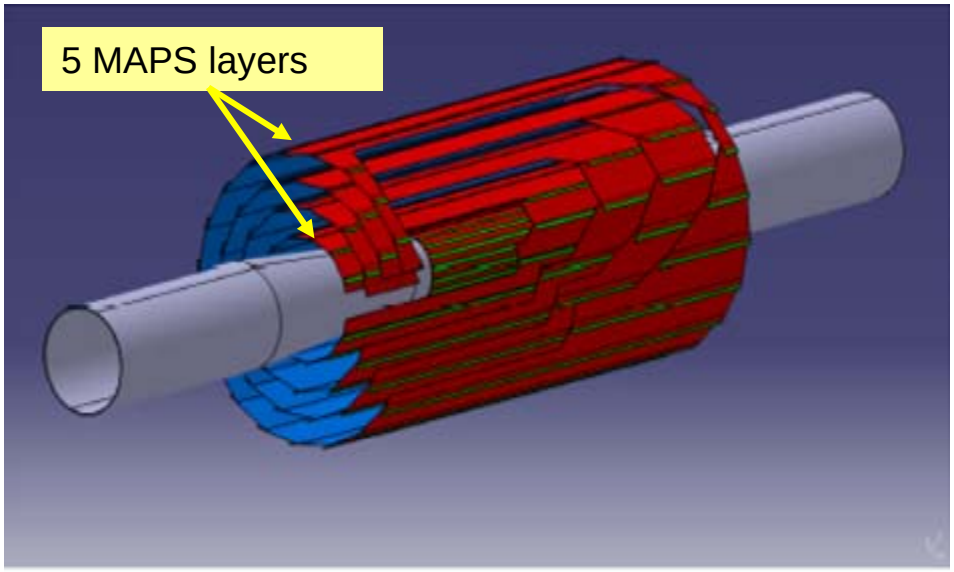
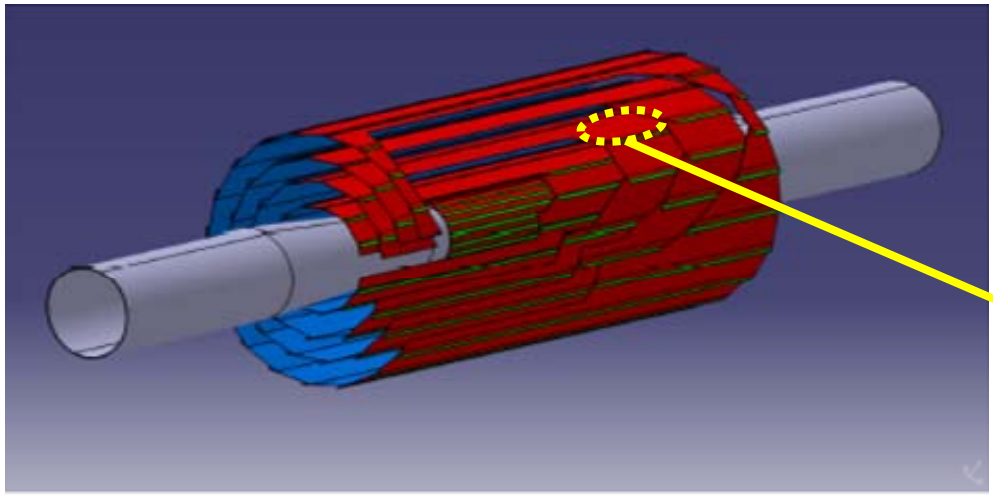
CMOS Vertex Detector Characteristics

- **Geometry: 5 cylindrical layers (R=15-60mm)**
- **Read-out time: 25 µs in L0, 50 µs in L1, ≤ 200µs in L2, L3, L4**

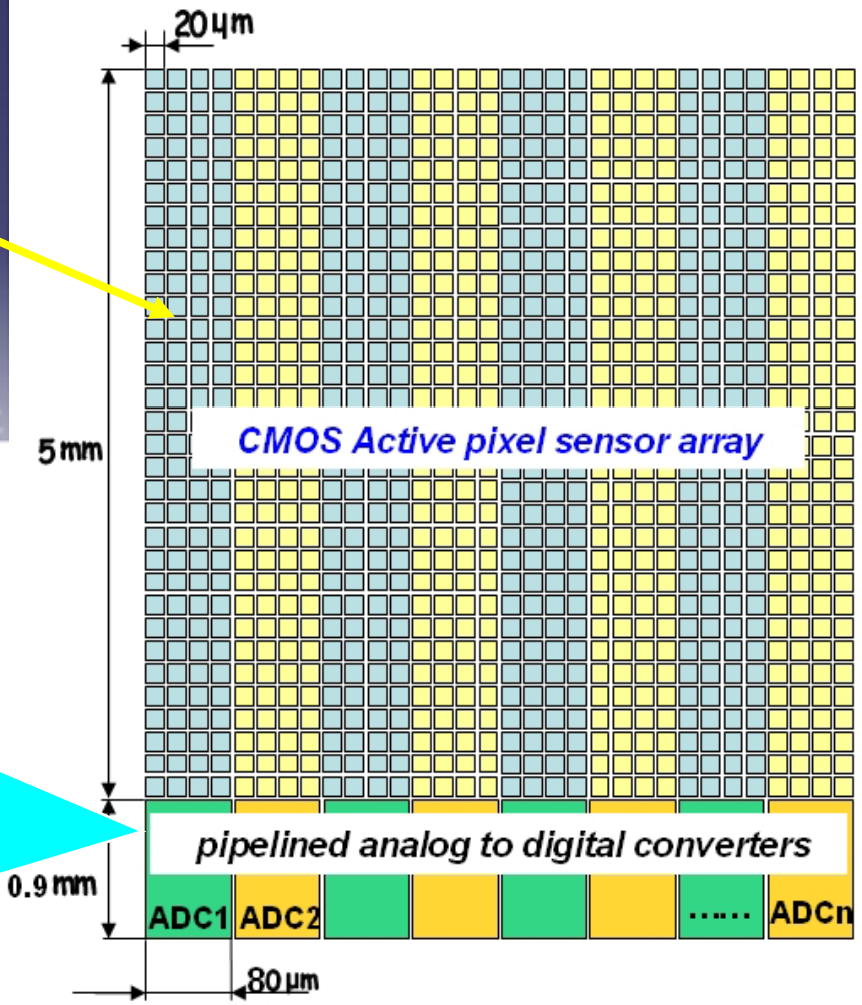
Layer	Radius (mm)	Pitch (μm)	$t_{r.o.}$ (μs)	N_{lad}	N_{pix} (10^6)	P^{inst}_{diss} (W)	P^{mean}_{diss} (W)
L0	15	20	25	20	25	<100	<5
L1	25	25	50	26	65	<130	<7
L2	37	30	<200	24	75	<100	<5
L3	48	35	<200	32	70	<110	<6
L4	60	40	<200	40	70	<125	<6
Total				142	305	<565	<29



MAPS array + read-out for ILC vertex detector



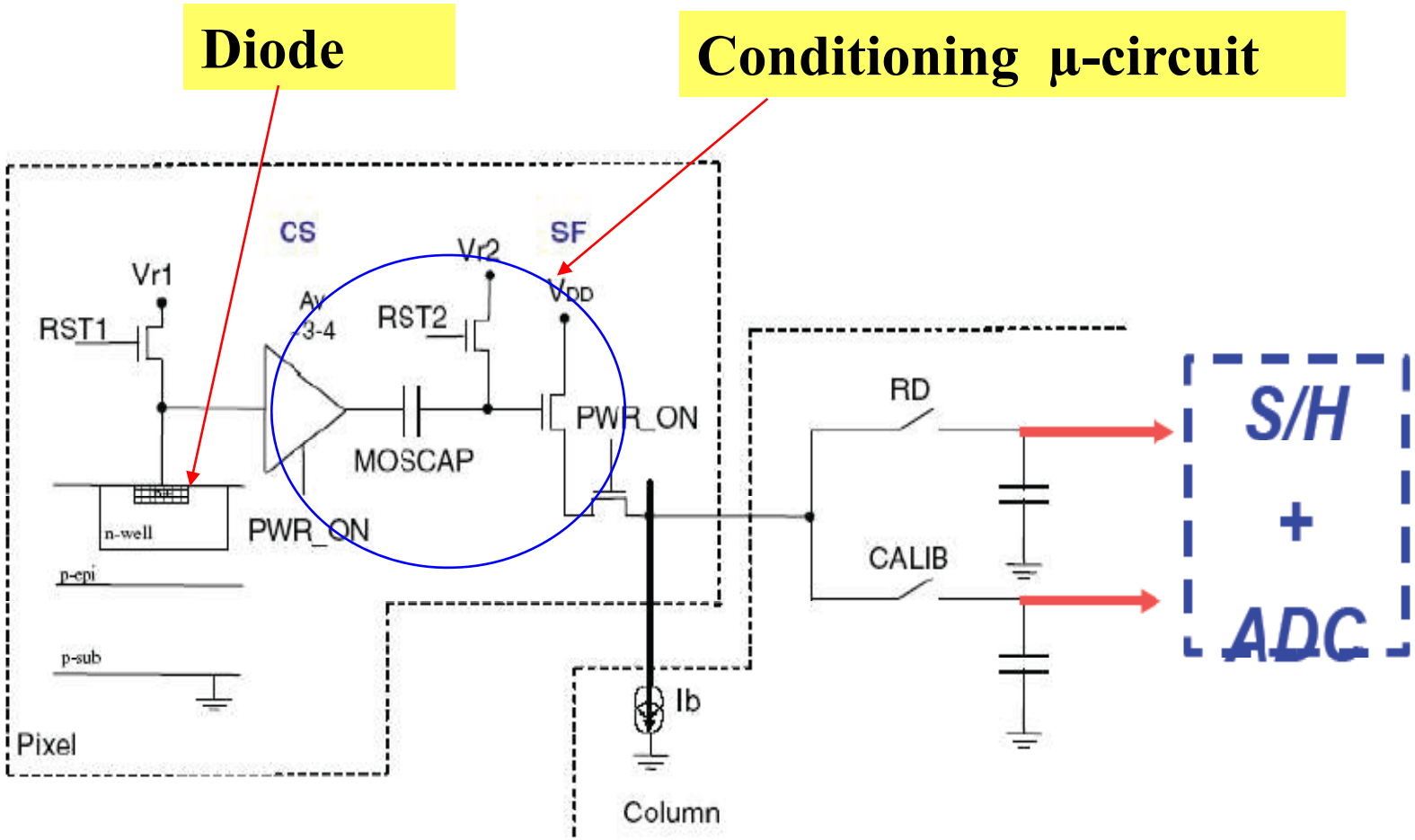
Collaboration LPSC-IPHC



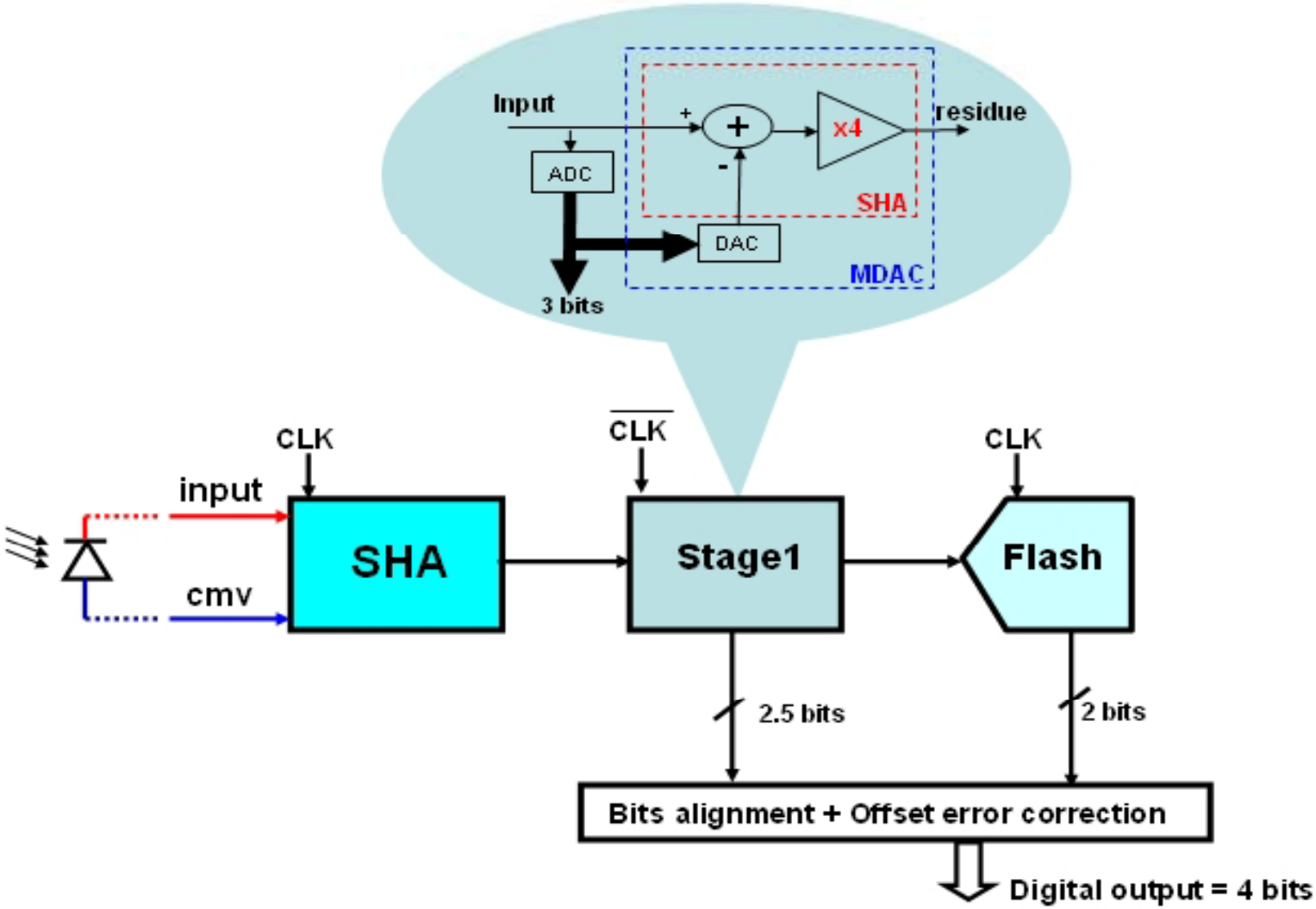
ADC design requirements:

- Small LSB →1mV
- Narrow column wide →20 µm
- Length <1mm
- Low power →0.5mW
- High speed >10MHz/column

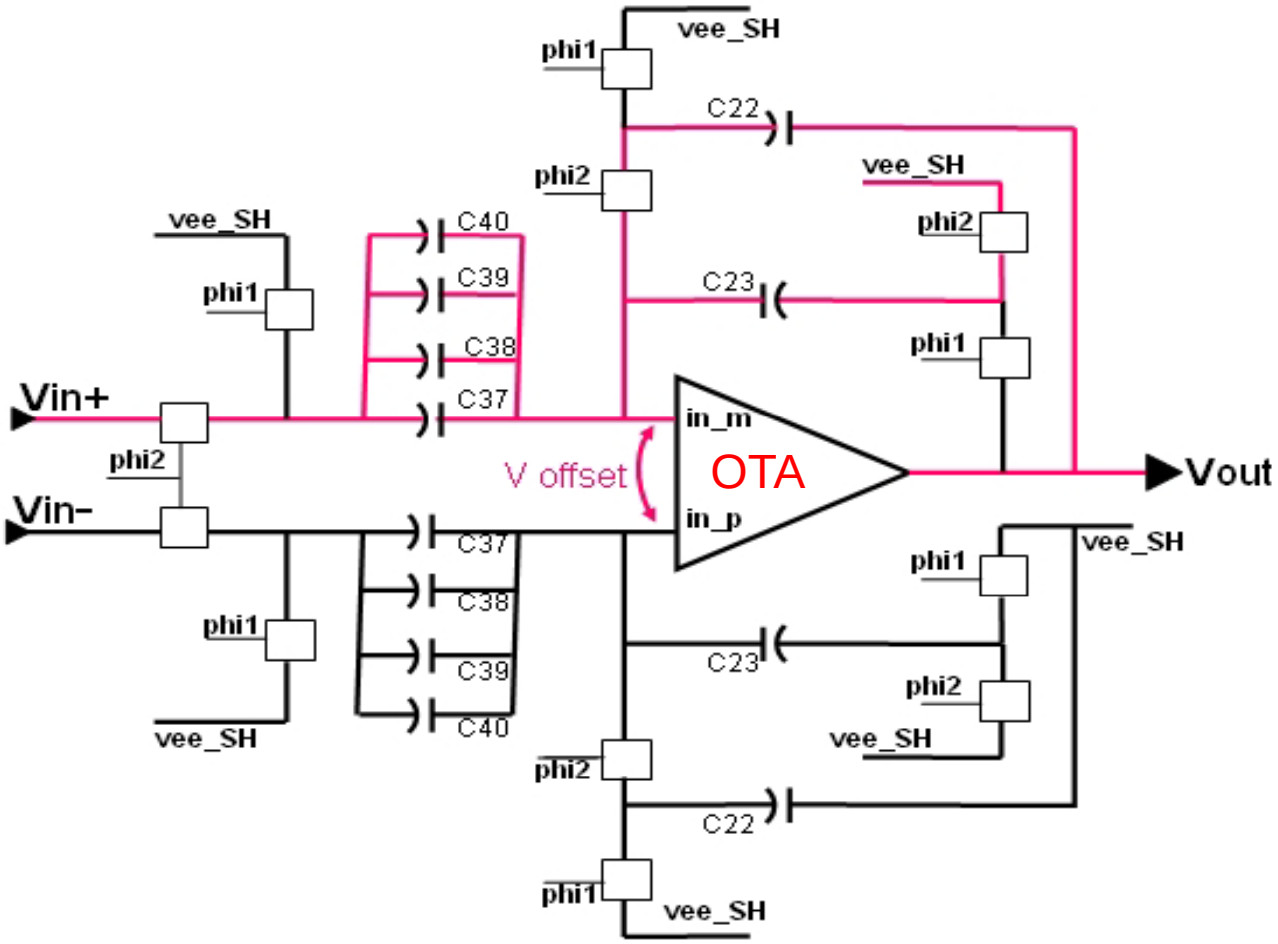
The Active Pixel Architecture



General block diagram of a 4bit pipelined converter



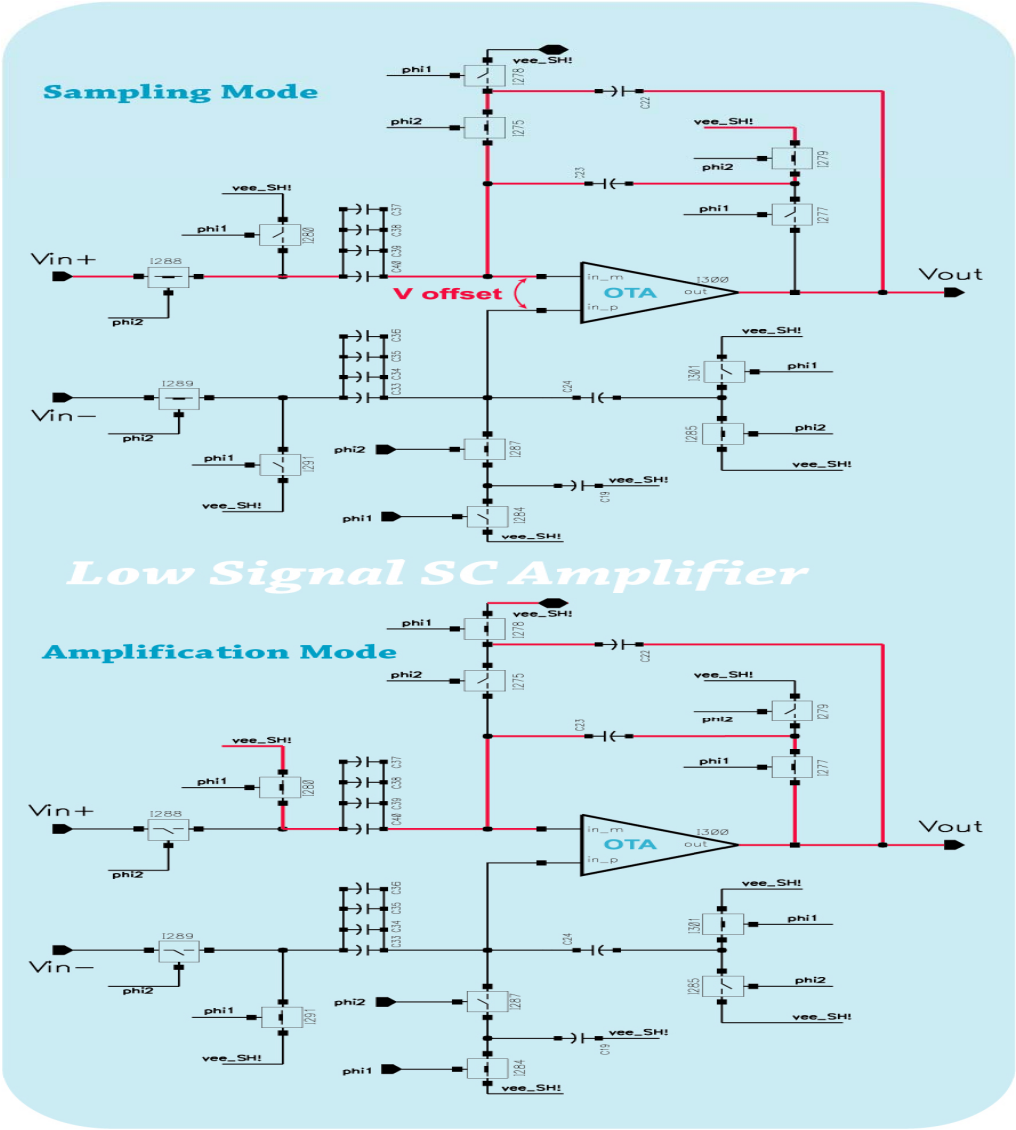
Sample & Hold Amplifier scheme (1)



- Pseudo differential switched capacitor architecture, no need to common mode control circuit:
- Input common mode fluctuation Rejection
- OTA Offset effect cancellation
- Amplification by 4 of the input signal:

•Comparator constraints relaxation => Low consumption

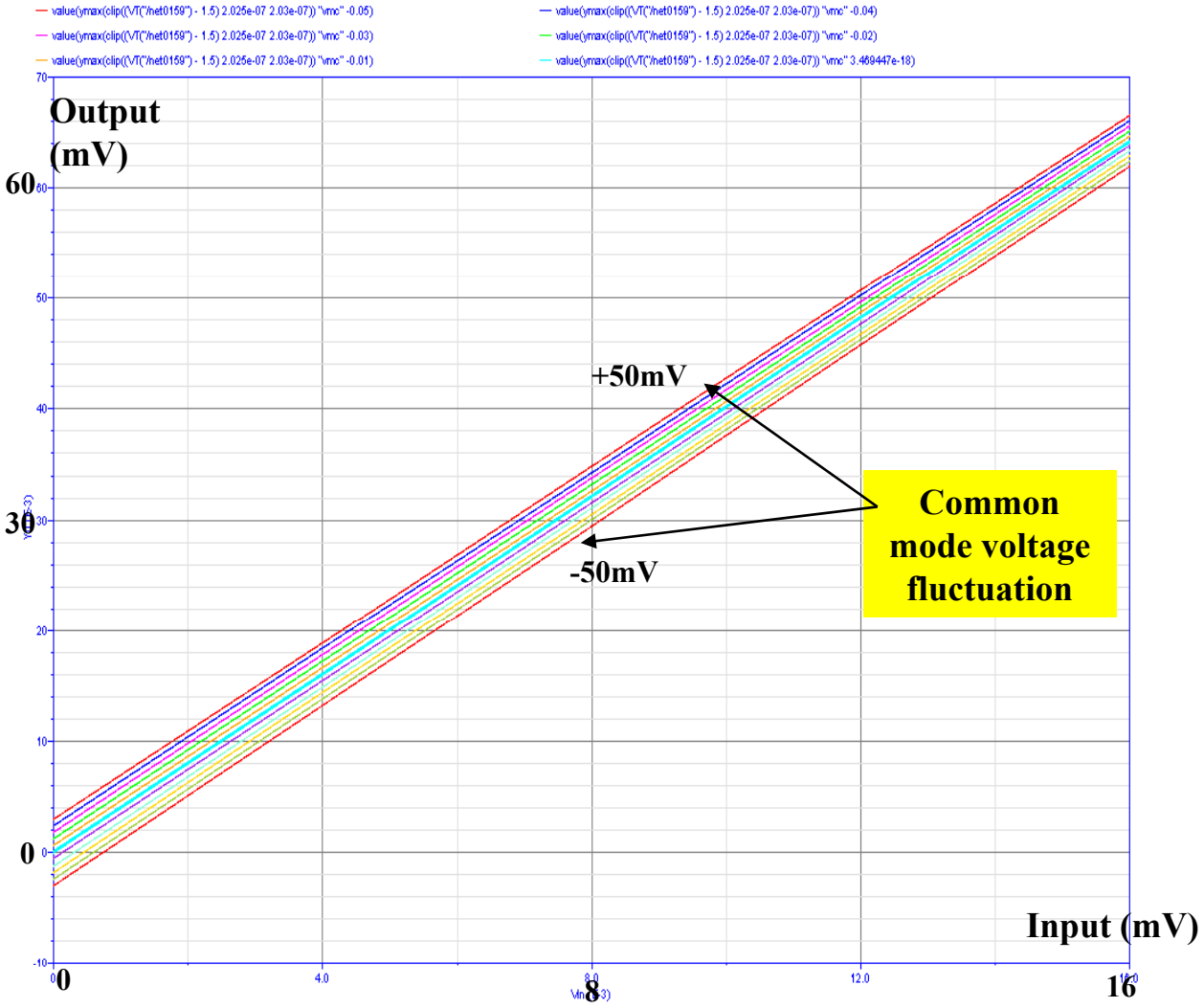
Sampling and amplification phases (2)



- **SAMPLING**
  - Input signal stored onto the sampling capacitors
  - Offset memorizing
  - Vout(t) = Vout(t-1), non resetting effect

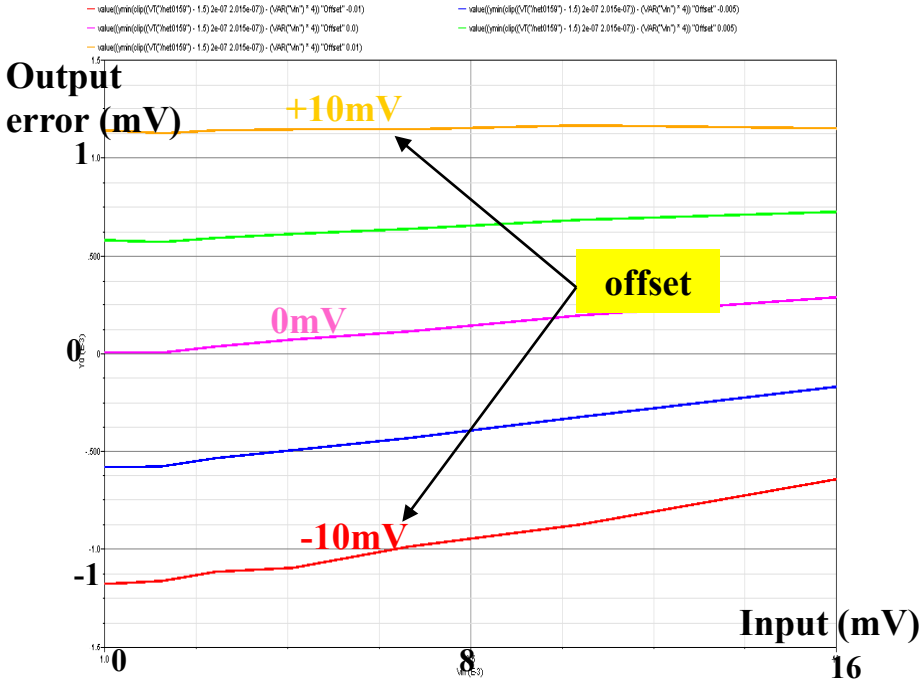
- **AMPLIFICATION**
  - Amplification by the capacitor ratio
  - Cancellation of the offset
  - Memorizing of Vout

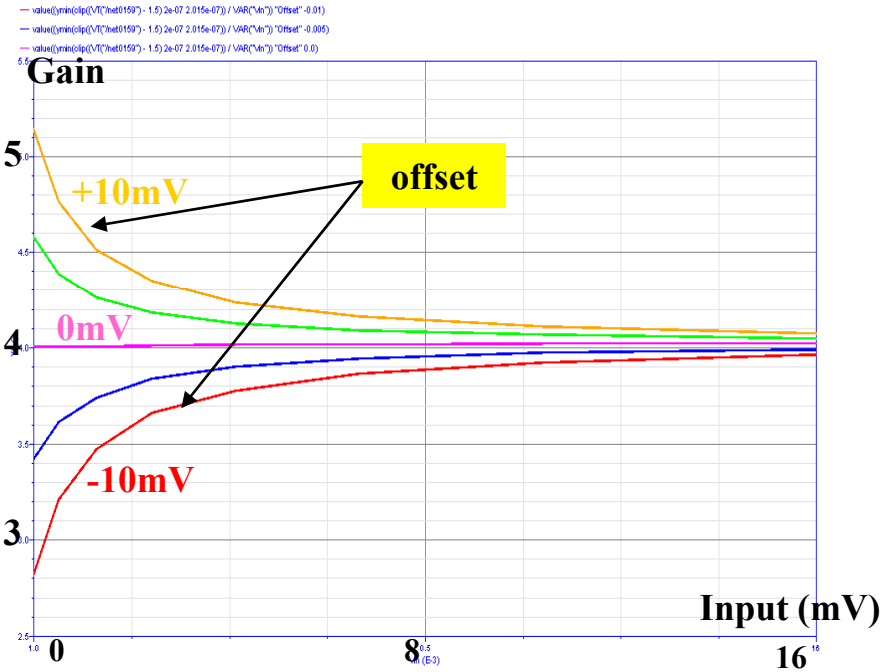
Rejection of the Input signal Common mode dispersion



•Regularity of the error on SHA output according to the input signal for different input common mode voltages

Input Offset rejection

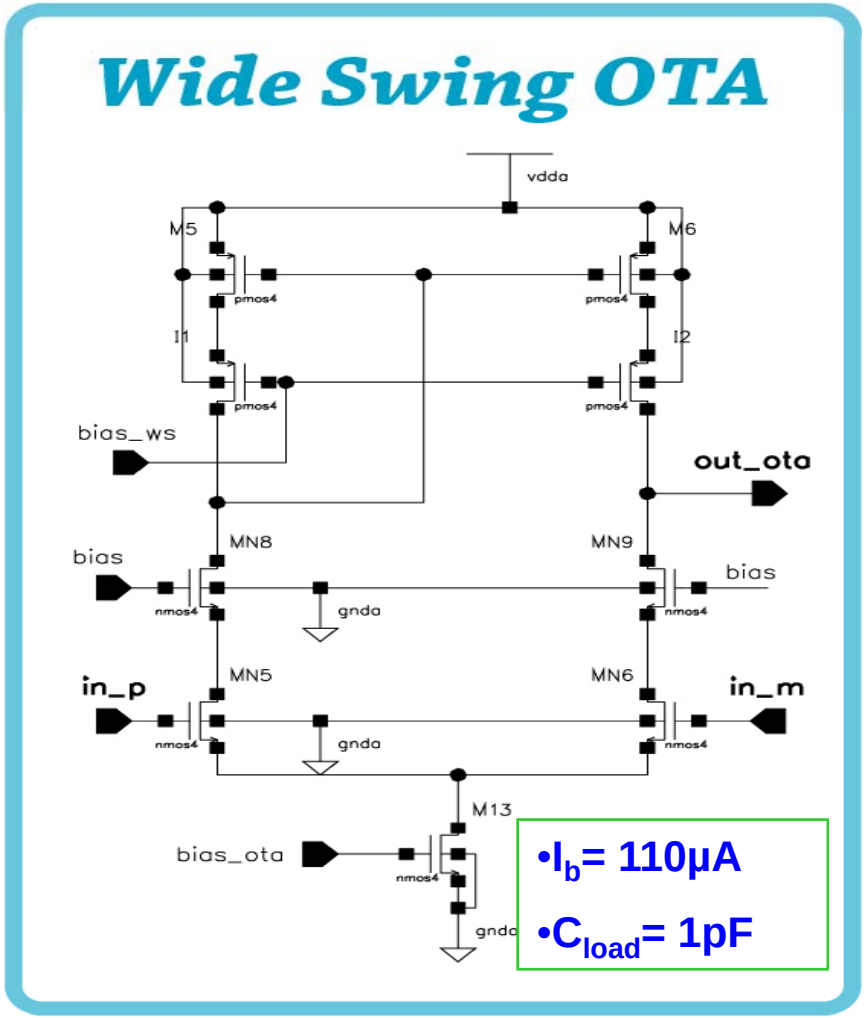


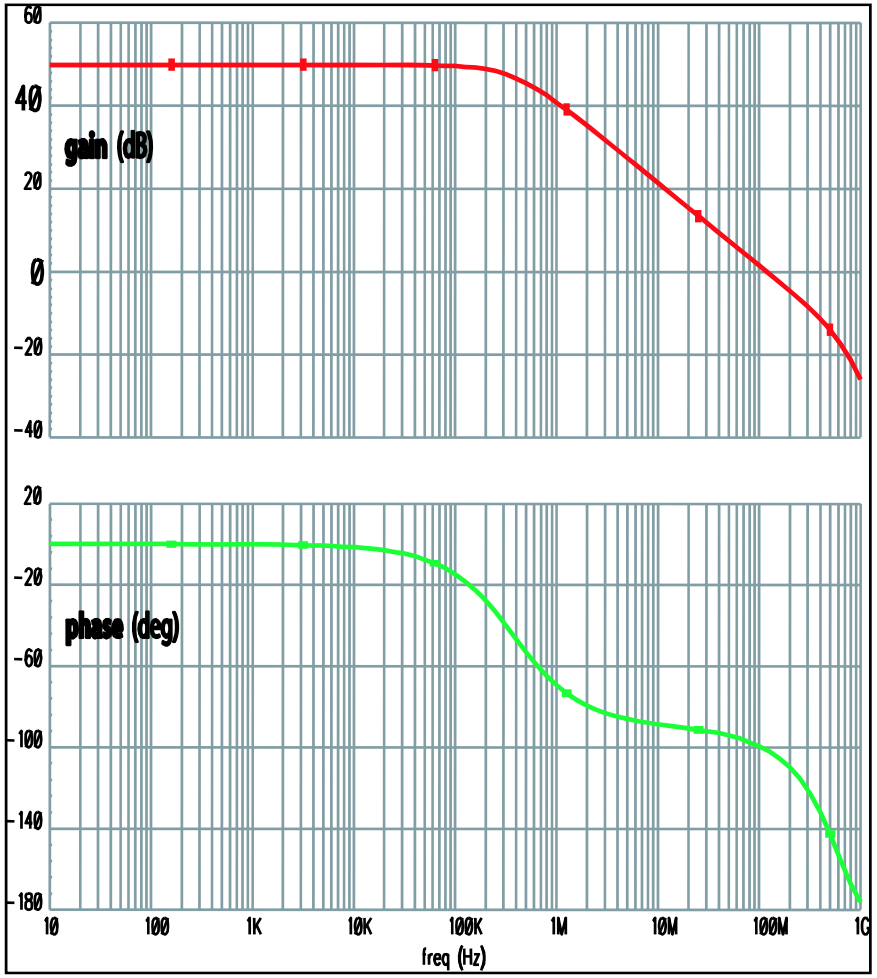


•Regularity or the error on SHA output according to the input signal for different OTA offsets

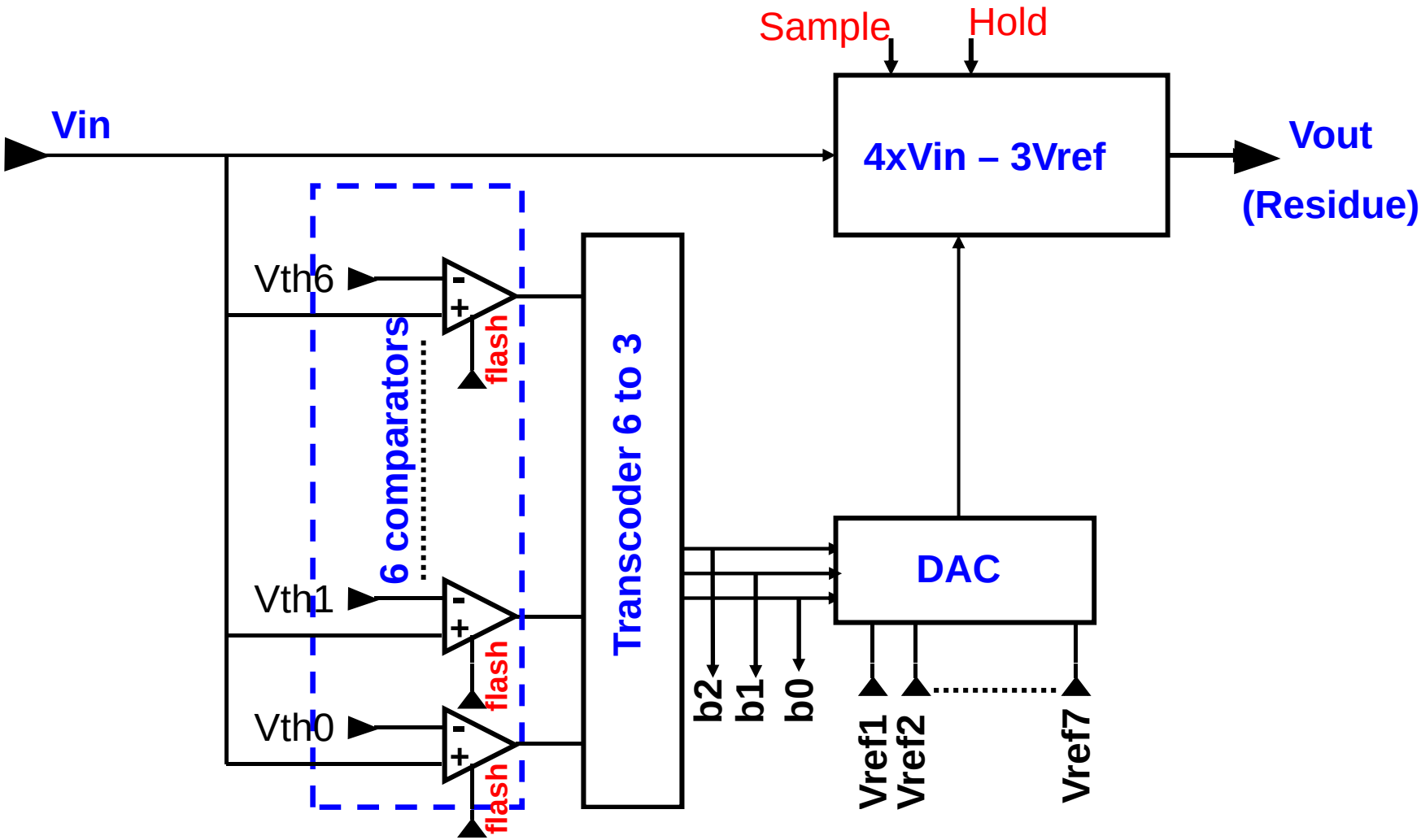
•The amplification factor still close to its optimal value (4) according to input signal when the offset voltage varies from -10mV to +10 mV

The Operational Amplifier architecture

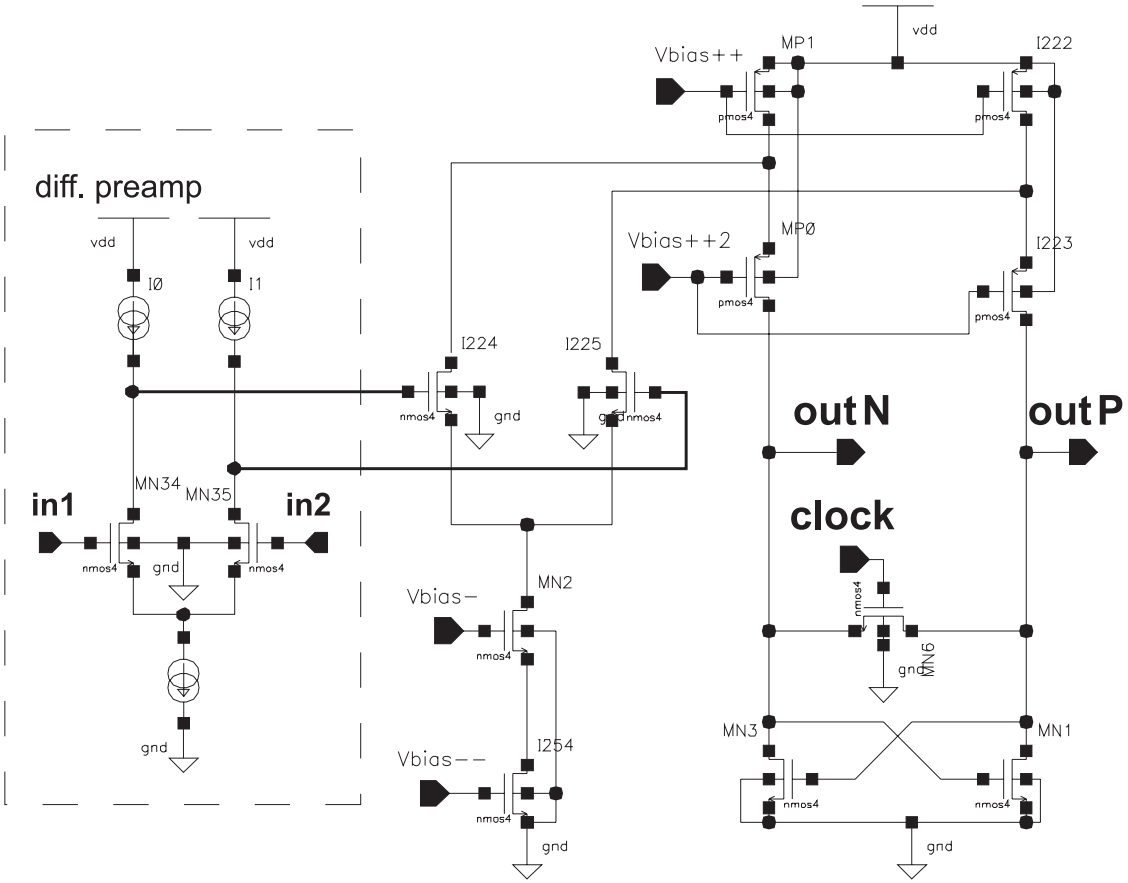




A 2.5 bit pipelined ADC architecture

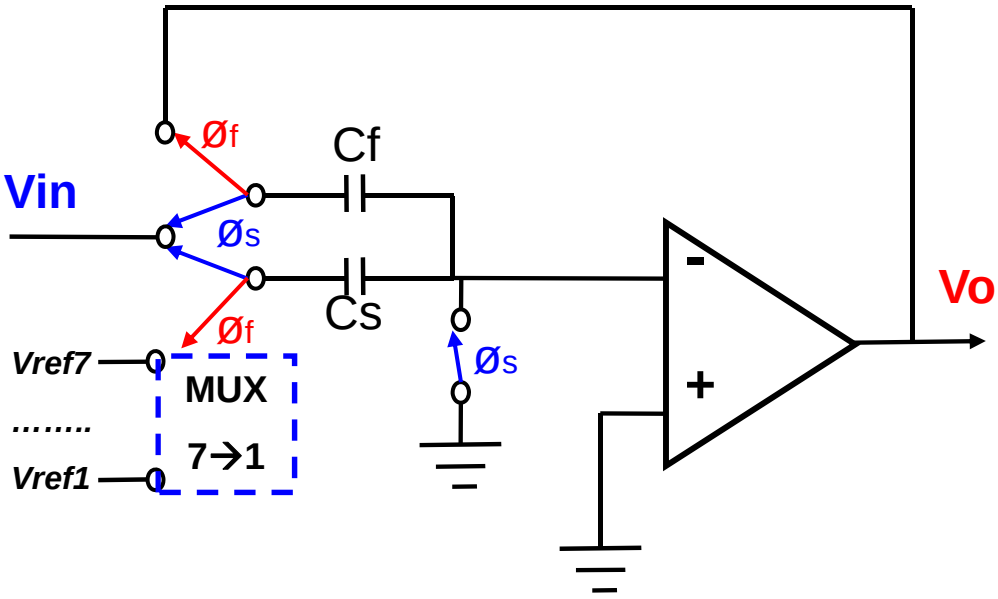


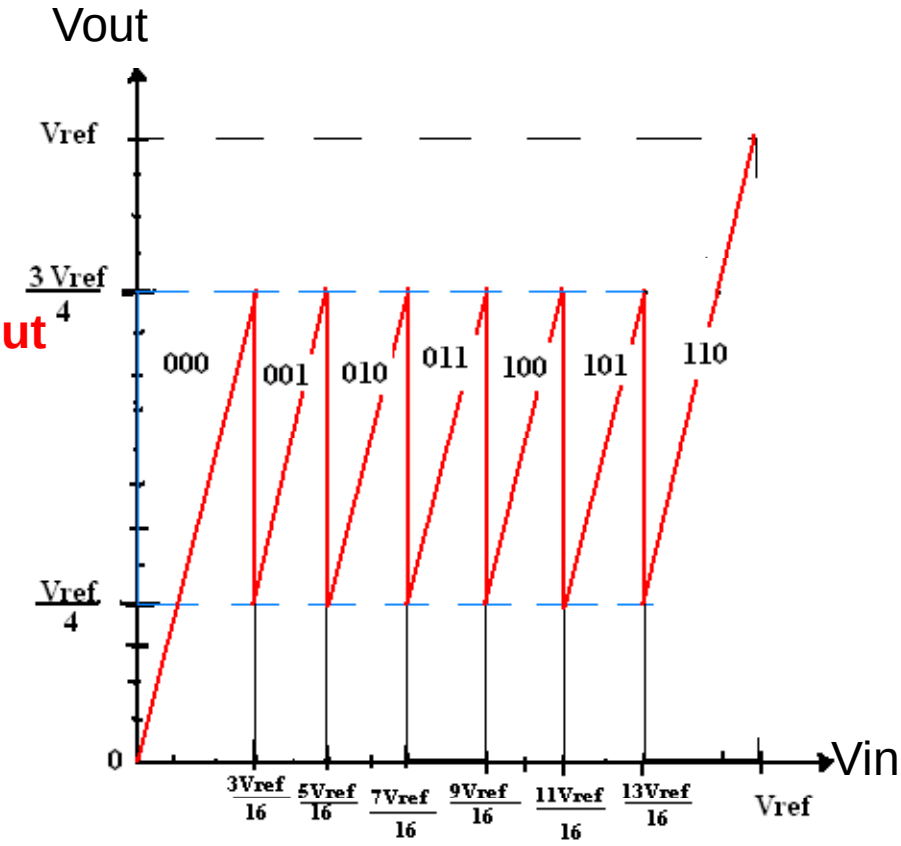
High speed comparator scheme



- composed of Three stages
  - •Preamplifier: gain 10
  - • folded cascode stage
  - •and flash stage
- Low offset (mc simulations: worse case ±5 mV)

A 2.5 bit MDAC Circuit implementation



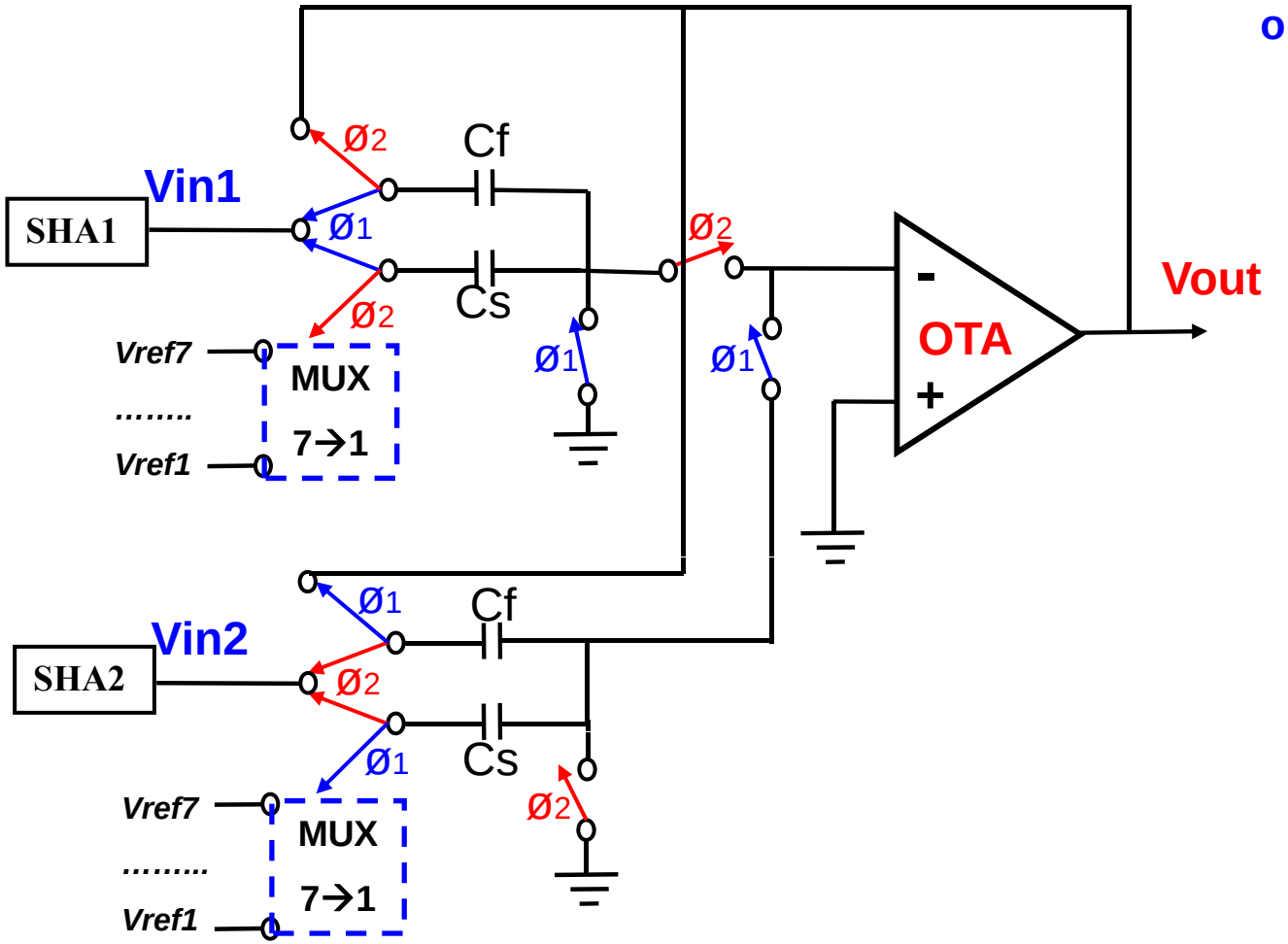


$$Vout = \left(1 + \frac{C_s}{C_f}\right) Vin + \left(\frac{C_s}{C_f}\right) Vrefi$$

Cs = 3Cf= 3*127 fF

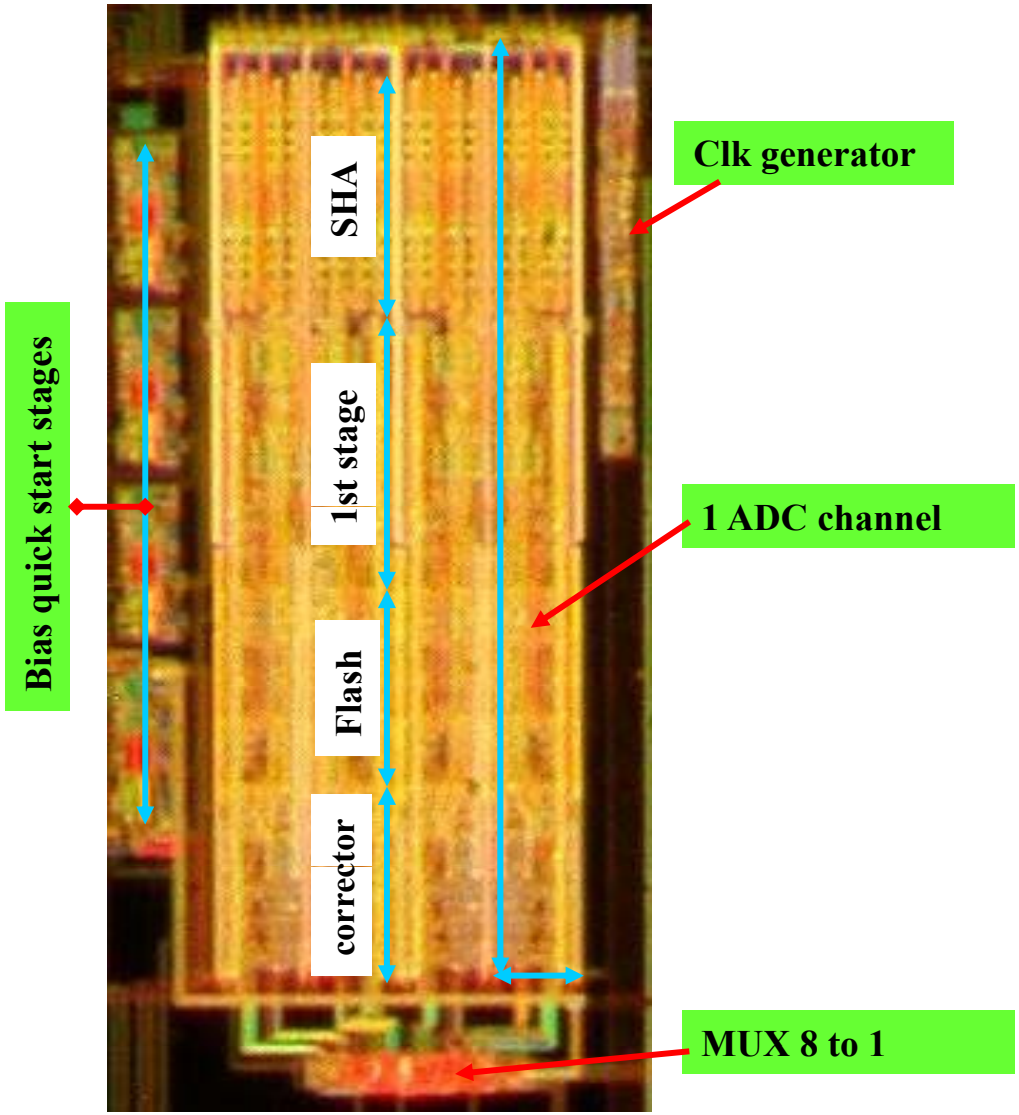
Tolerated Offset = ±Vref /16

Double sampling principle



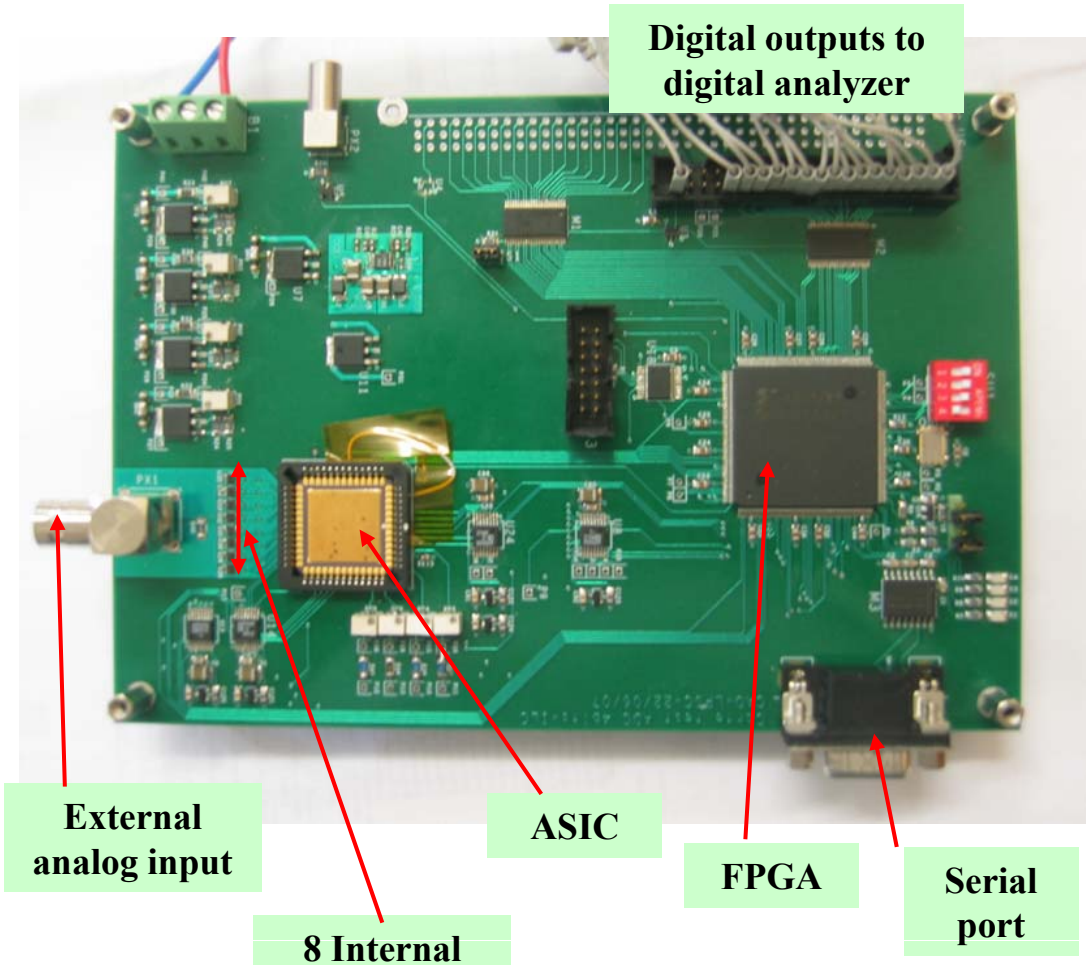
- **Stages of each ADC channel work in opposite phases, so:**
  - ***The OTA is shared between two adjacent channels***
  - ***All digital part and comparators are shared also***
  - ***Frequency is doubled for the same consumption***
  - ***The number of switches and clock signals is increased***

Prototype of 8 double sampling ADC channels



- 8 Double sampling 4bits (2 x 25 MHz) ADCs
- Dimensions of an ADC channel corresponding to one pixel column : 900µm x 20µm

Test card

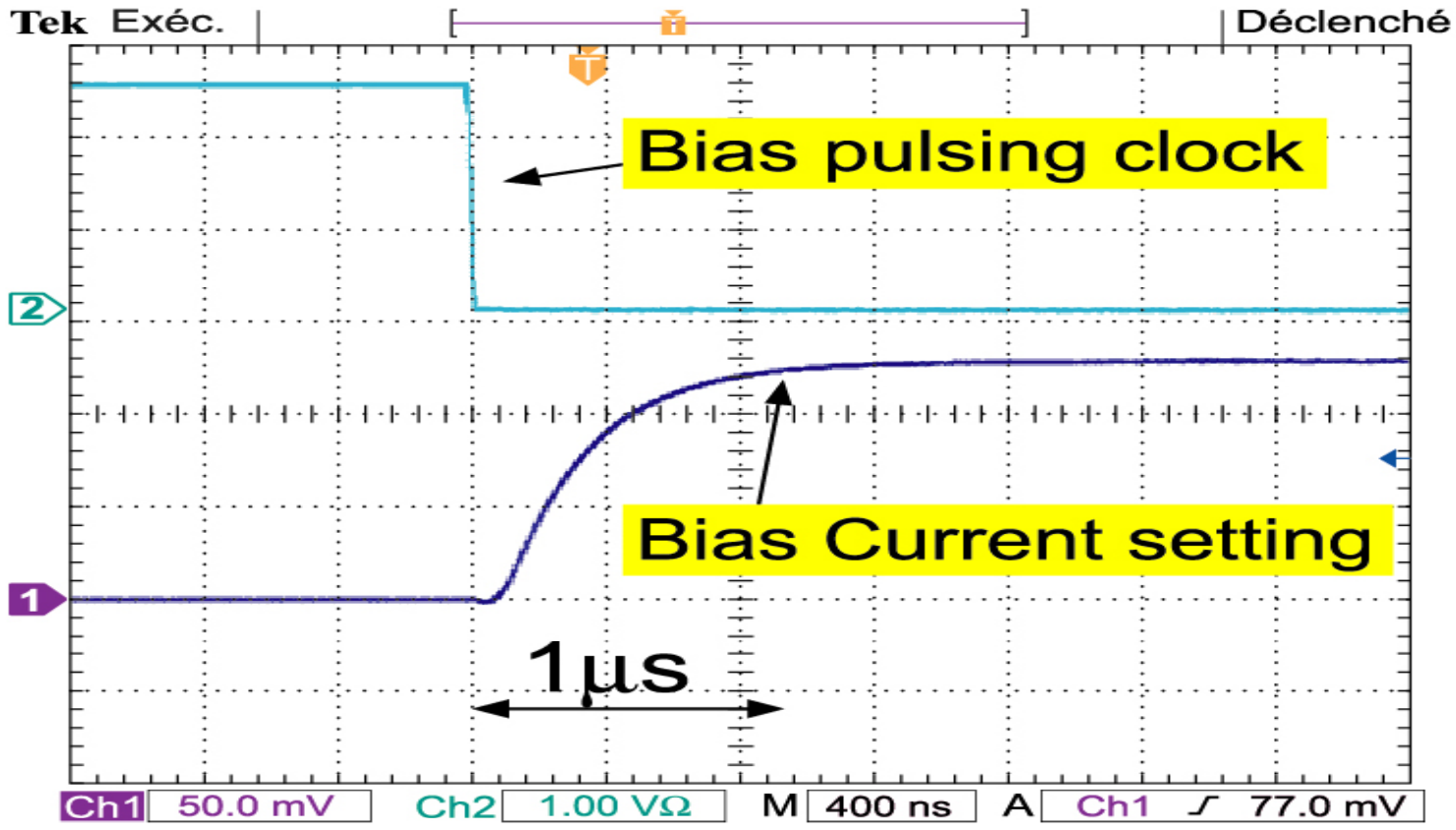


- reference and threshold voltages are generated by 16 bit DACs commanded by FPGA Xilinx program
- This method offers good flexibility, but DACs present an output impedance non negligible.
- Solution: follow the DACs by amplification stages.
- Still measuring FFT, INL and DNL of the ADC

Analog bias fast switching results

All the analog part is switched off in less than 1µs

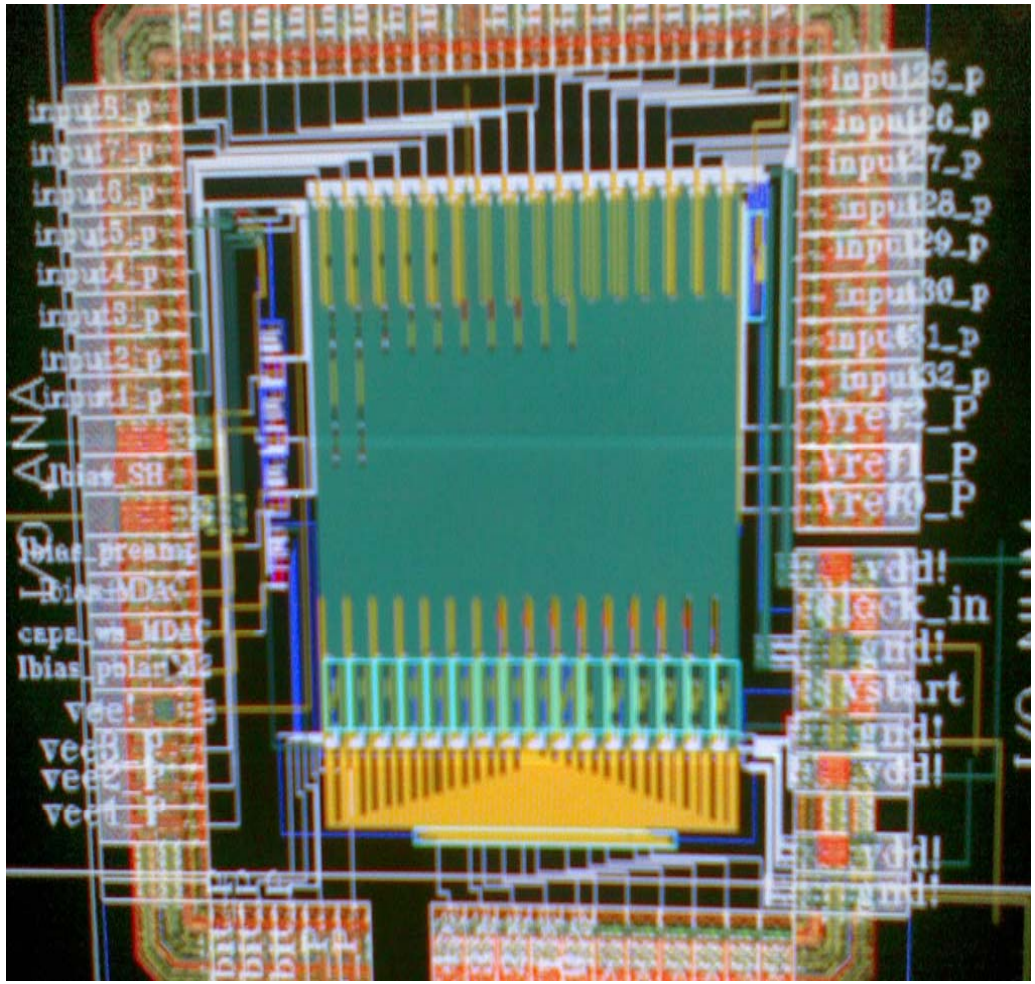
Efficiency : consumption is reduced to less than 1/1000



performance table of different ADC versions

	ADC 5bits 2005	ADC 5bits 2006	ADC 4bits March 2007	ADC 5bits Jul 2007
Frequency	17 MHz	25 MHz	25 MHz	25 MHz
Dimensions	43µm*1500µm	43µm*1500µm	40µm*900µm	40µm*1300µm
Dissipation @3.3V	1.7 mW	1.7 mW	1.18 mW	0.9mW
Dissipation @2V	1.04mW	1.04mW	0.72mW simulation	0.5mW simulation

Layout of the next ADC version



- Layout of 32 parallel ADCs
  - Supply voltage: 2V
  - Sampling rate :2 x 25 MHz
    (double sampling ADC)
  - Very low power

- Aim:
  - study of Cross talk between channels

Conclusion

- Still optimizing ADCs :
  - *Design of a new low voltage (2V supply voltage) ADC.*
  - *Cross talk correction between ADC channels*

- Second step of work:
  - ADC-pixel interface study and design
  - Preparation of the ADC-PIXEL integration on the same Wafer.

THANK YOU FOR YOUR ATTENTION!