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a low power and low signal 4 bit 50MS/s double sampling pipelined ADC for Monolithic Active Pixels Sensor

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For CMOS monolithic active pixels sensor readout, we developed a 4 bit very low power analog to digital converter using a double sampling pipelined architecture. The converter consists of a non-resetting sample and hold stage followed by a 2.5 bit sub-ADC and a 2 bit flash. This prototype consists of 4 ADC double-channels; each one is sampling at 50MS/s and dissipates only 2.3mW at 3.3V supply voltage. It includes a fast power down input. The size for the layout is 80µm*0.9mm. This corresponds to the pitch of 4 pixel columns, each one is 20µm wide.

Summary

SUMMARY:
CMOS Monolithic Active Pixel Sensors (MAPS) provide many well-known advantages for vertex detectors, high precision beam telescopes etc… Granularity, radiation tolerance, random access and high speed read-out are the most appealing characteristics. However, there are several constraints on the design of the associated readout electronics:
·The process is chosen first according to its particle detection performances.
·The minimum readable signal is very low (»1 mV).
·The layout dimensions must fit with the narrow pixel pitch.
·The power dissipation is a critical issue.
The design presented here is a 4 bit double sampling pipelined Analog to Digital Converter (ADC). According to the power dissipation and the layout size, it is an improved version in comparison with the results we published last year (San Diego IEEE NSS 2006). This design is one of the candidates to equip the pixels array designed at IPHC-Strasbourg in collaboration with DAPNIA-Saclay for the future International Linear Collider (ILC) Vertex Detector.
The converter consists of a sample and hold amplifier (SHA) stage followed by a double sampling pipelined stages.

A) The Sample and Hold Amplifier (SHA):

It amplifies the small incoming signal by 4 and compensates the amplifier's offset effect and the input common mode voltage fluctuations.
A charge redistribution architecture is used. Four non overlapping clock signals control the sampling and the hold phases. During the sampling phase, the input signal is stored onto the sampling capacitor (400 fF). During the hold phase, the charges are transferred onto the feedback hold capacitor (100 fF).

B) Double sampling pipelined ADC:

The pipeline architecture provides the best deal between speed, consumption and area required for the MAPS. A 2.5 bit pipelined stage followed by 2 bit flash stage is used in this ADC. A digital error correction stage is added to leave room for the comparators' offsets.
Two successive stages of the ADC are always in opposite clock phases. Therefore the amplifier and the comparators are shared between two adjacent parallel ADC channels. The full logic part is also shared. Due to the critical input signal, each ADC channel has its own SHA stage. By using double sampling switched capacitor method, the equivalent sampling rate is doubled, the power is reduced almost by 40% and the surface is significantly reduced compared to

the simple pipelined architecture. In contrast, the complexity of the pipelined stage is increased; more switches and more different clock phases are needed. Two important side effects are caused by sharing the amplifiers. First, the load capacitance of the amplifier is increased and that affects its bandwidth requirements. Second, the amplifier offset is never reset; this can be tolerated by an adequate amplifier open loop DC-gain.
For the ILC case, the beam duty cycle is 1/200. A bias pulsing stage is integrated in the circuit. Therefore, the analog part is switched OFF or ON in less than 1µs.
We have already designed and successfully tested two first prototypes of 5 bit simple pipelined ADC. The design presented here introduces several improvements and theses results will be presented.

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