Production and Testing of the LHCb Outer Tracker Front End Readout Electronics

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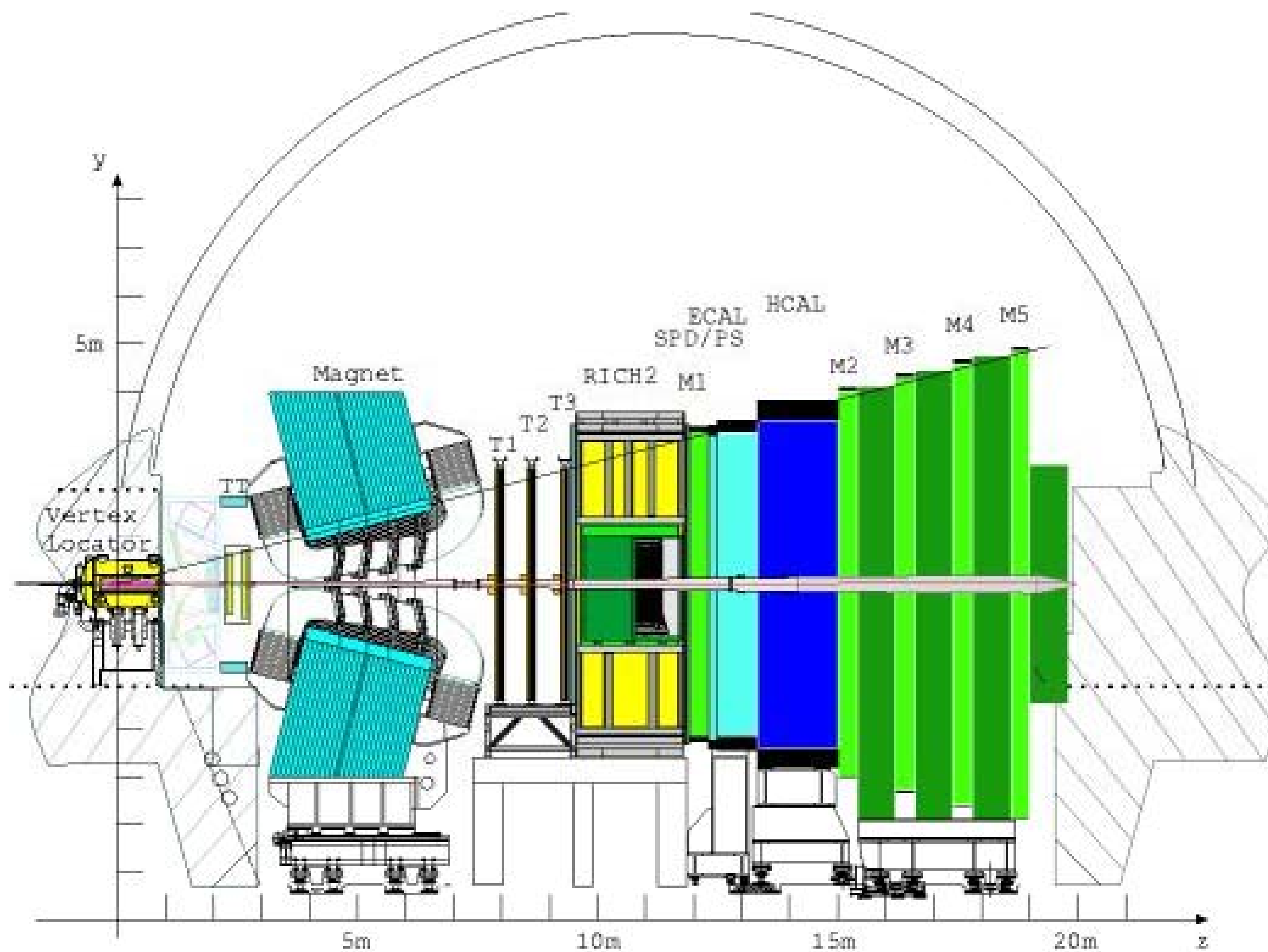
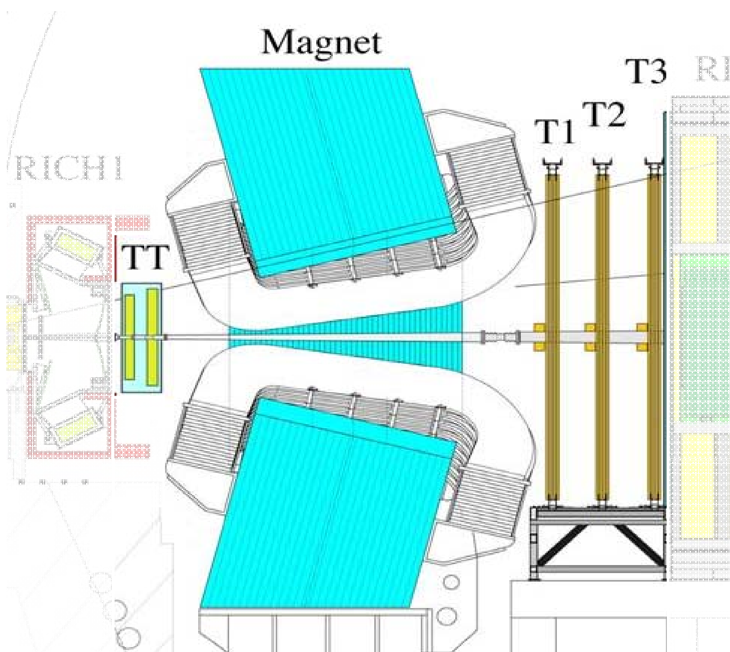
OUTLINE

- LHCb and the Outer Tracker sub-detector
- FE Electronics Overview
- Quality Assurance
- Commissioning of the FE-Box
- Summary

The LHCb Detector



The LHCb Outer Tracker



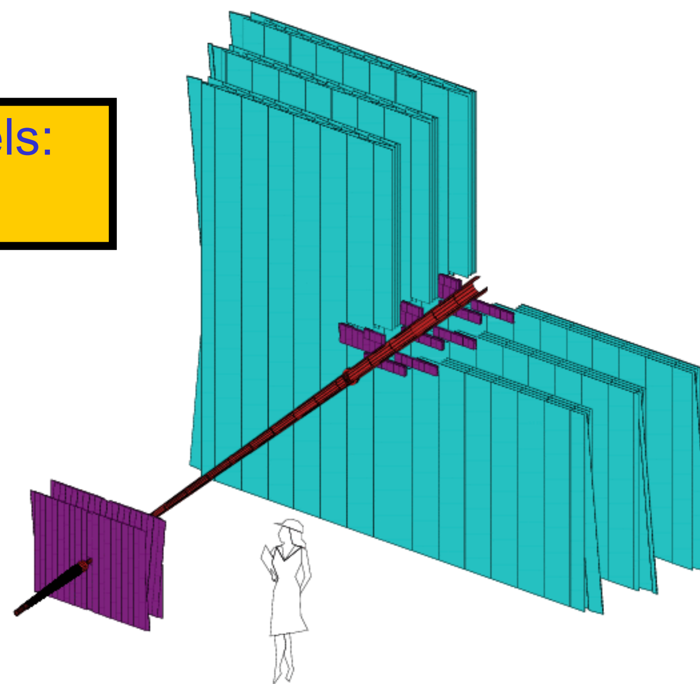
3 OT Stations T1,T2,T3, modular design.

Each OT Station consists of 4 planes XUVX.

B-Field vertical, (measure x-coordinate)

qU,V = ± 5°

Total channels: >56.000

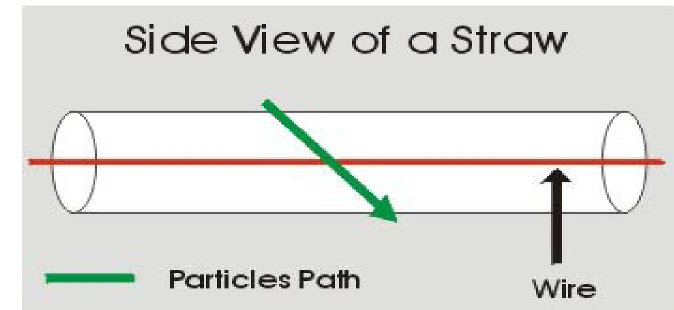


Along the Beam pipe (1%): High-flux region

(Vertex, trigger and inner tracker)

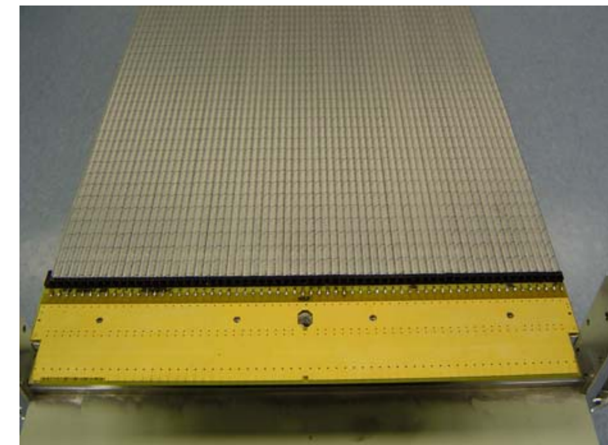
Remaining Area (99%): straw drift-tubes (Outer Tracker)

Basic OT Unit: the module



- A straw tube, (5mm ∅), is wound from two layers of foil material, (carbon-doped kapton and aluminum).
- Gold plated tungsten wires (25 mm ∅).
- Gas mixture Ar/CO2 in ratio 70/30

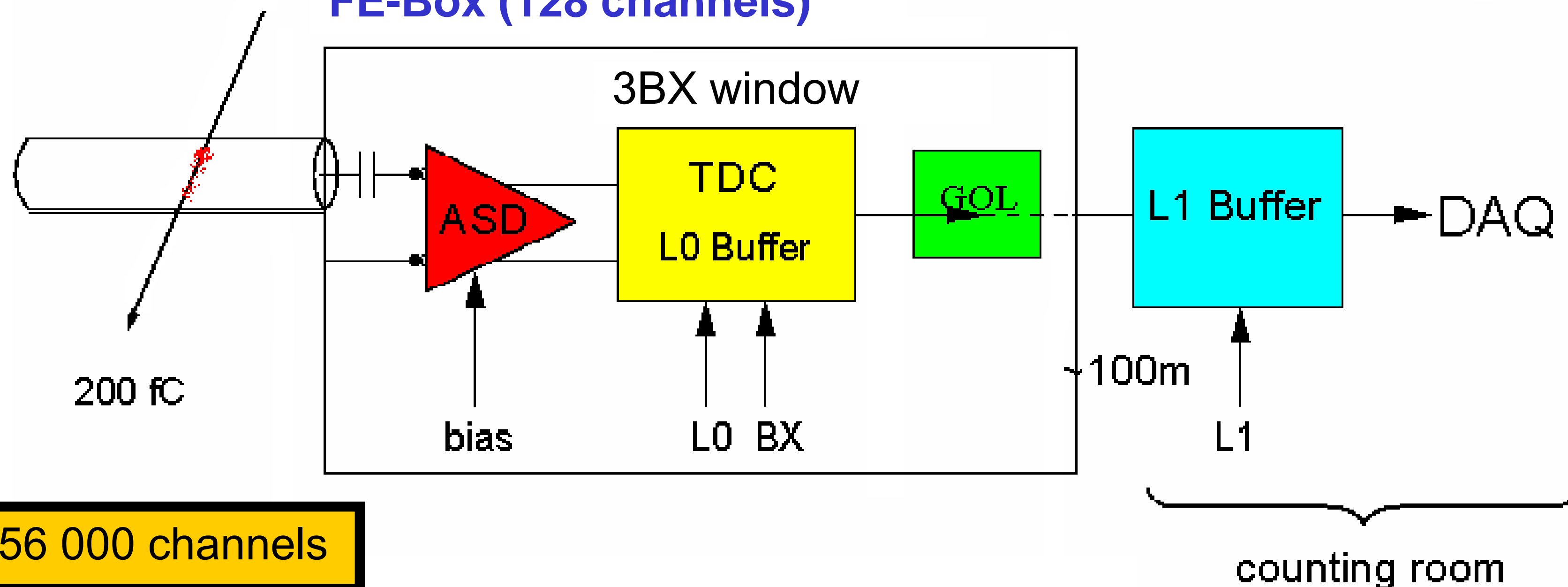
- Two mono-layers of 64 straw tubes each
- Two sandwich panels to support the straw tubes
- Two side walls to seal the gas box



Extremely Light-Weight Structure (crucial for tracking!)

- ❑ **Total weight in sensitive area: 6.8 kg**
- ❑ **Total radiation length X/X_0: 0.37%**

OT FE Electronics Overview



- Amplify analog signals from anode wires (ASDBLR board)
- Digital conversion (ASDBLR board)
- Drift Time measurement (OTIS board)
- Data optical link and services (GOL board)

OT FE Electronics Overview

MASS PRODUCTION:

500 GOL/AUX Boards

2.000 OTIS TDC Boards

4.000 ASDBLR Boards

2.000 HV Boards

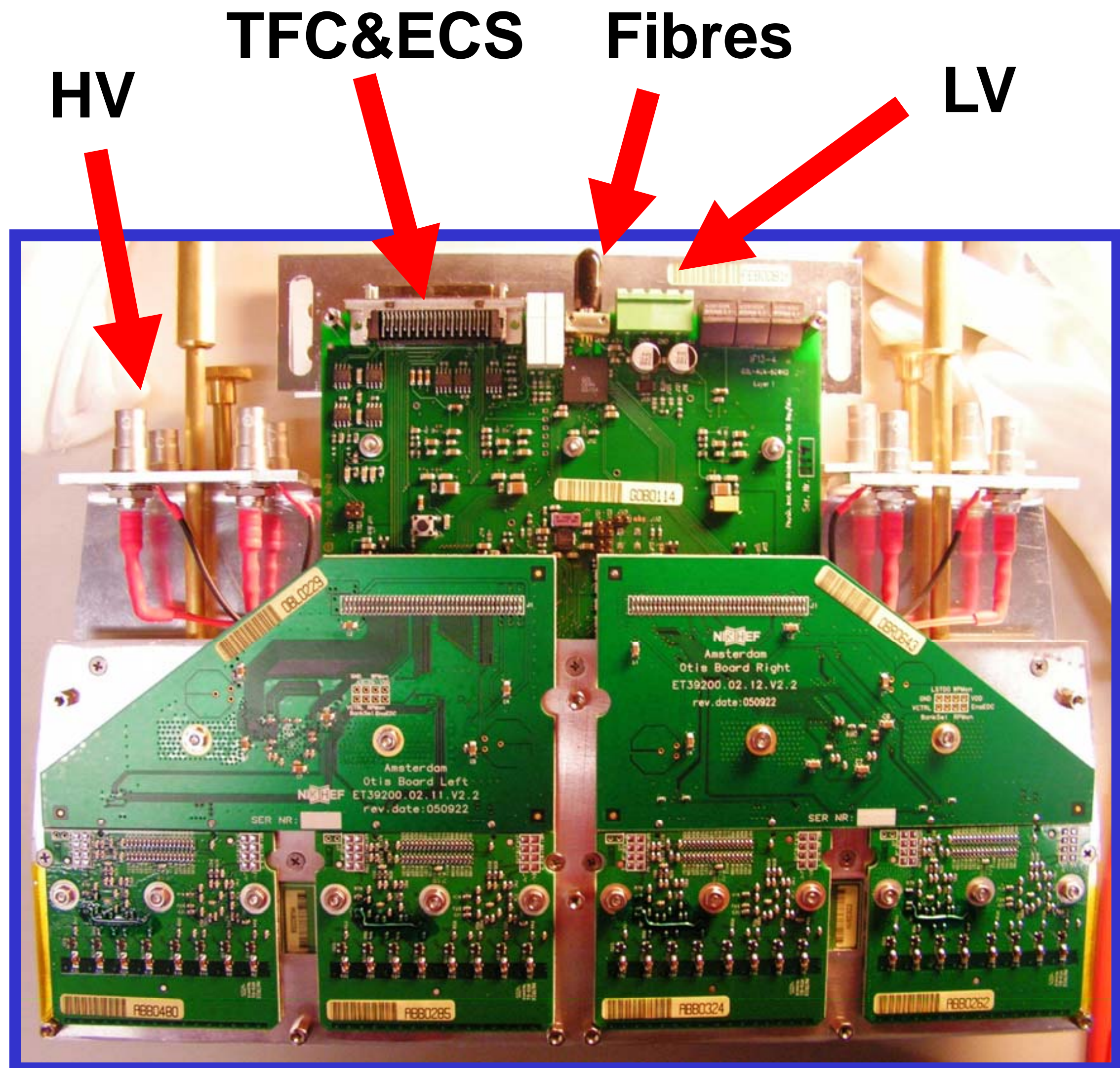
Front end box (full size):

128 channels

16 ASDBLR chips

4 OTIS TDC chips

1 optical link: 1.6 Gbit/s



Quality Assurance

- **HV board :**
  - Visual Inspection of bare PCB (alignment holes)
  - Thickness measurement of the bare PCB
  - Leackage and capacitance long term burn-test in a hoven
- **ASDBLR board :**
  - ASDBLR ICs Selection (~40% used ⇒ single Thr sub-detector!)
  - Visual inspection of the input/output connectors
- **OTIS Board :**
  - OTIS ICs selection
  - Visual Inspection of bare PCB
  - Visual inspection of the input/output connectors
  - Bonding and test (before and after globtop)
- **GOL Board :**
  - Dedicated Setup for GOL board-testing
- **FE-Chassis**
  - Mechanical and electrical check

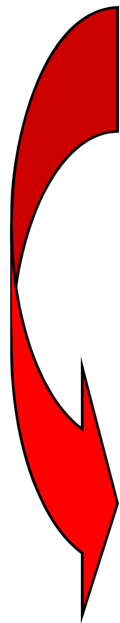
All test informations collected in a DataBase (important to track back problems)

FE-Setup

FE-Setup for commissioning of a completed FE-Boxes

Test of global functionality of FE-Boxes, requirements:

- Analog input signal injection (mimiking the straw-like signal)
- Generation of ECS & TFC
- Data Acquisition (Fiber ⇒ Disk)
- High time accuracy (~0.15 ns)



Threshold Scan

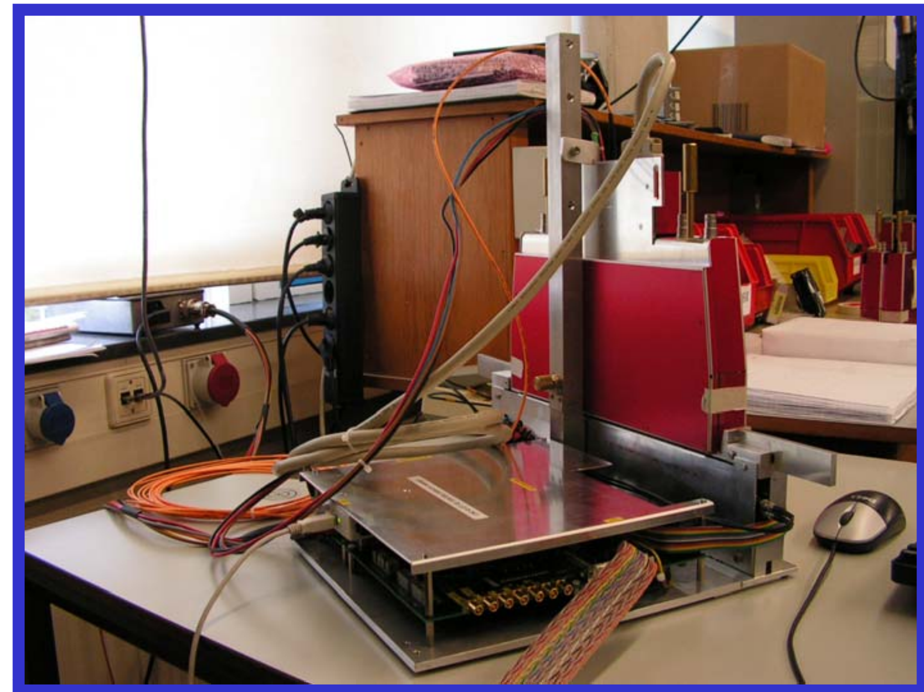
ASDBLR TestPulses (high and low)

Input delay Scan

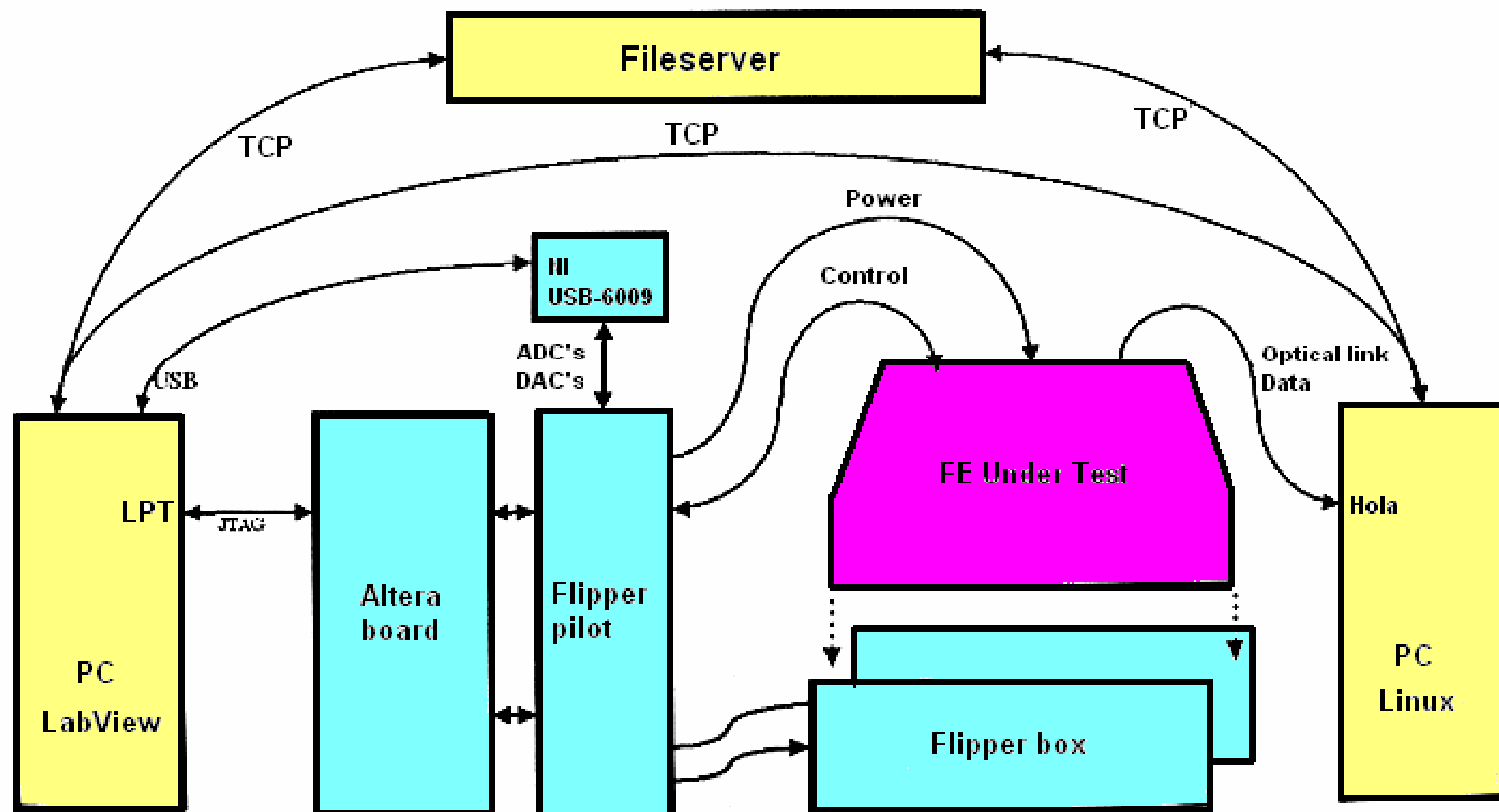
Signal amplitude Scan

L0 (latency scan)

Ect…



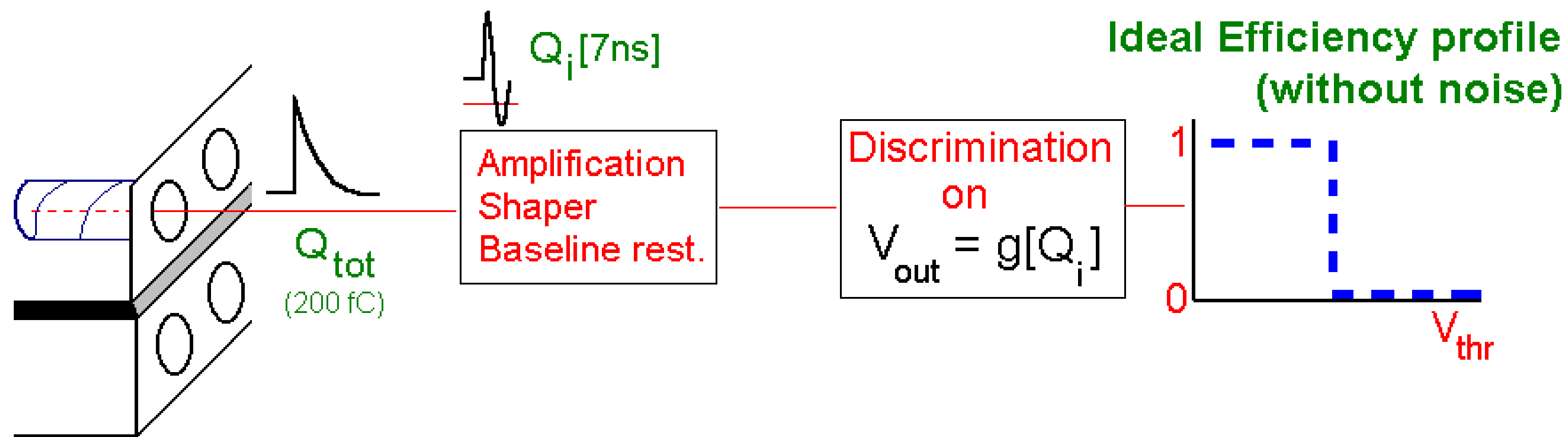
Functional blocks of the FE-Setup



Standard Test sequence

- **Threshold characteristics :**
  - Amplitude Scan with input signal $\Rightarrow V_{thr}^{50\%}$, noise, cross-talk etc…
  - Thr Scan with input signal $\Rightarrow V_{thr}^{50\%}$, noise, cross-talk etc…
  - Thr Scan with Test-Pulse Low $\Rightarrow V_{thr}^{50\%}$, noise, cross-talk etc…
  - Thr Scan with Test Pulse High $\Rightarrow Q_{thr}^{50\%}$, noise, cross-talk etc…
- **Noise :**
  - Thr Scan with no input signal
- **Timing :**
  - Drift-time spectra of all channels
  - Delay scan over the full time range
- **L0 scan :**
  - L0 Delay Scan in steps of ½ BX
- **Analysis**
  - Control histograms automatically generated for all tests

Threshold Characteristics



For a Gaussian Noise Distribution

$$Pr[V_{thr}, Q_i] = \int_{V_{thr}}^{+\infty} f[V]\,dV = N \int_{V_{thr}}^{+\infty} e^{-\frac{1}{2}\frac{(V-g[Q_i])^2}{(s_{noise})^2}}\,dV$$

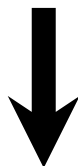
$$Pr[V_{thr}, Q_i] = \frac{1}{2} - \frac{1}{2} Erf\left[\frac{V_{thr} - g[Q_i]}{\sqrt{2}\; s_{noise}}\right]$$

Threshold Characteristics

$$Pr[V_{thr}, Q_i] = \frac{1}{2} - \frac{1}{2} Erf\left[\frac{V_{thr} - g[Q_i]}{\sqrt{2}\ s_{noise}}\right]$$

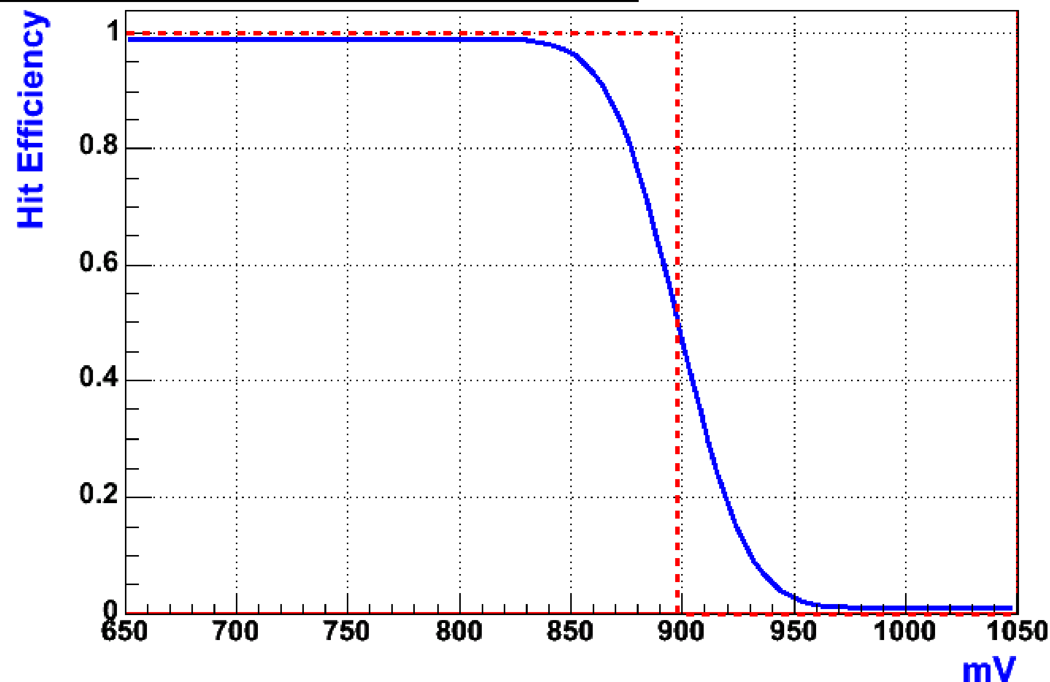
$$if \quad V_{thr} = g[Q_i]$$

$$Pr[g[Q_i], Q_i] = 0.5$$



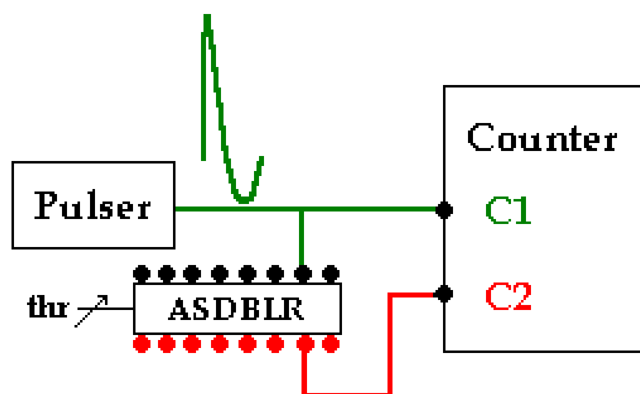
$V_{thr}^{[50\%]}$

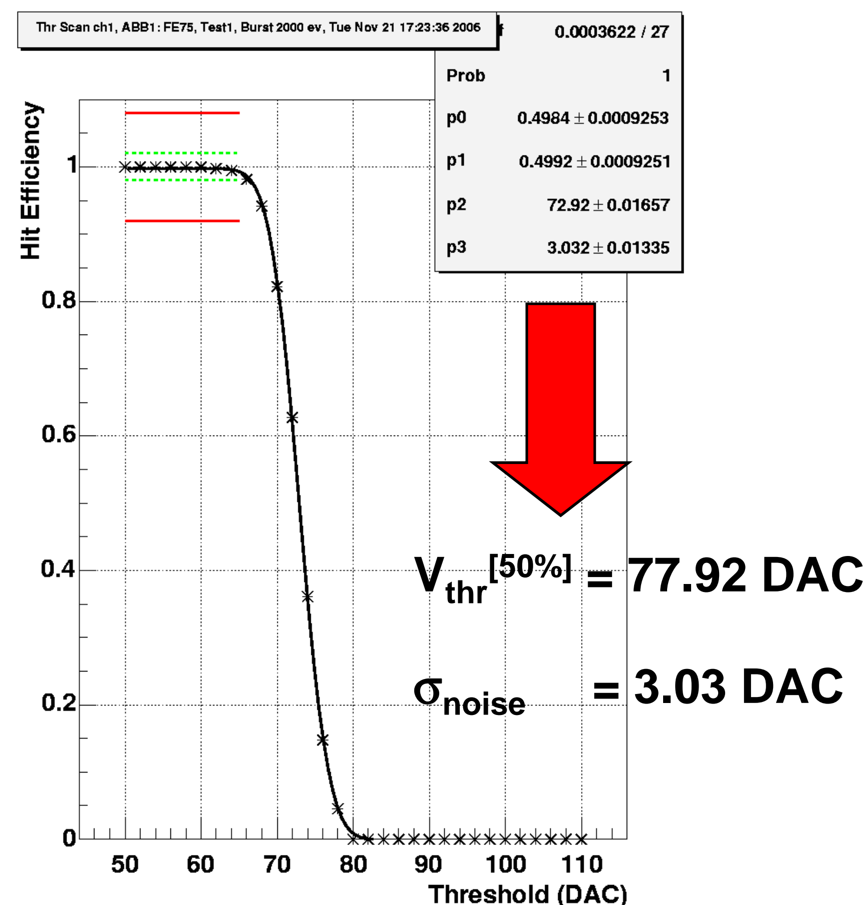
best estimator of g(Qi)



Measure the hit efficiency profile **for each channel**, fit errf model to data and determine $V_{thr}^{[50\%]}$ and σ_{noise}

Hit Efficiency = C2 / C1

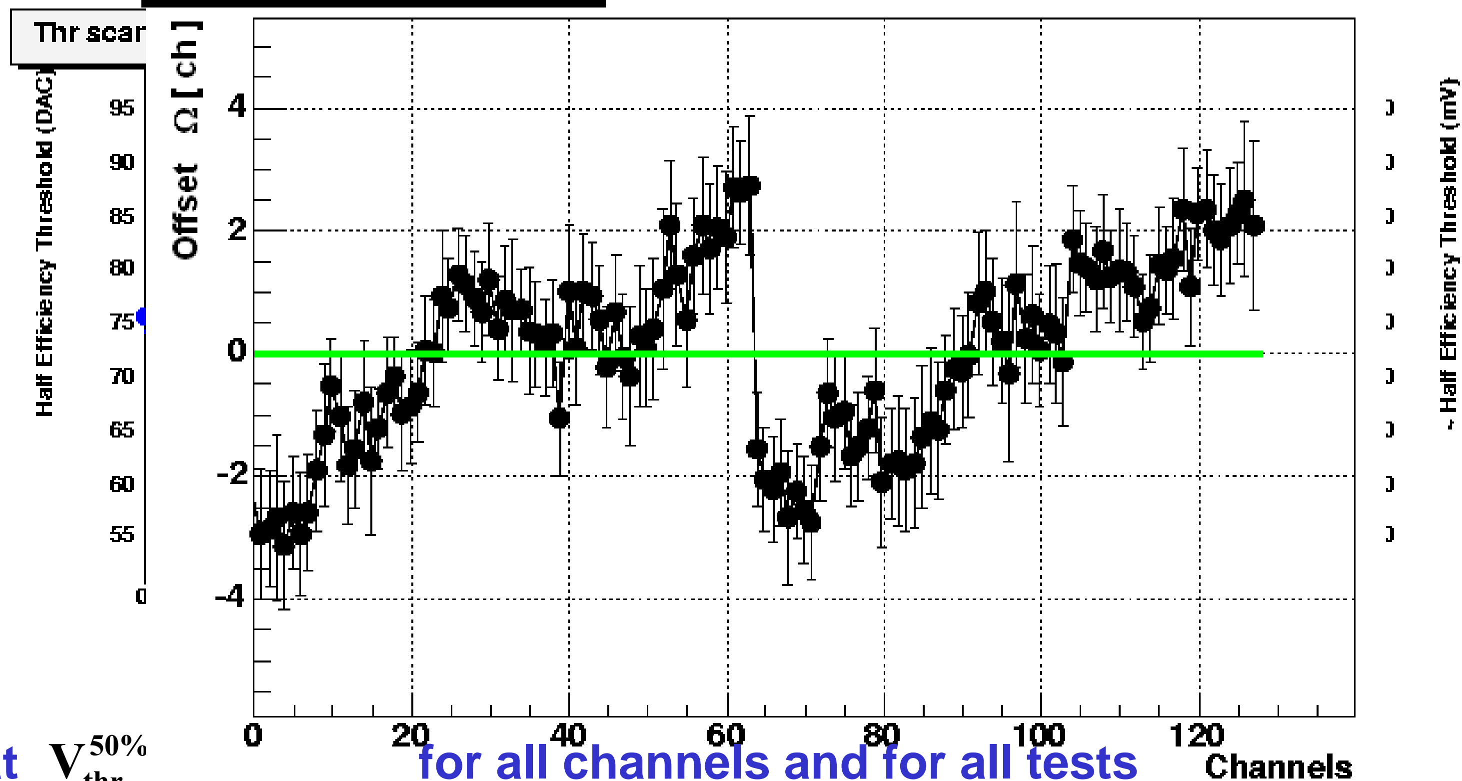




Channel to channel uniformity expected to be within ~50 mV

FE-Test Systematics: Charge Offset

Preliminary

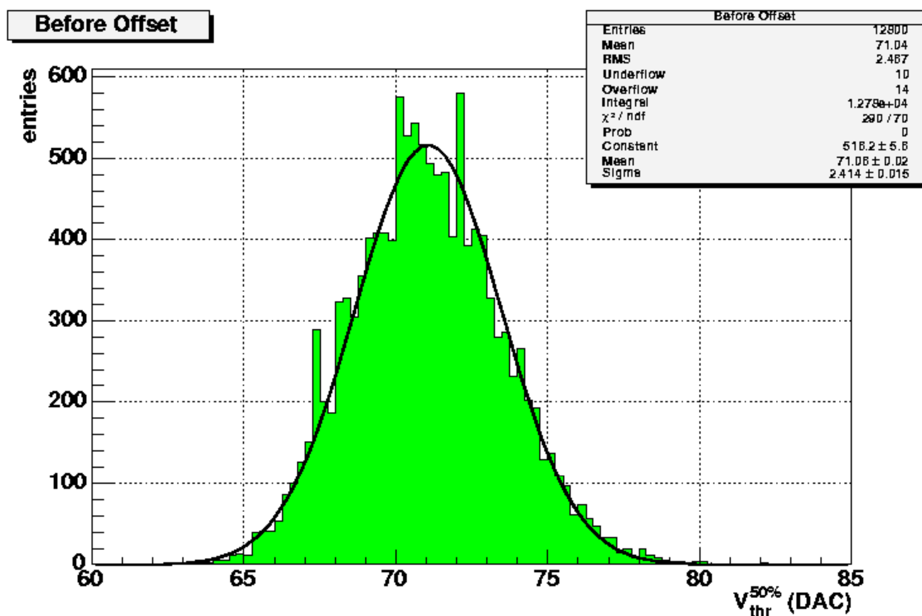


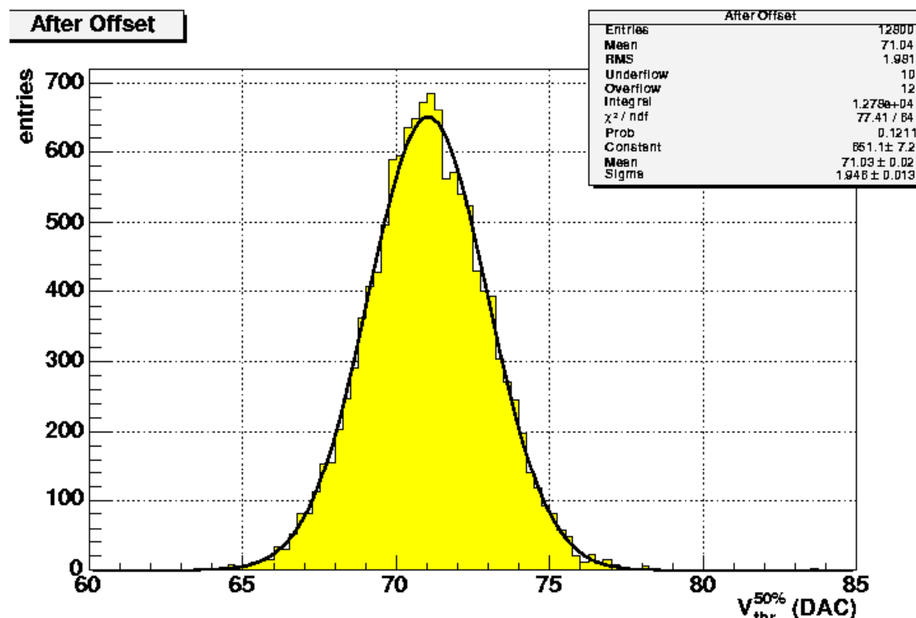
Look at $V_{thr}^{50\%}$ for all channels and for all tests

Define correction offsets:

$$\Omega[ch] = \frac{\sum_{ch}\sum_{Tests} V_{thr}^{50\%}[ch,\#Test]}{128 N_{Tests}} - \frac{\sum_{Tests} V_{thr}^{50\%}[ch,\#Test]}{N_{Tests}}$$

Correct for Charge Offsets





- $V_{thr}^{50\%}$ Distribution before Offset Corrections
- $V_{thr}^{50\%}$ Distribution after Offset Corrections

Powerful Check:

- Large deviating or broken channels found: due to missing component, shorts on the connectors, bad chip soldering ect…
- Amazing uniformity (we gonna use one threshold for all the discriminators)

Amplitude Scan

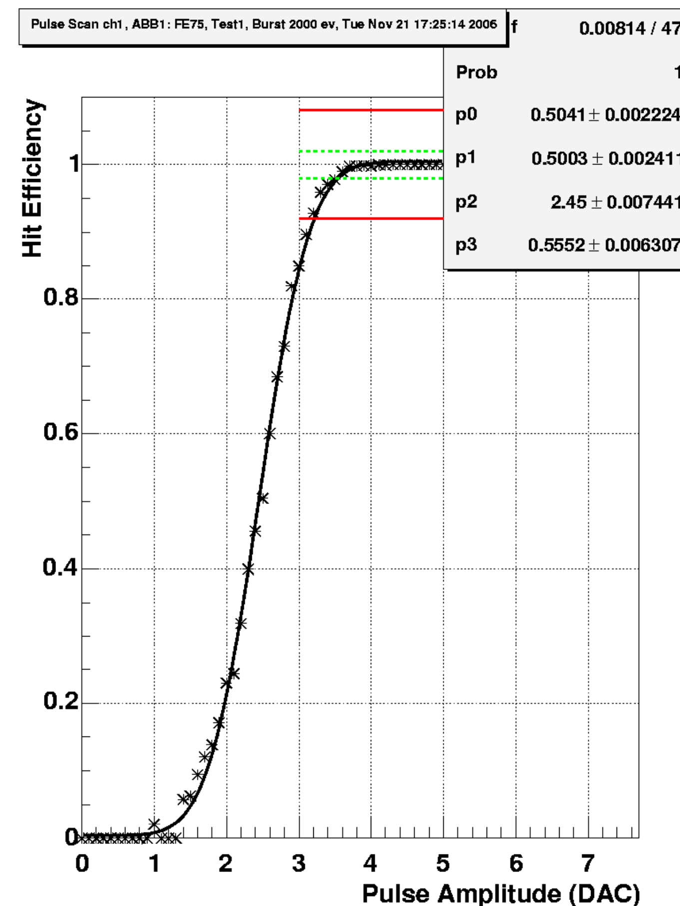
- Fixed threshold of ~800 mV, Burst length of 2000 events

$$Pr[V_{thr}, Q_i] = \frac{1}{2} + \frac{1}{2} Erf\left[\frac{Q_i - Q_{thr}}{\sqrt{2}\ \mathbf{ENC}}\right]$$

- Fit error function to data points for **each channel**
  - Half-Efficiency Amplitude
  - Width (σ)
  - Chi2 (χ2)

- Q_{thr} Global Uniformity

- **ENC** Direct measurement of Equivalent Noise Charge (fC)

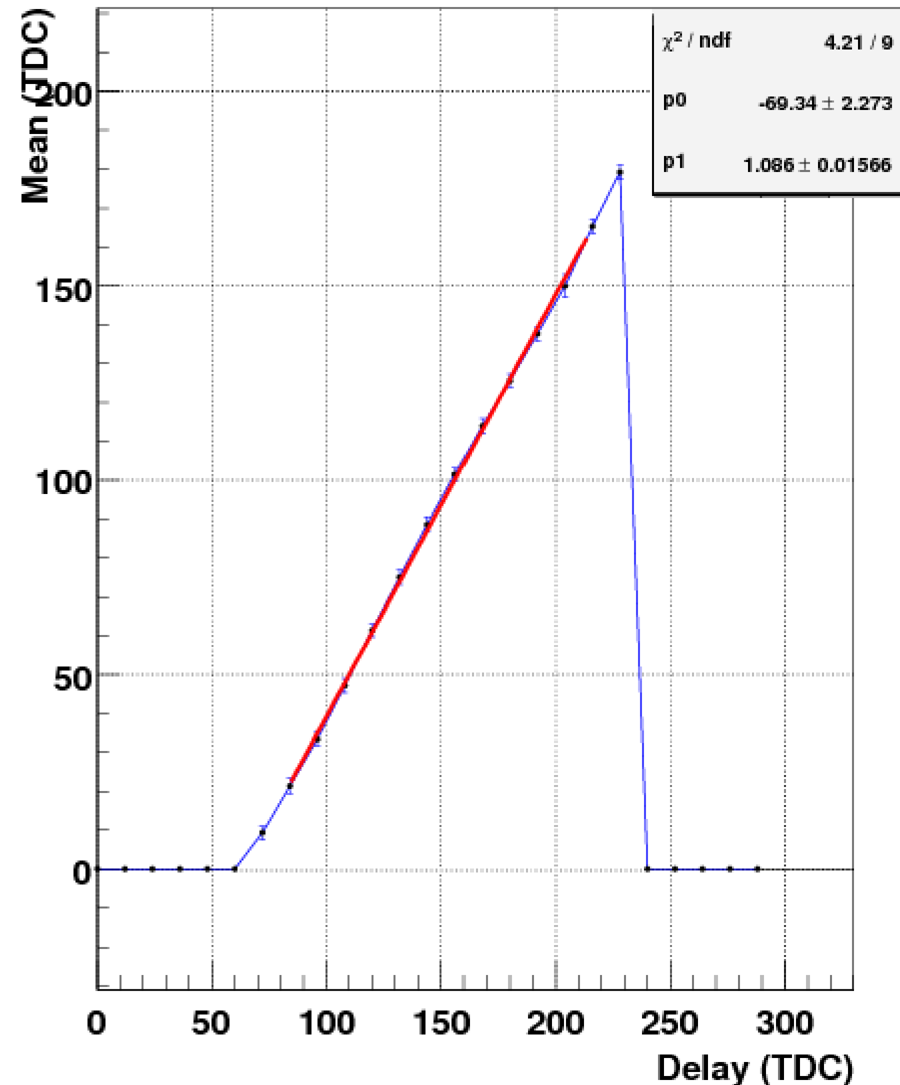


Input Charge Delay Scan

- Fixed threshold of ~800 mV,
  Fixed charge of ~6 fC
  Burst length of 2000 events

- Fit linear function to data points for **each channel**

- Reject if:
  - Offset deviant from other channels.
  - Large χ2/Bad data



Time Resolution

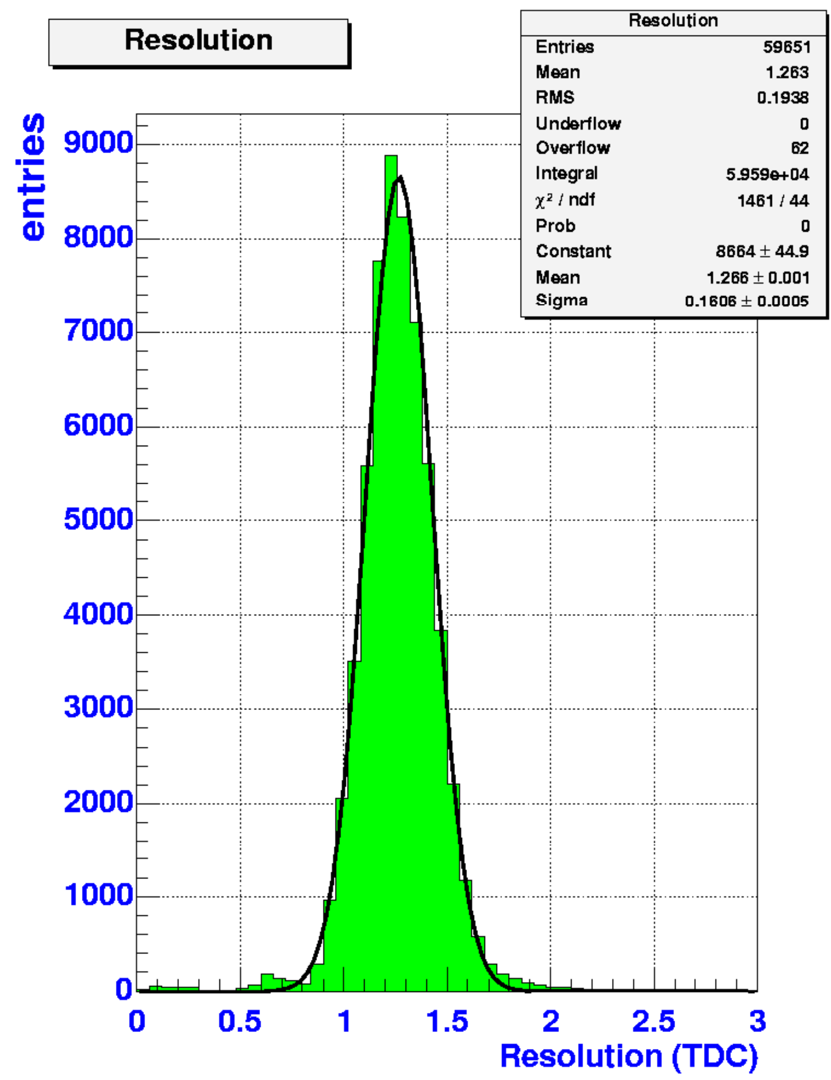
Average result over 50 FE Boxes:

1.27 ± 0.16 TDC channels

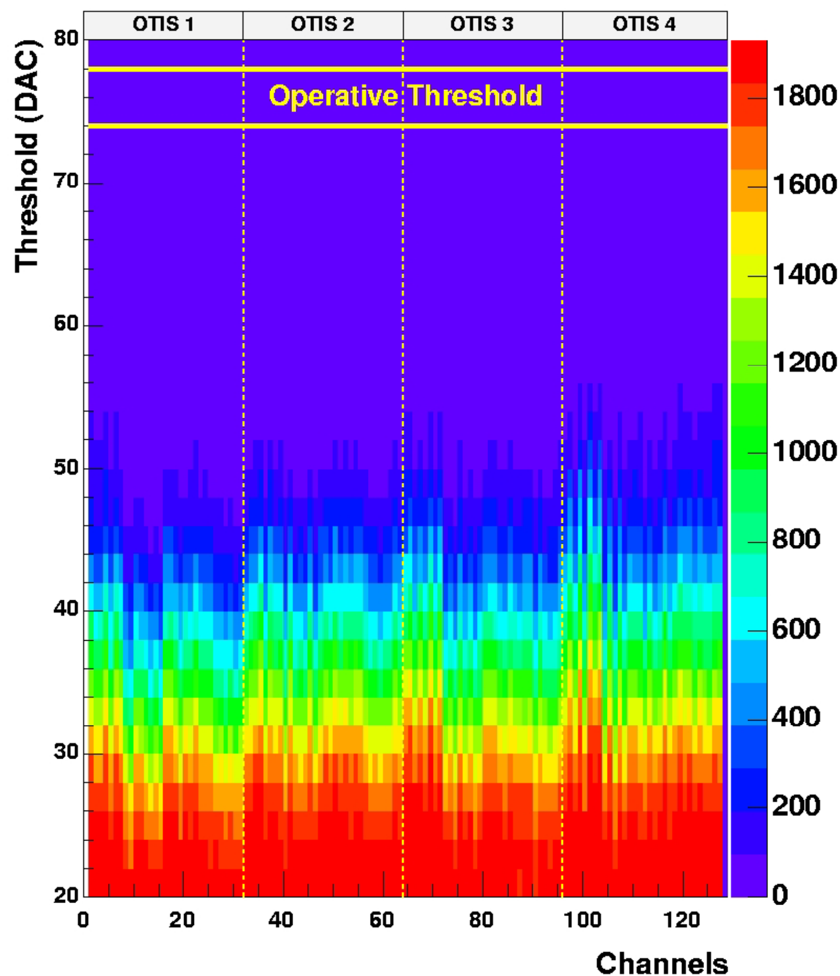
i.e.:

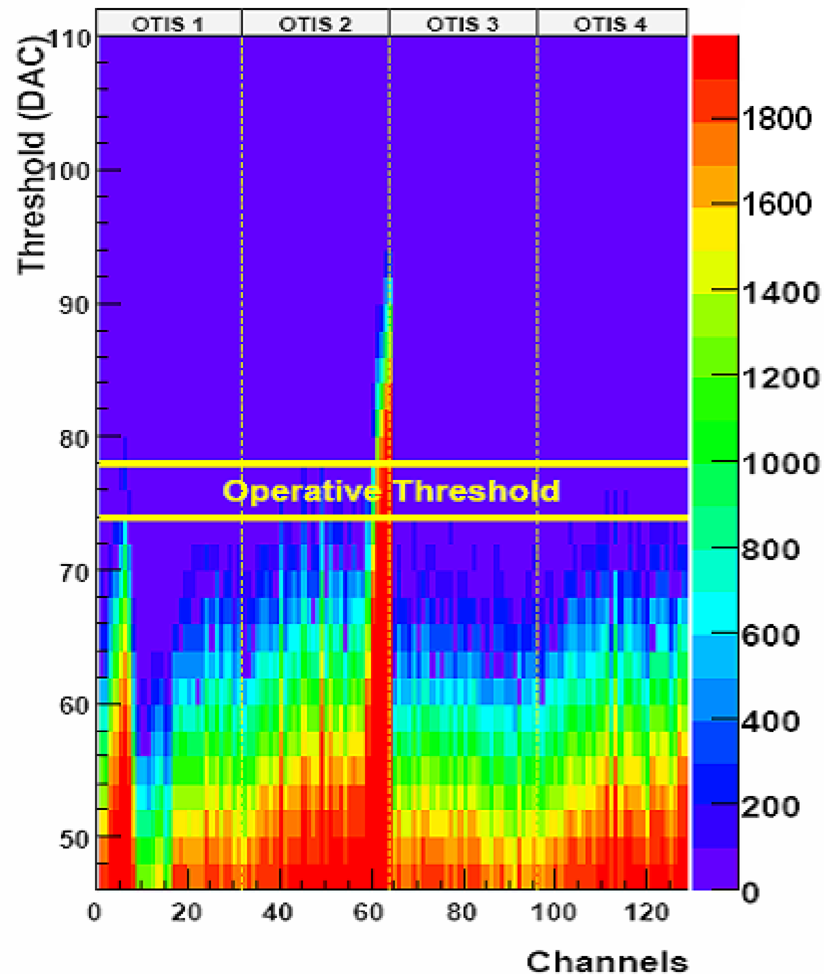
0.496 ± 0.062 ns

(includes contribution of input-pulse timing resolution, etc.)

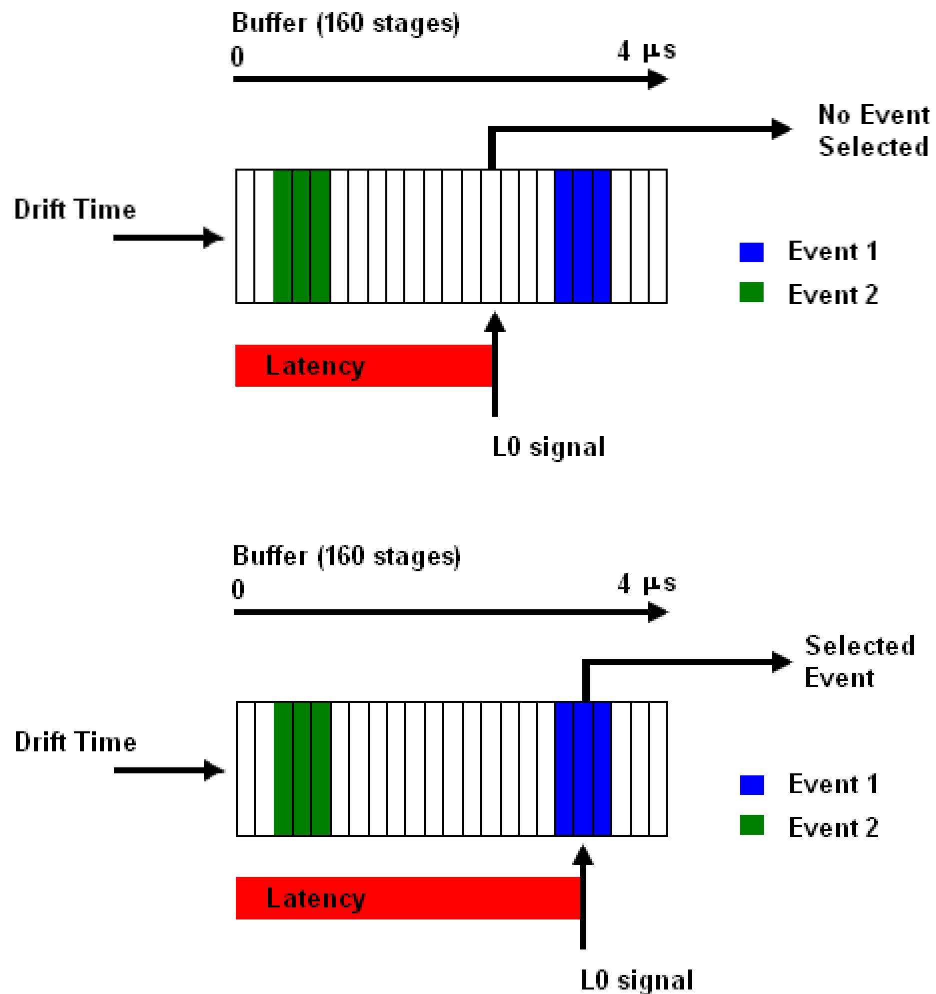


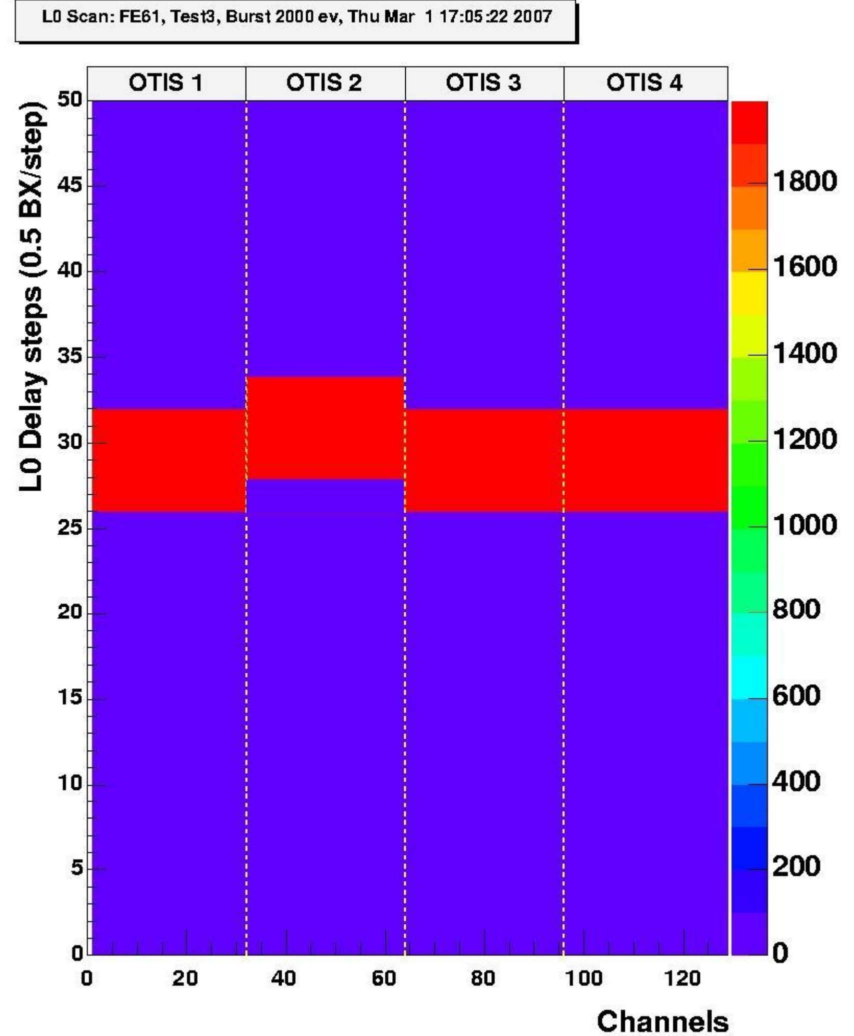
Noise





Latency





Summary

- Boards production&test completed in June 2007

- FE Production at NIKHEF of the LHCb Outer Tracker electronics is currently at Regime:
  - ~210 / (~50%) FE-Boxes assembled and tested
  - 36 FE-Boxes installed and tested in situ

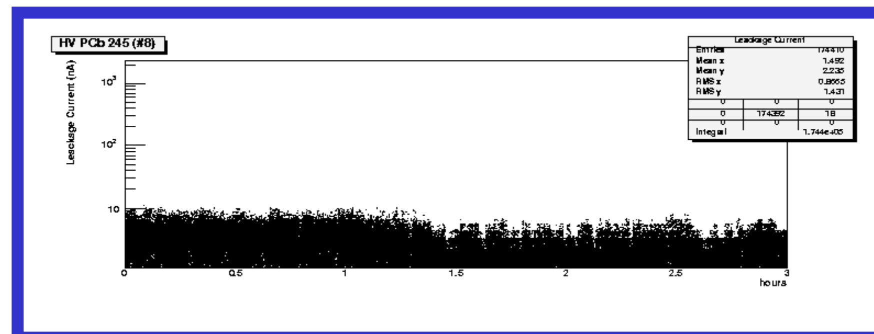
- Excellent and compact test-of-performance of the Read-Out achieved using the FE-Tester Setup (important in the R&D phase)

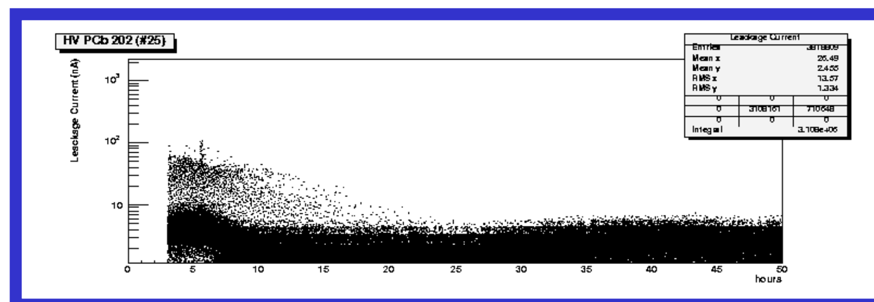
- Electronics partially installed on the Outer-Tracker: used for a first commissioning of the electronics chain (straw ⇒ Counting room)

- A FE-Setup will be kept in the LHCb pit for FE-Testing and hardware debugging

Additional Slides

HV Board Test





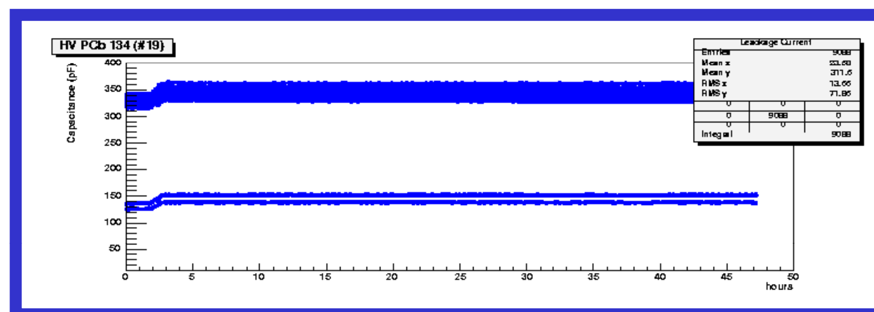
Test for:

Capacitance

Leakage Current

Settings

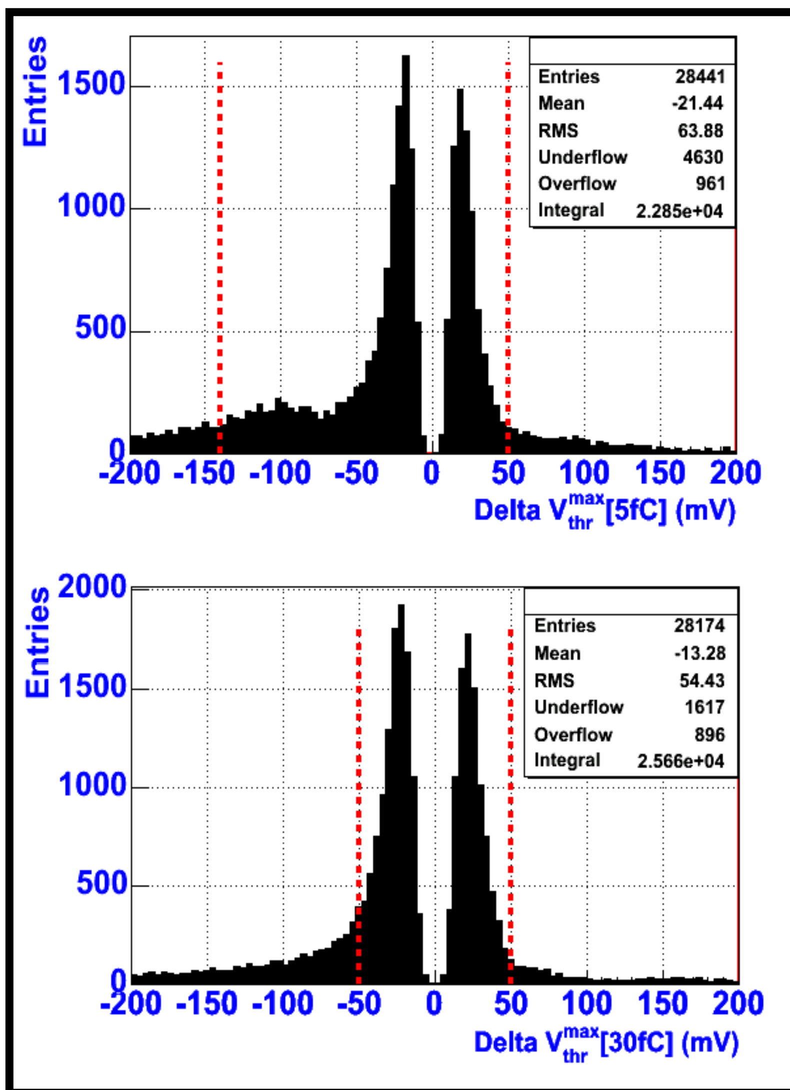
- 48 hours
- 2000 Volt
- 70° C



ASDBLR ICs Selection

Cut	Test	Losses	Survivors (%)
T1	*Input Resistance*	1738	94.10
T2	*Supply Current (P)*	2015	87.26
T3	*Supply Current (N)*	102	86.91
T4	*BLR Monitor*	46	86.75
T5	*Diode Voltage*	119	86.35
T6	*Input Current*	272	85.43
T7	*Output Current*	131	84.98
T8	*Output Switch*	2678	75.89
T9	*Broken Channels*	4023	62.23

Cut	Test	Losses	Survivors (%)
T1-T9	*Pre-Selection*	11124	62.23
T10	*Half Efficiency*	5690	42.90



Deviation Parameter

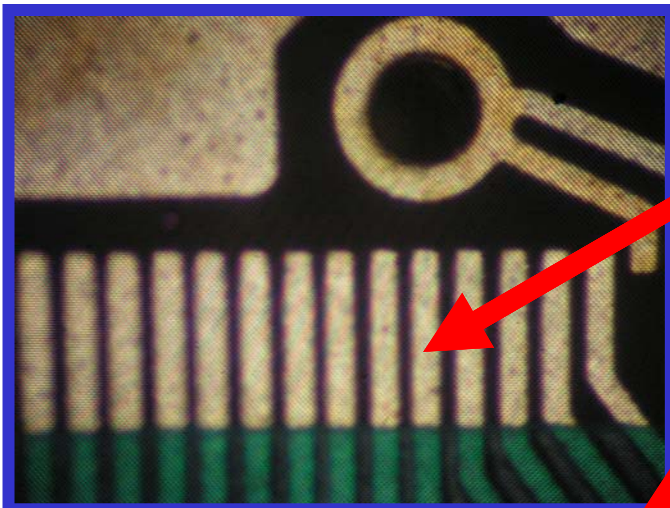
$$\Delta V_{thr}^{[50\%]}[j] = 1/8 \sum_j V_{thr}^{[50\%]}[j] - V_{thr}^{[50\%]}[j]$$

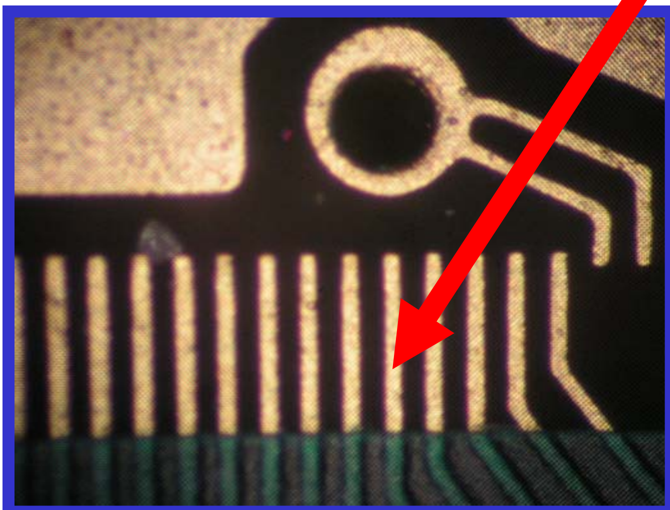
Max Deviation Parameter

$$\Delta V_{thr}^{max} = Max_{j \in \{1;8\}} \{ \Delta V_{thr}^{[50\%]}[j] \}$$

Performed:

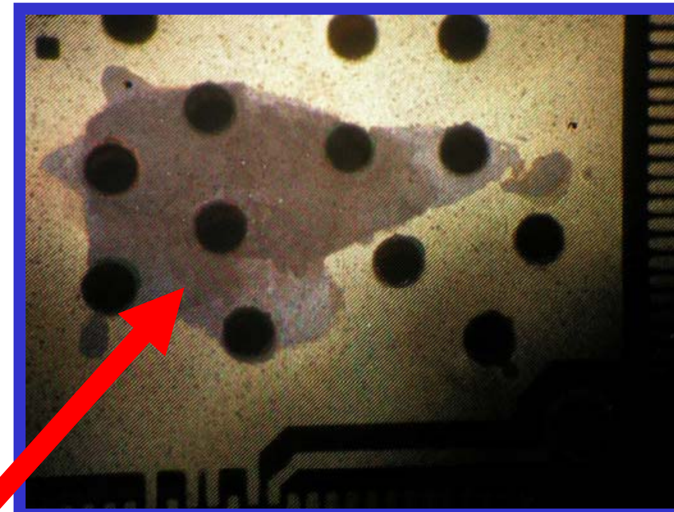
* For each chip
* Foreach Charge injected

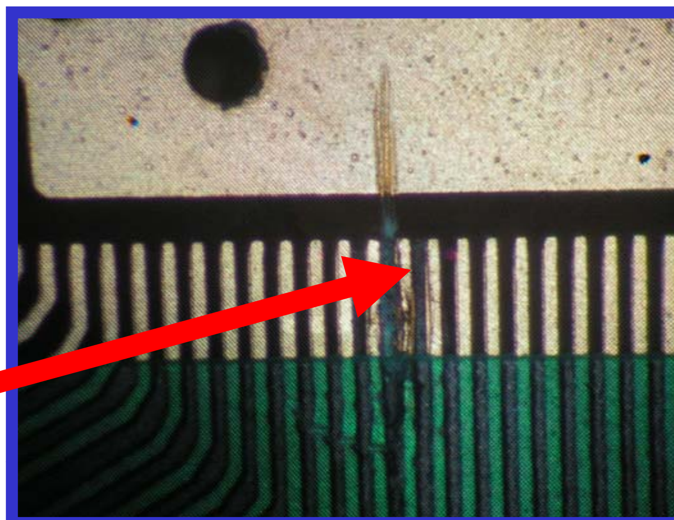




Good bonding pads

Bad (thin) bonding pads





Spot on grounding plane

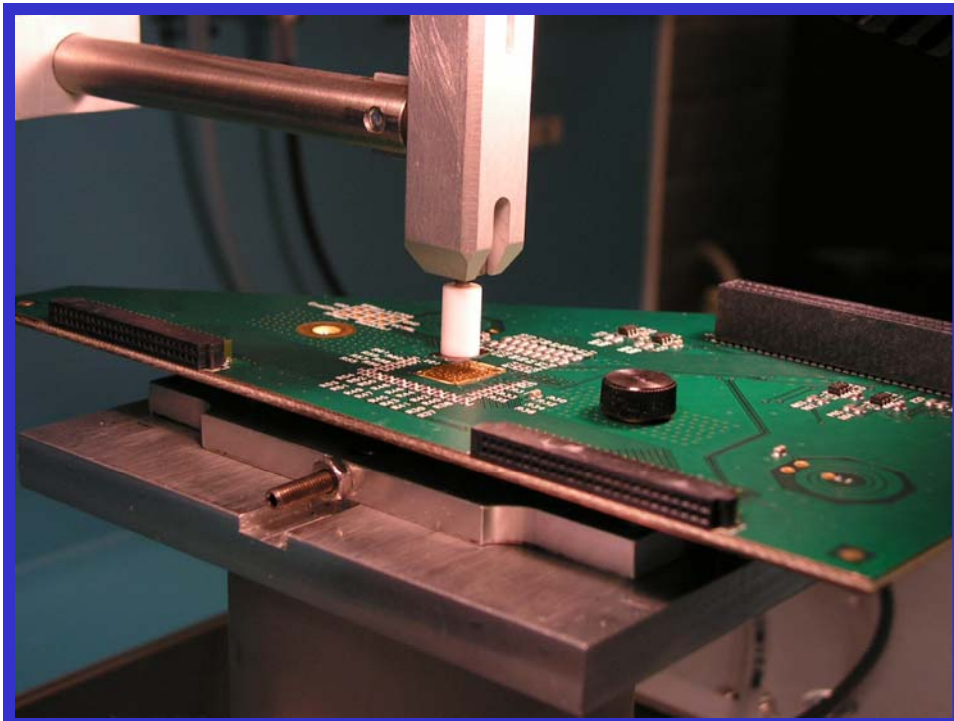
Short

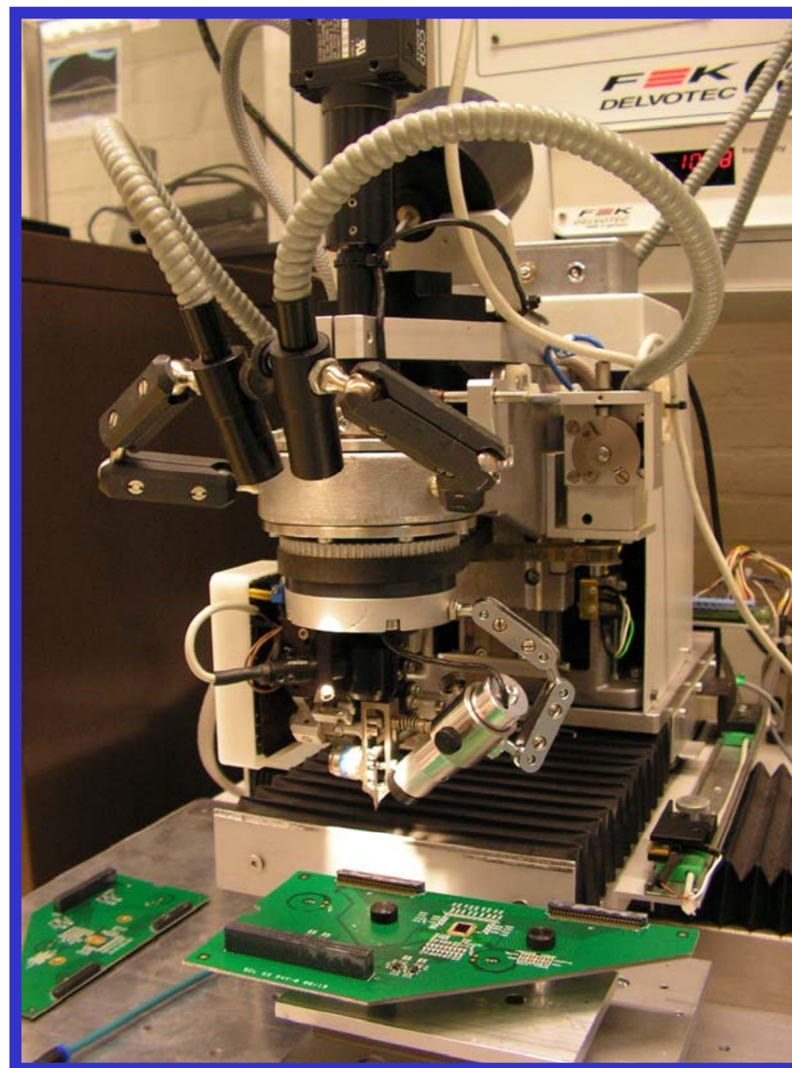
OTIS ICs Selection

Test procedure for each chip:

- power consumption ok? (I < 300mA@2.5V)
- Slow control test: Check position ID and registers
- FPGA test:
  - Chip alive?
  - Header ok?
  - All channels alive?
  - Measurement of DNL for channel 0, 15,16, 31
    (DNL < 2.0 bins for OTIS 1.2 and
    DNL < 1.9 bins for OTIS 1.3,
    typical values: 0.5 bins< DNL < 1.5 bins)
  - Buffer overflow recognized?
- DAC‘s functional?

OTIS Board Bonding and Test





Solid silver-filled epoxy glue

Ultrasonic Soldering (~16 gr/wire)

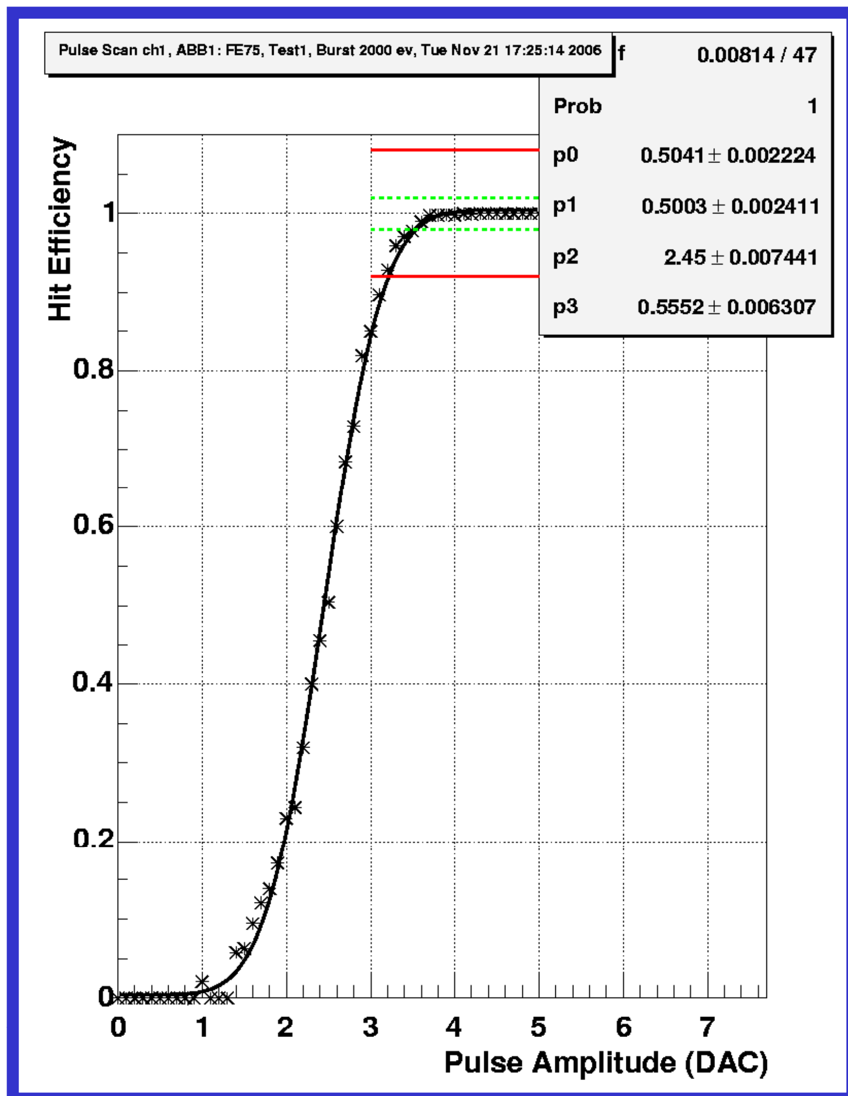
Semi-Automatic procedure (~120 s)

Visual Inspection (1-2% repaired)

OTIS Board Bonding and Test

- **I2C test** (test of the OTIS register)
- **ADC Test** (Set the ASDDAC of the OTIS and measuring the output voltage)
- **ID Odd** (check if the data set is received correctly)
- **L0 Reset** (Check the data receiver)
- **Event ID distributions** (Flatness distribution with random trigger)
- **Header Bits** (Comparison with standard default header)
- **Event count Reset** (Check of the number of triggers received)
- **Power Up Reset** (Check the DAC register)
- **Id Even (**Check if the data set is received correctly**)**
- **Hit Map Odd/Even** (Check of the number of valid hits)

Amplitude Scan



If,

$$g(Q_{in}) = V_{off} + G \bullet Q_{in}$$

Then,

$$Pr[V_{thr}, Q_i] = \frac{1}{2} + \frac{1}{2} Erf\left[\frac{Q_i - Q_{thr}}{\sqrt{2}\ \mathrm{ENC}}\right]$$

Where,

$$Q_{thr} = \frac{V_{thr} - V_{off}}{G}$$

- **Q_{thr}** Global Uniformity
- **ENC** Direct measurement of Equivalent Noise Charge (fC)