System Aspects of the ILC-Electronics and Power pulsing

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- Introduction: Parameters from accelerator, physics, detector
- Physics prototype
- System aspects: (calorimeter) electromechanical design, DAQ chain, calibration
- Power power cycling, cooling
- Outlook

Work done by the CALICE Calorimeter for ILC

...ilc - The Accelerator

s = 0.5 TeV

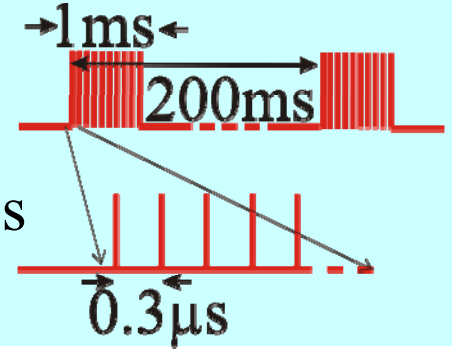
point like particles

- ► precision physics
- ► seldom interactions

Time structure of bunches

Trains of bunches

Individual bunches



Consequences for electronics:

- ► Fast electronics: 0.3µs structure and faster for precision
- ► Power intensive fast analog only for <1% of the time
- ► Long breaks for data handling
- ► Low occupancy
- ► No radiation damage

Physics Plans

Study of heavy particles: Properties with precision

Case studies:

t,H → Z,W → leptons

jets

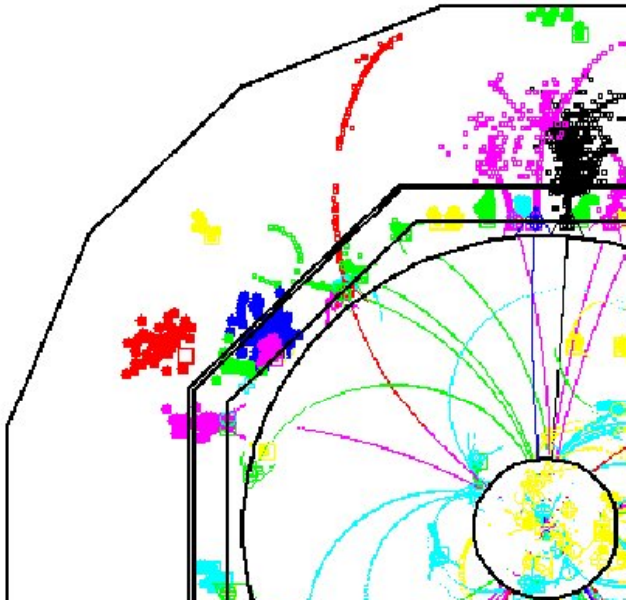
Distinguish by mass reconstruction

Requirements for the detector:

- High energy resolution: Jets $\Delta E/E = 30\%/\sqrt{E}$
- Vertex and tracking

This talk

Jet Energy by Particle Flow



Measure individual particle by p or E:

- charged: momentum
- Photons: elec.magnetic calorimeter
- Neutral hadrons: hadronic calorimeter

Sum: Each particle once and only once

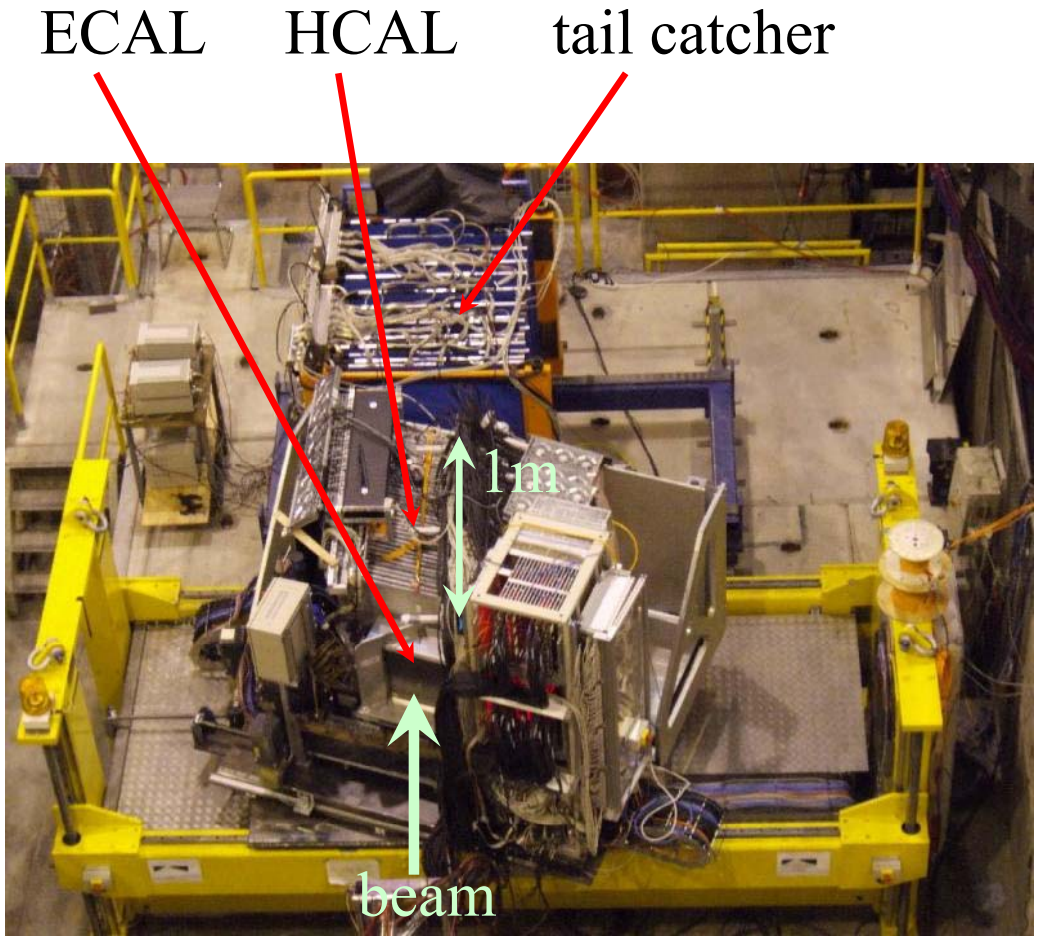
Compensating: Separating shower into
elec.-magn./hadronic contributions
delayed hits from neutrons (ns)

Requirements to detector design:

- ► Separate each particle before hitting the calorimeter
  - ► large B-field and large radius for tracking
- ► Track particles inside calorimeter
  - ► **high granularity**, small shower sizes, ns-timing

Prototype Running at Test Beam

Physics prototype was in test beam at CERN for 2 month



Goal to prove algorithm
test ideas/components

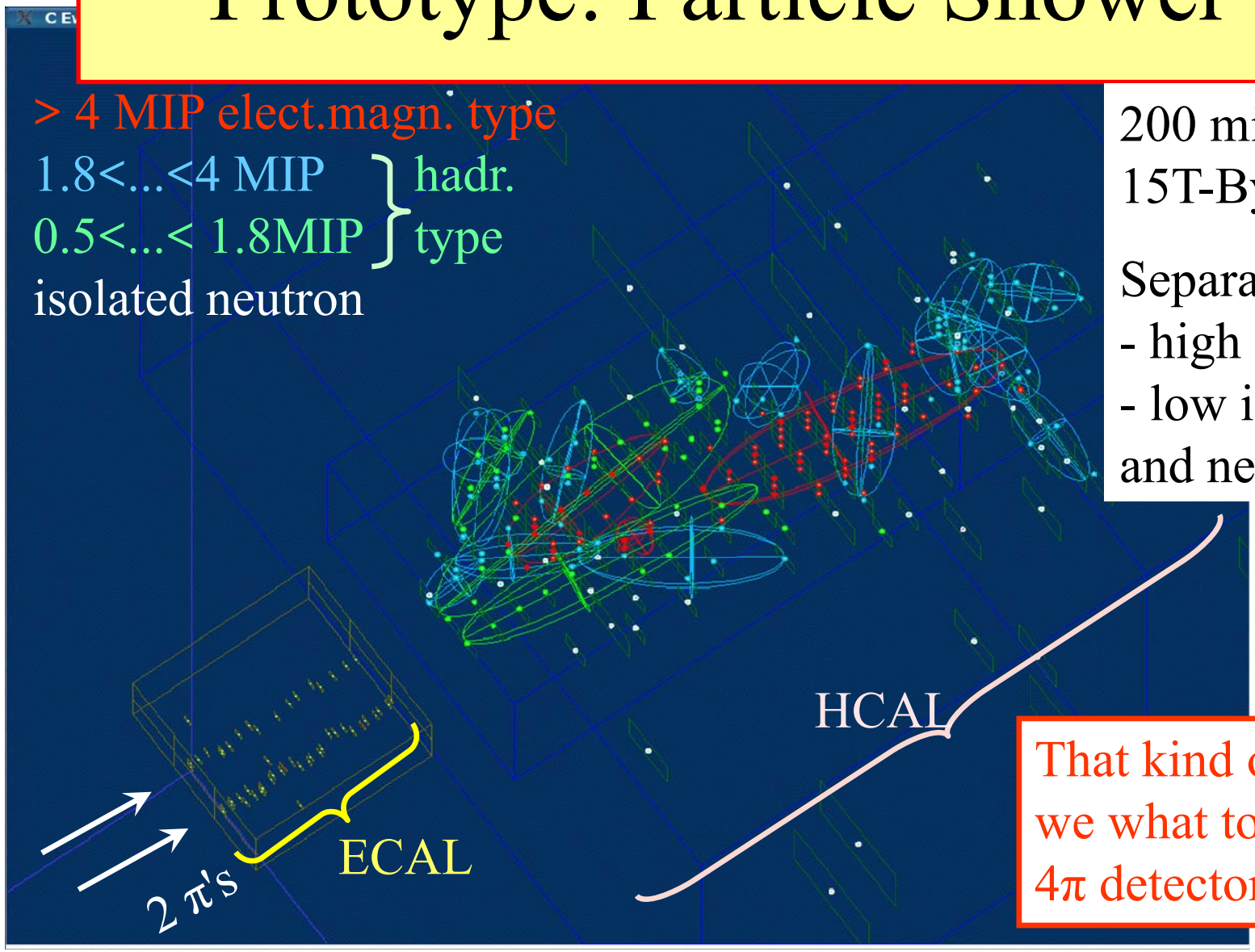
Already many channels

ECAL	6480 channels
HCAL	7608 channels
tail catcher	320 channels

Total 14k channels

Electronics sits at the side, but
ILC needs: No dead volume
► concept for
integrating the electronics

Prototype: Particle Shower

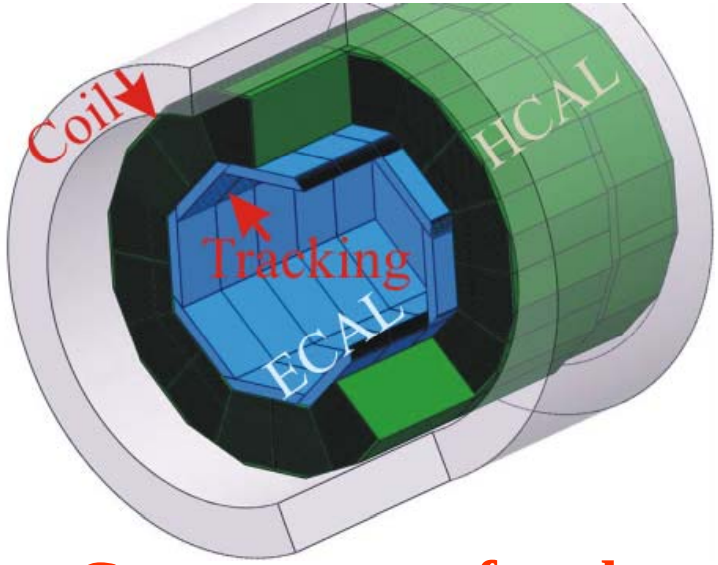


200 million events
15T-Byte

Separated clusters
- high ionization
- low ionization
and neutrons

That kind of detail we what to use at an 4π detector at ILC

Detector Concept:



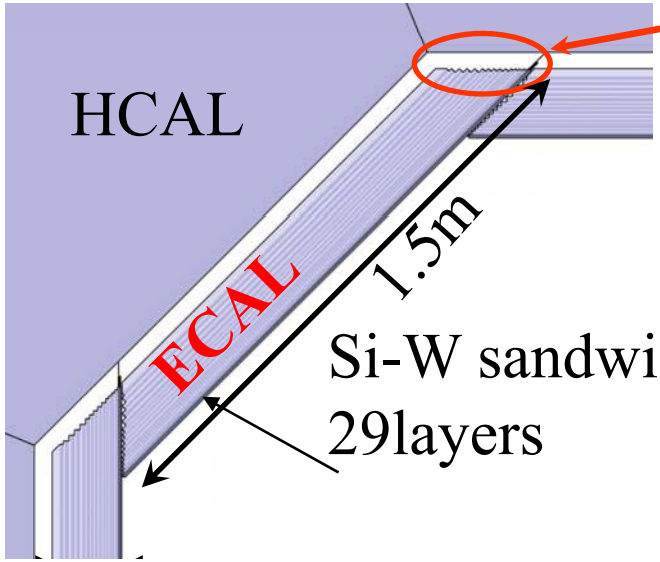
Calorimeter squeezed - Large Tracker
- Outer Coil (costs)

► Dense calorimeter,
W, Fe (stainless) absorbers
Thin sensors and electronics
►High granularity: 100 million channels
16 bit resolution

Consequences for electronics:

► First stage (VFE) integrated into absorber, located in the showers
► VFE has to be compact ► ASIC's
► Multiplexing in VFE with few control/signal lines
► Simple and small infrastructure: e.g. cooling ► very low power
► Some additional space at surface and cracks of modules

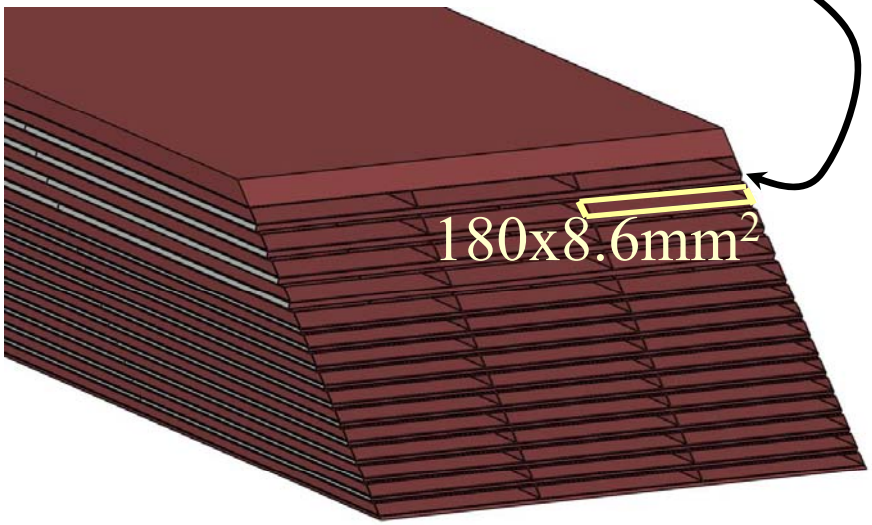
System: ECAL

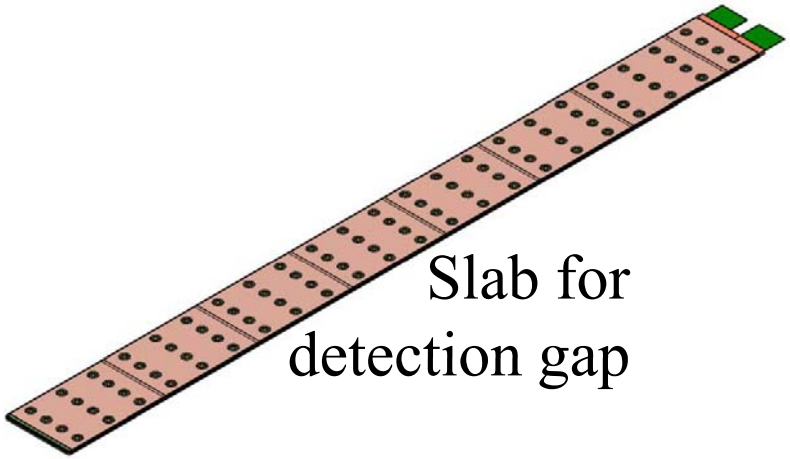


Space for end-gap electronics
for infrastructure

Si-W sandwich
29layers

Structure, in which electronics
has to be slapped in over 1.5m

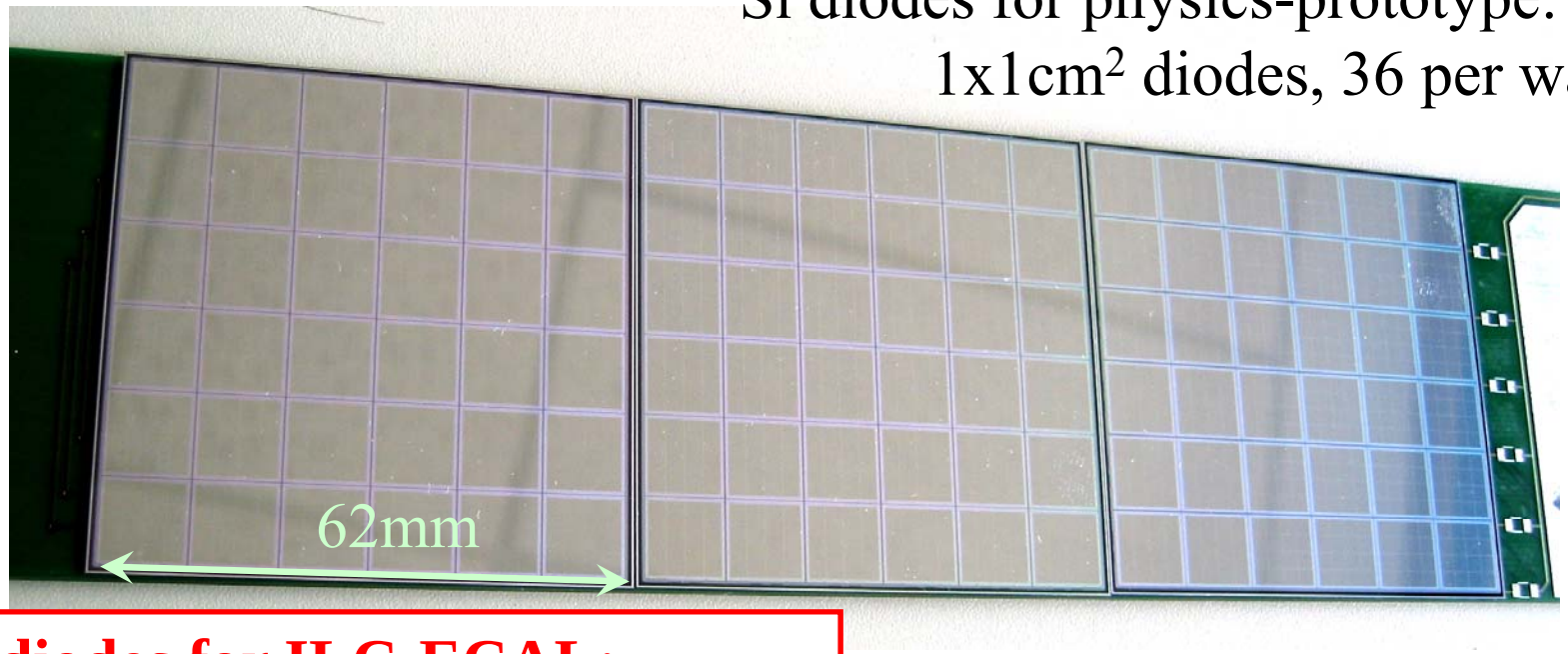




Slab for
detection gap

ECAL: Si-Diode as Sensor

Si diodes for physics-prototype:
1x1cm^2 diodes, 36 per wafer

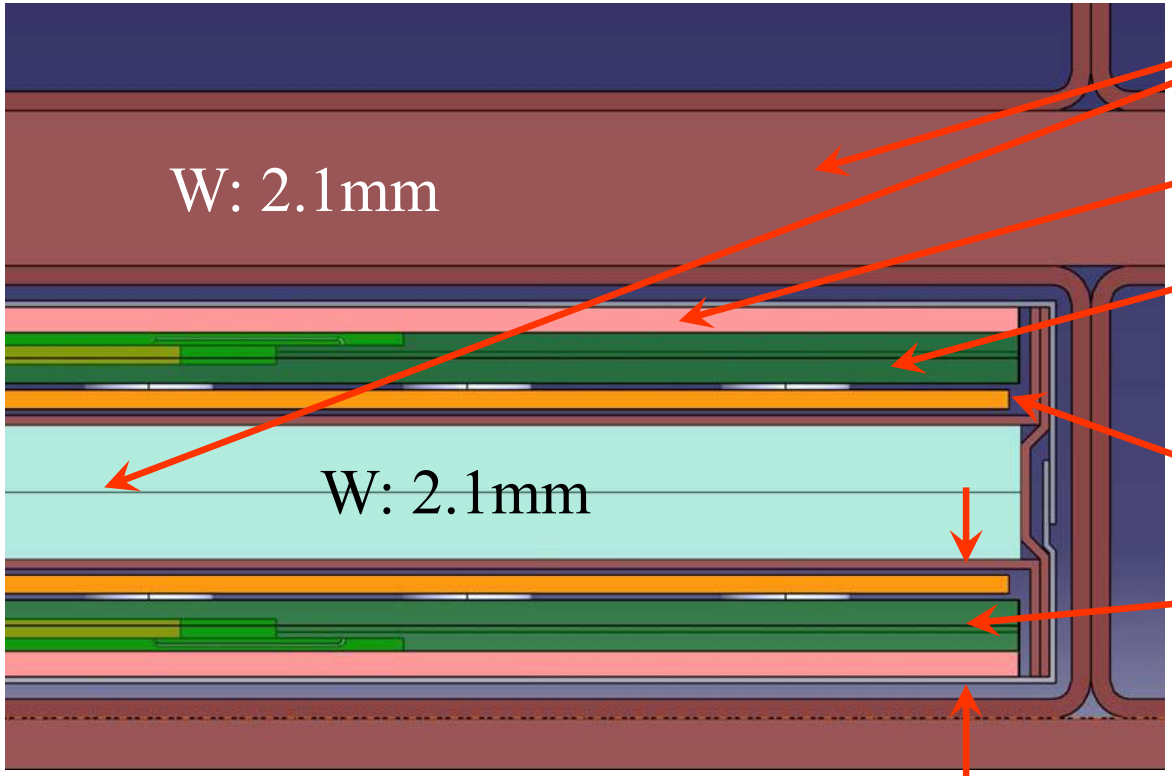


Si-diodes for ILC-ECAL:

thickness	300µm
size	0.5x0.5cm^2
wafer	4" or 6"
channels	80 million

Alternative sensors MAPS:
See G.Villani

ECAL: Electronics in Gap



W-plates: stability

Heat shield: 500µm Cu

800µm PCB
including components

300µm Si-diodes

overall 2.2mm/gap for
sensor + electronics
+ mechanics

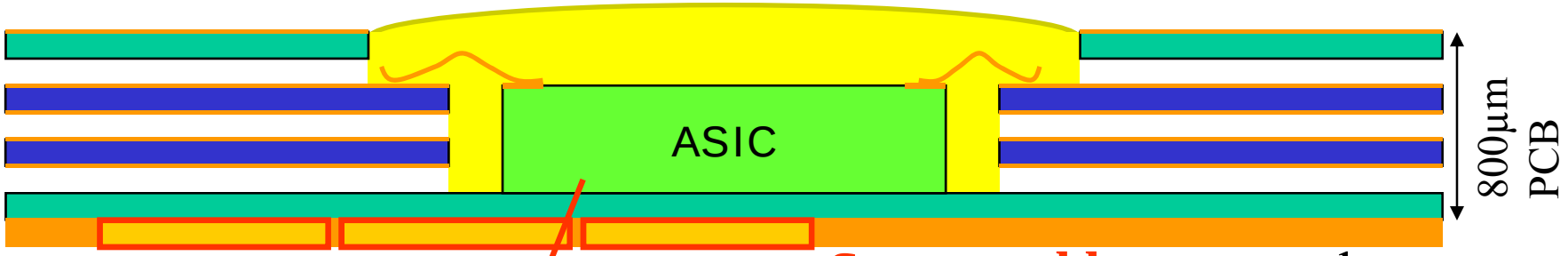
electronics challenging

thin:	2.2mm
long:	1.5m

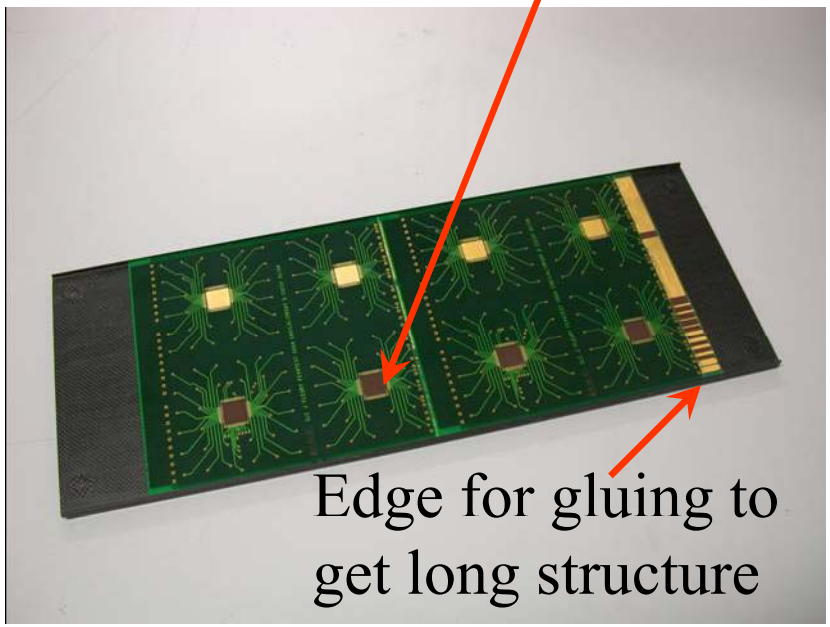
But still small Moliere Radius

pure W:	9mm
whole structure:	~ 14mm

Thin PCB's with Chip inside



Si-diodes on wafer



Staggered layers, so that
- Chip disappears inside PCB
- Chip bonded to two layers
- no additional components

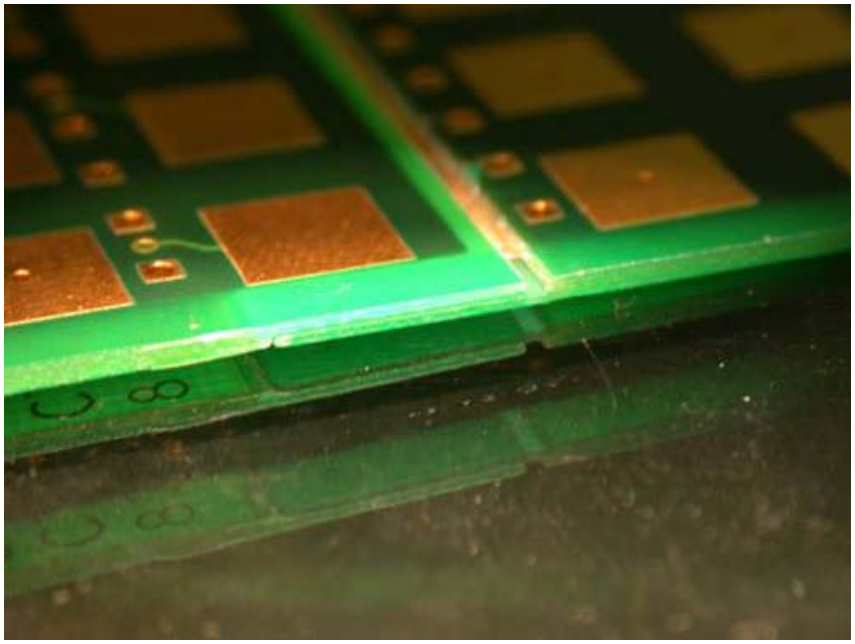
8 Layers in 800 µm
- for shielding
- power-GND filtering
- analog and digital signals

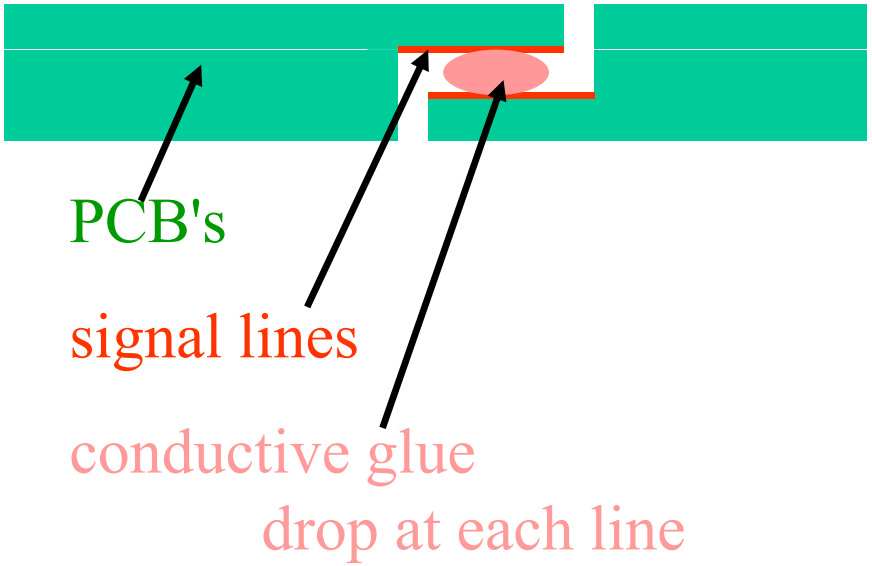
Short board to allow
pre testing, higher yield

ECAL: Long Structure

Technique to get the long structure: Gluing

Known from gluing wafers to PCB's

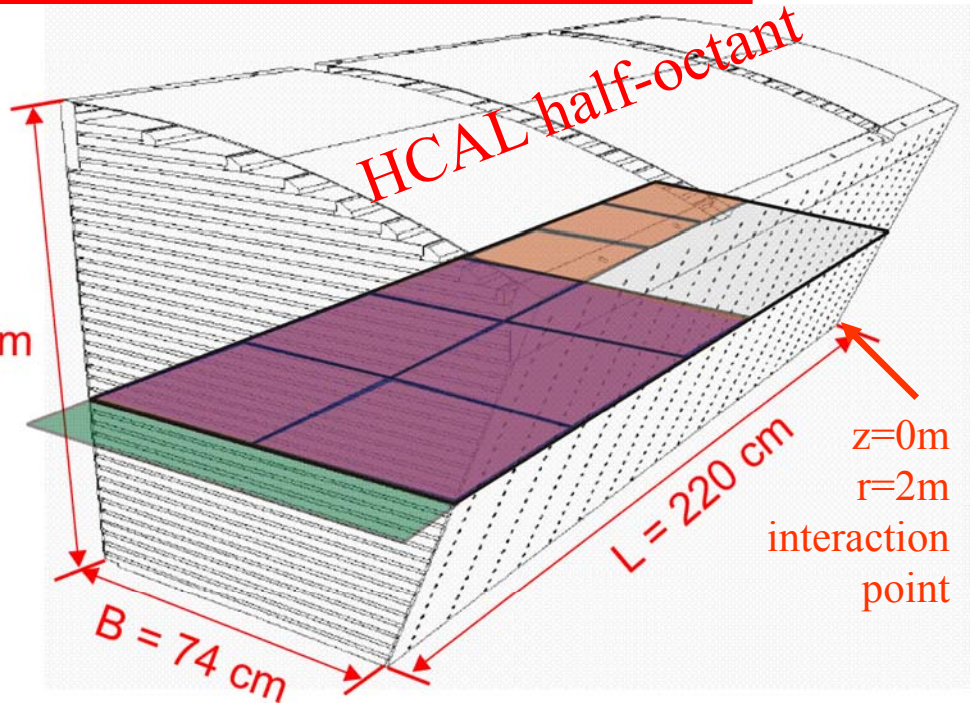




System: HCAL

- even larger volume, longer
- broader spatial resolution
- density not so stringent
- maintenance accessible

►Other technical approach



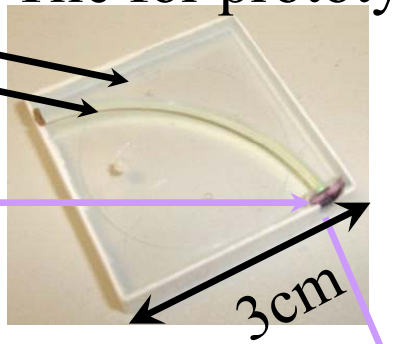
Basic parameters for barrel

- Sampling: Every 2cm of stainless steel
- Sensor size: 3x3cm^2: typically 2200sensors/gap
- 38 Gaps: 32 half octant's: 2.5 million channels
- Inside gap are boards with connectors for plugging while installing
- Room for additional electronics at end plates z=±2.2m

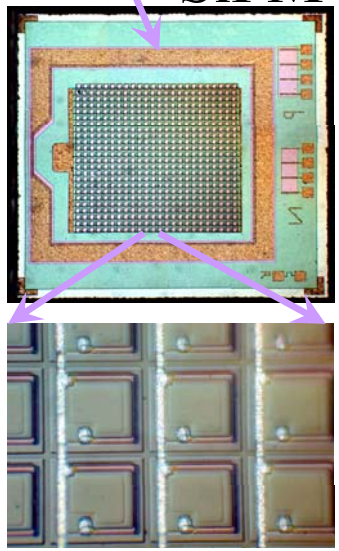
HCAL: The active Media

- Extruded scintillation tiles
- With wavelength shifting fiber
- Small photon detector with gain 10^5-10^6:
  Geiger mode multi pixel diodes
  In physics-prototype of CALICE
  used SiPM from MePhi/Pulsar

Tile for prototype



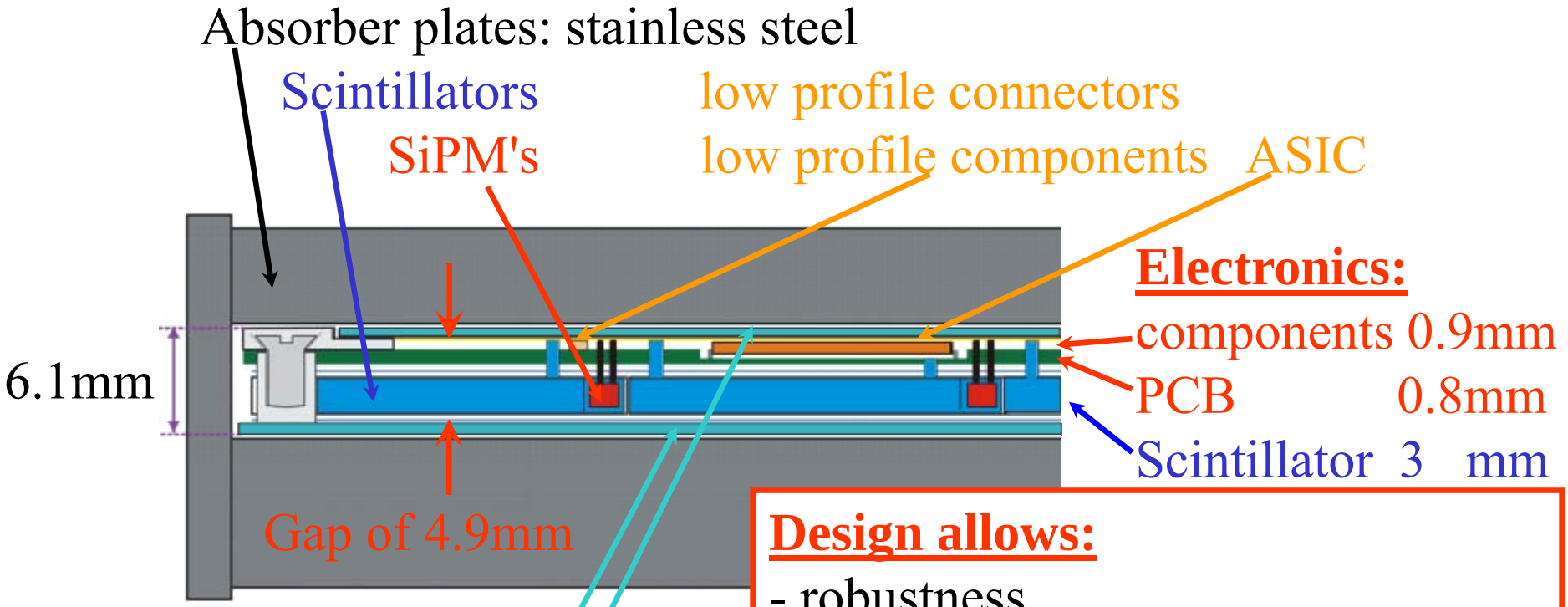
SiPM



For full system design we are studying:

- Mount directly to PCB's by extruded pins
- Need of wafelength shifting
- Solder the SiPM directly to the PCB

HCAL: Electronics in the Gap



Robustness by closed cassettes:
steel counts as absorber,
electrical isolation foil

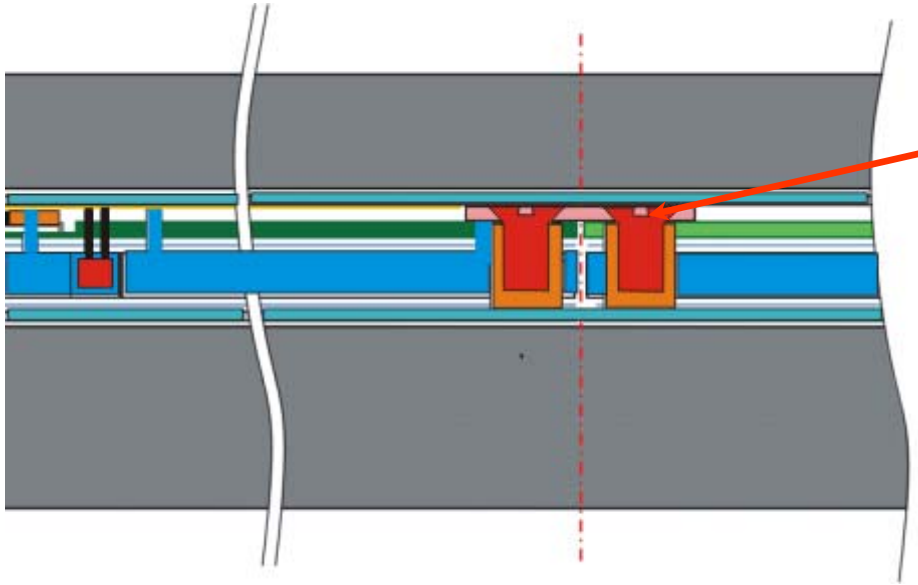
Design allows:

- robustness,
- modularity, even while installing
- pre testing individual components
- maintenance, reinstalling

HCAL: Long Modules

Technique to get long modules:

- manufacture standard sized PCB's: costs and fancy designs
- interconnect boards with thin connectors
- assemble in the lab to reasonably sized modules
- further interconnect in situ while sliding into gap. "repair"



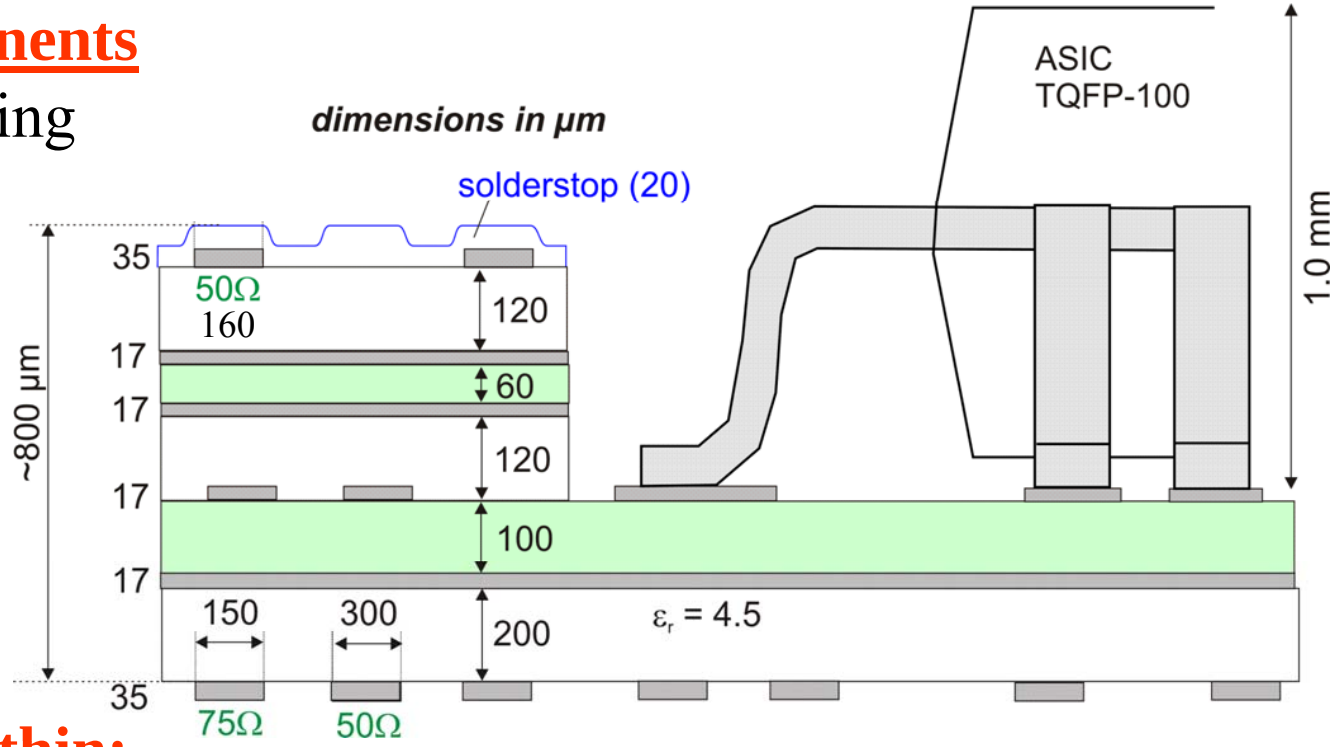
Space for mechanical interconnect
and
small height connectors

Small Component Heights

Additional components

needed for decoupling
for low noise V_{bias}
and supply V
in 2.2m length

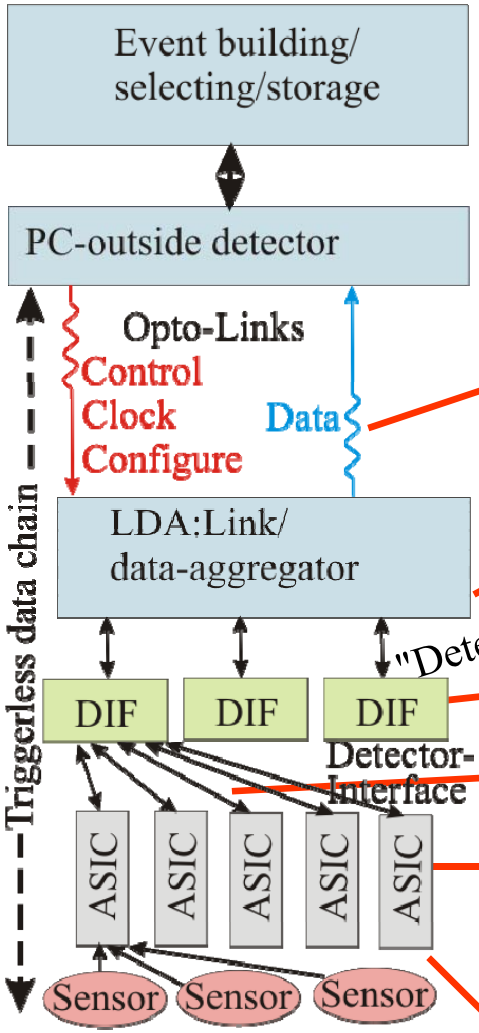
- available
thinness: 700µm



Fanciness to stay thin:

- Thicker ASIC's, connectors soldered to inner layer
- allows low impedance power GND systems
- allows 3 signal layers with two different impedances

General Concept of DAQ



Out of detector:
- data collection, sorting,
no global triggering

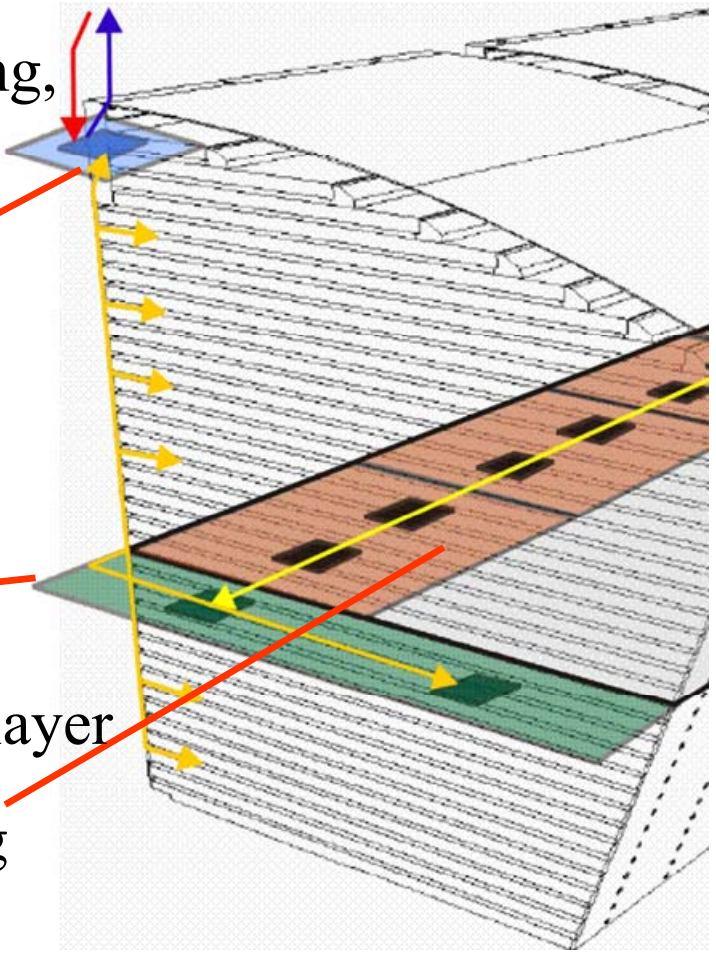
200Mb/s/half-octant

Slow data rate: 5Mb/s/layer

digitizing, multiplexing

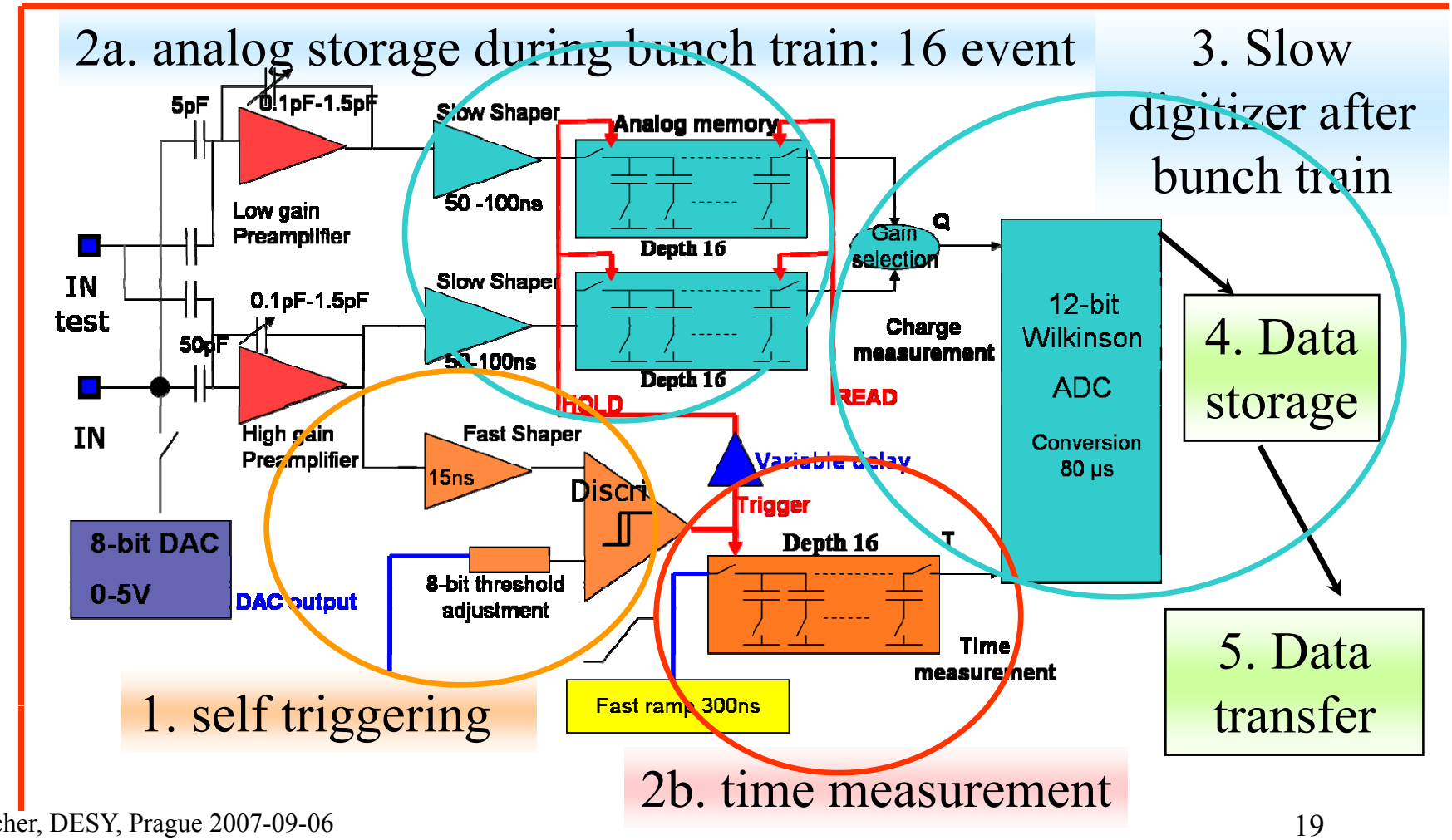
Analog handling

Self triggering of each sensor



DAQ: In-Gap Functionality

All functionality is in one ASIC One ASIC/36channels



More as posters: 06-Sept. by F. Dulucq, L. Raux
as talk 07-Sept. by J. Freury
yesterday: by N. Seguin Moreau

DAQ: In Detector Electronics

In detector are:	Detector Interface	per layer
	Link/Data-Aggregator	per module

Tasks

"Local distribution and aggregation to minimize cable"

- Providing control signals to multiplex a row of ASIC's
- Data readout during full 199ms break between the trains
- Distribution of clocks for synchronization to bunches
- Storing and distribution of power
- Slow monitoring, boot and control

Technique:

- FPGA with
  - -opto-Link's to an external PC
  - - user-defined bus to ASIC's

Calibration

Calibration is essential for the use of a calorimeter
it has to be designed into the system

- Aim: 1% for each channel

- Most critical: gain of Geiger-Mode-diodes:
  $(dQ/dV_{bias})/Q \approx 70\%/V_{bias}$ $(dQ/dT)/Q \approx -4.5\%/K$

  Needs measurement of environment,
  but also fast gain monitoring.

- Electronics calibration: Charge injectors to input of ASIC

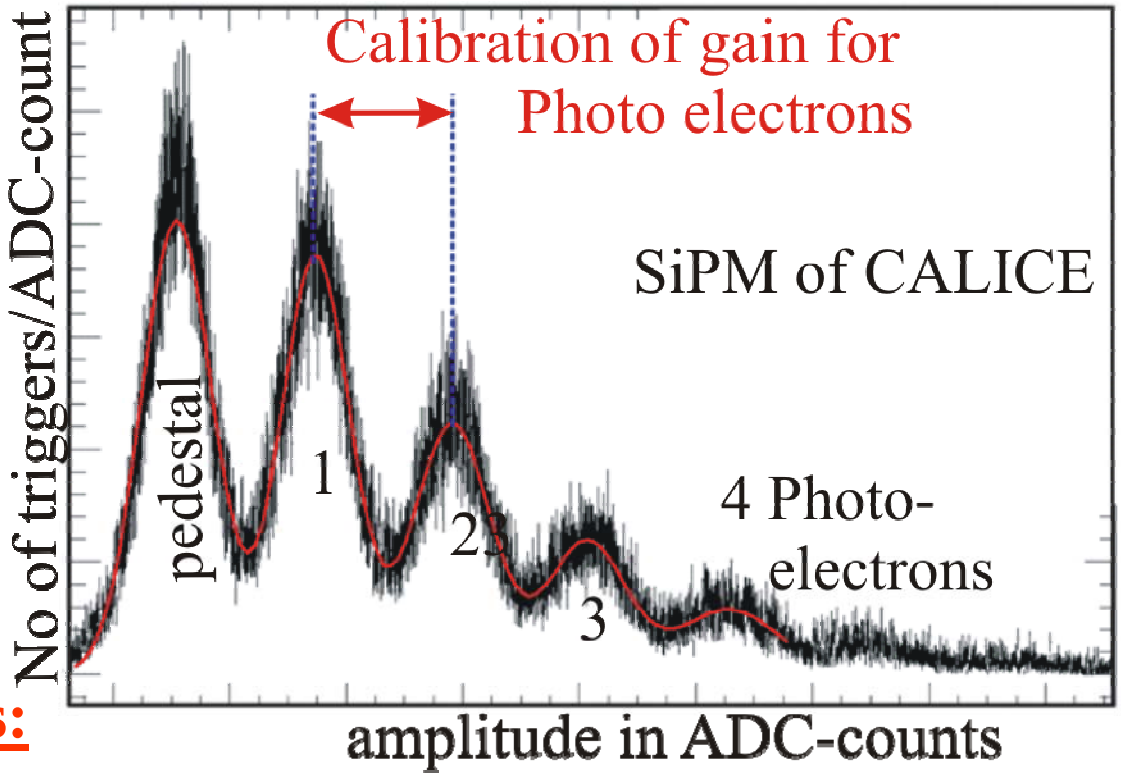
- Long term physics minimum ionizing particles
  Mass reconstruction of particles

Calibration of multi Pixel Geiger Mode Diodes

Use:

Noise and pixel-fluctuations good enough to see

- peaks of single pixel hit by photon or self generated electron/hole



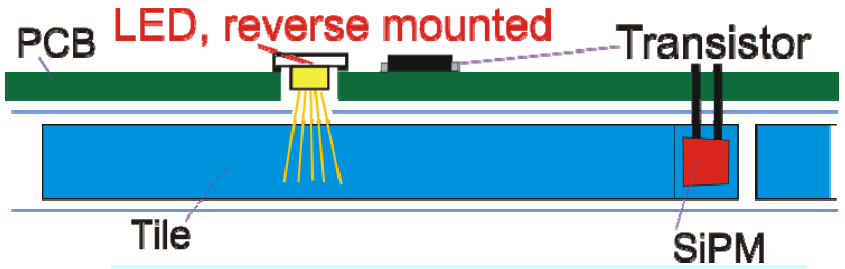
Requirement to electronics:

- Self-trigger on 1/2 Photo-electron
- triggered light sources, triggering also DAQ

Calibration: Light Source

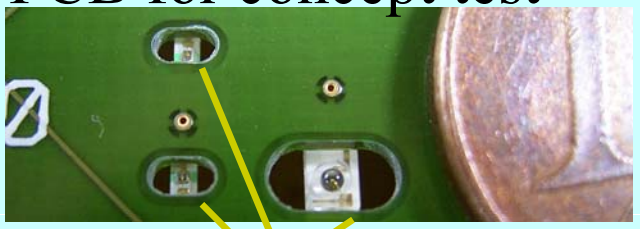
Under study: What is feasible, easy and cheap?
Some components have to be located
in the already filled up detection gap

1. Version: Now used for test beam
   Strong LED's but still timed to nano-seconds
   Worries: Fiber to each pad
   Source outside the gap



2. Version: LED per scintillator tile
   pulser nearby photo sensor
   small pulses to LED
   EMI-crosstalk solvable?
   power-GND-system in PCB?
   Easy assembly: LED in hole of PCB

PCB for concept test



LED's 1cent-€

Power Cycling

Why: Avoid active cooling inside detection gaps
expensive, risky, space

Possible: Due to train bunch structure 1ms every 200ms
2ms = 1% "ON"-time required,
- including time for digitization, stabilization
- whole time ON, while analog signal processing

Aim: 25µW/channel for DAQ-electronics in the gap
First ASIC design is submitted

How: ASIC switches on control signal
- fast high power analog part ON/OFF
- low power in digital by slow continuous transfer

Needs: Power distribution handling fluctuations in current

Power Cycling: Parameters

Single channel

Mean current/channel	7.5μA/channel
Peak current/channel	750μA/channel

HCAL typical layer has 2200 channel/half-octant

Mean current per layer	17mA/layer
Peak current per layer	1.7A/layer

Total mean current for gap electronics in sub detectors

HCAL-barrel:	2.5M channels	20A
ECAL, total	80 M channels	600A

► Total mean currents looks not critical due to power cycling

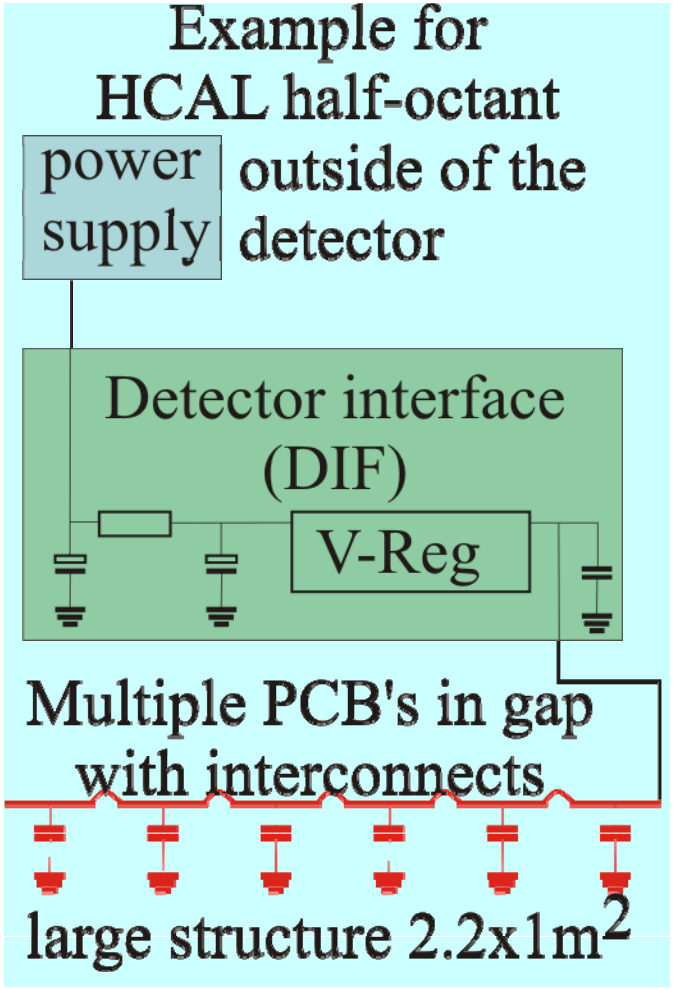
Power Cycling: Concept

Estimation of the effort and feasibility

Actors are the ASIC's themselves,
the power electronics has to react

Aim: Keep fluctuations locally
best inside subcomponent

- ► limited EMI-problems,
  W,Fe-plates act as EMI-shield
- ► thinner power cables
- ► outside only DC-currents
  - nice for commercial supplies
  - no disturbance to others



Idea: Buffer charge inside the gaps and at end of the gap

Capacitance inside the Gap

Parameters of 2.2 long PCB structure:

- signal speed : 15ns from end to end
  also fastest time to take charge from the DIF

- layer-layer distance for power-GND of 60µm 70pF/cm^2
  capacitance per 9cm^2 channel: 0.6nF/channel
  per ASIC: (36channels) 20nF/ASIC

That is for free and does the HF-filtering of any switching

Voltage drop by the first 15ns each channels:

$$\Delta V = \frac{750\mu A/channel \bullet 15ns}{0.6nF/channel} = 19mV$$

► Better discrete capacitors of 500nF/ASIC ► ΔV<1mV
available as 3 pieces á 220nF with height 650µm

Resistance inside the Gap

The 2.2m long structure: composed out of 6 small sized boards:

Each connection has a resistance of typically 10mΩ/pin
Factor 2 for GND and Power line

Peak current was 1.7A/layer at begin of layer
Factor 1/2 because of distributed consumers

Voltage drop per used pin:

$$\Delta V = \frac{10m\Omega}{pin \bullet connection} \bullet 6connections \bullet 2 \bullet \frac{1.7A}{2} = \underline{\underline{100mV}}$$

Its no critical: It is DC, does not vary during the bunch train.

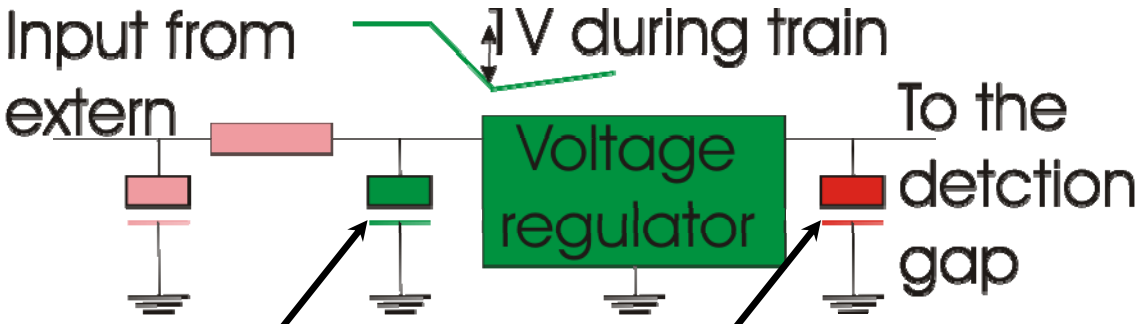
Multiple parallel pins is not a problem: around 10pins for 10mV

Charge Storage at DIF

Concept: Two stages of charge storing:

- For fast stabilization (1µs) C after V-regulator
- For slow (2ms) C before V-regulator

Resistor for stabilization of input current



For 1V in 2ms:
3.4mF
10 SMD tantal

For 5mV in 1µs:
340µF as
40 large ceramic

Additional heat

- not critical position
  - 1V for dynamic
  - 1V at regulator
  - 0.5V at resistor
  - current 17mA

► 45mW/layer,
low, OK!

Not problem for a 1m long DIF

Cooling

Aim: No active cooling inside the calorimeter volume

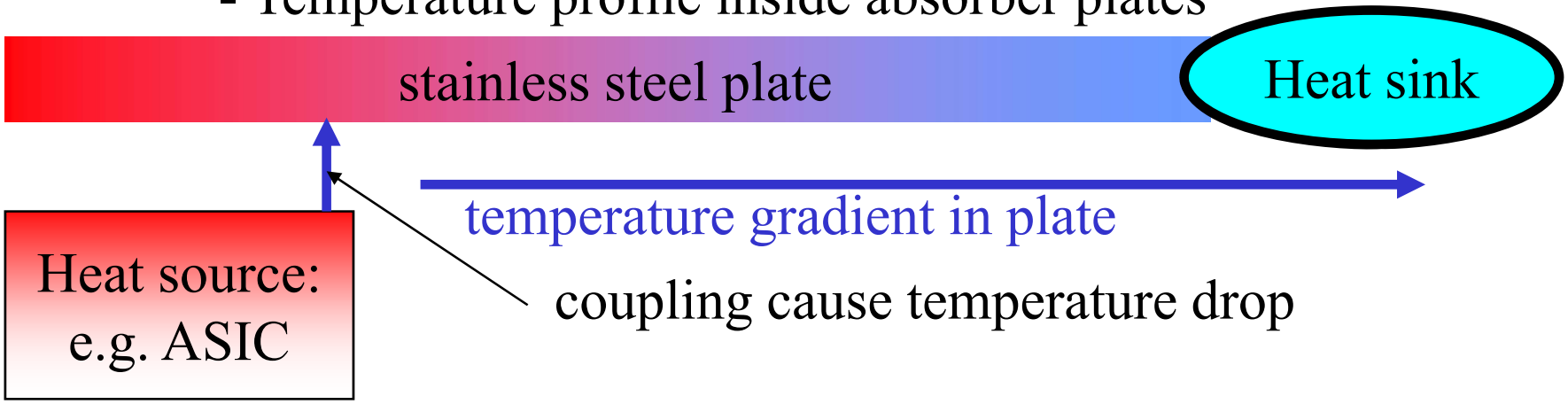
Reasons: space, costs, risky

Heat transfer

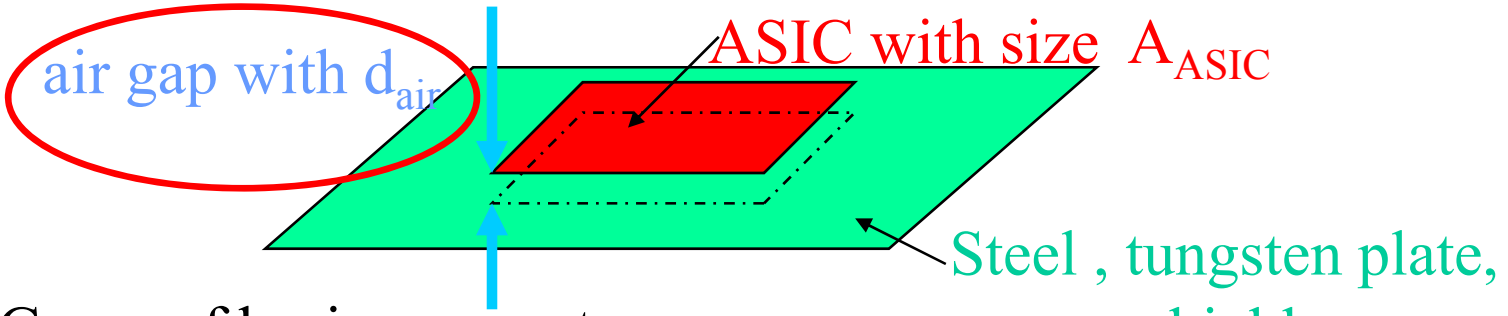
- mainly in metal plates: absorbers, heat shields

To be looked at:

- how does the heat get into the plates?
- Temperature profile inside absorber plates



Heat Transfer: ASIC to Metal Plate



Guess of basic parameters

λ_{air}= 24mW/Km (Nitrogen)

A_{ASIC}= 4cm^2 effective area for transport

d_{air}=1mm

P_{ASIC}=(36channel)*P_{chan}=0.9mW

Temperature difference at air gap: without convection (small gap)

$$\Delta T_{gap} = \frac{1}{\lambda_{air}} P_{ASIC} \frac{d_{air}}{A_{ASIC}}$$

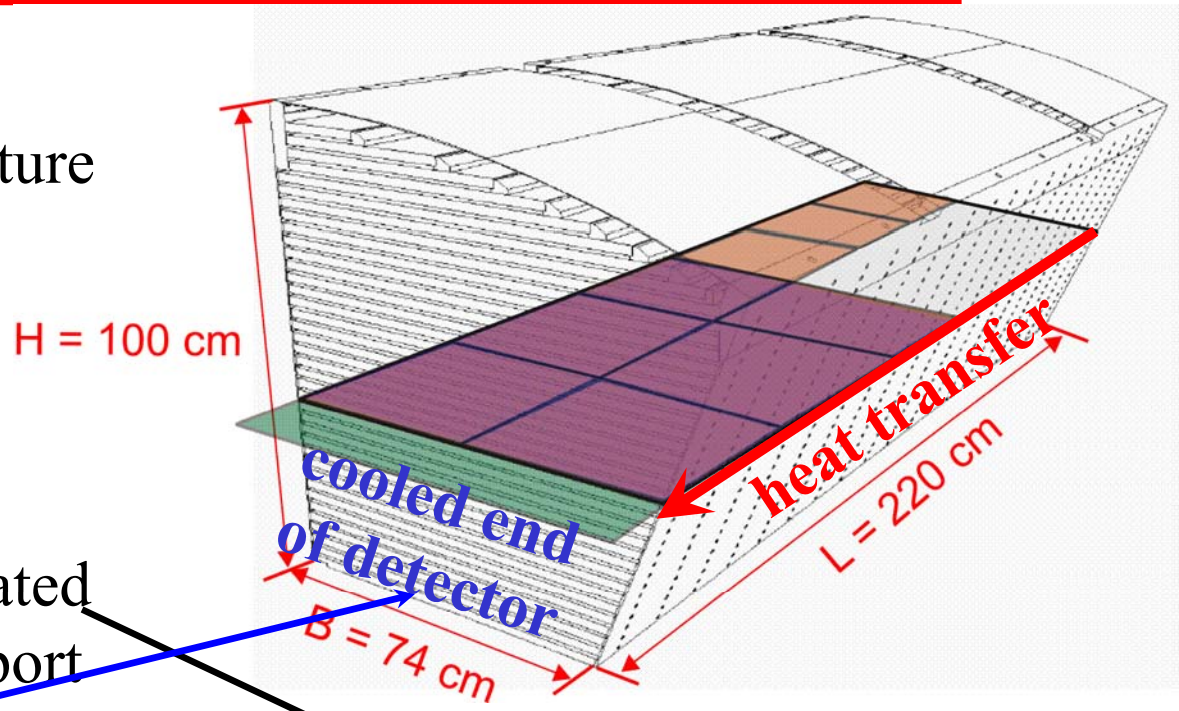
➡ ΔT_{gap} = 0.1K OK, due to low power!!!!!,

Easy mechanics: No touching needed

Cooling: HCAL Calculations

No radial heat transfer
due to sandwich structure

No heat transfer in φ
rough symmetry



Simplified geometry:

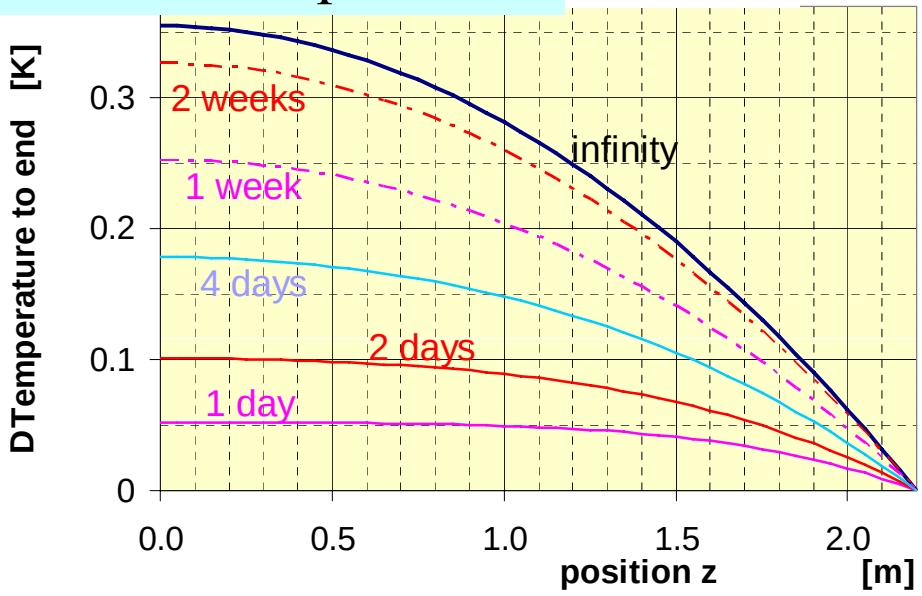
- plate homogeneous heated
- one-dimensional transport
- cooled at 2.2m
- symmetry at z=0

1100channels/m^{2*}
(25μW/channel ASIC
+ 15μW/channel) V_{bias} of SiPM
= 44mW/m^2

HCAL: Heat Transport in Absorber

Energy conservation, heat flow ~ grad(T): linear diff. equation

$$T(z,t) = \frac{\frac{Power}{area}}{2\,\lambda\,d}\left\{(L^2 - z^2) + \sum_{\alpha=1/4,3/4,5/4\ldots} A_\alpha e^{-t/\tau_\alpha}\cos\left(2\pi\alpha\frac{z}{L}\right)\right\}$$



time constants: α=1/4, 3/4, 5/4,.....

slow !

days 5.6, 0.6, 0.2.....

Parameters: (stainless steel)

heat conductivity: λ=15W/Km

heat capacitance: 3.7MJ/m^{3}K

Geometry:

Length of calorimeter: L=2.2m

thickness of absorber d=2cm

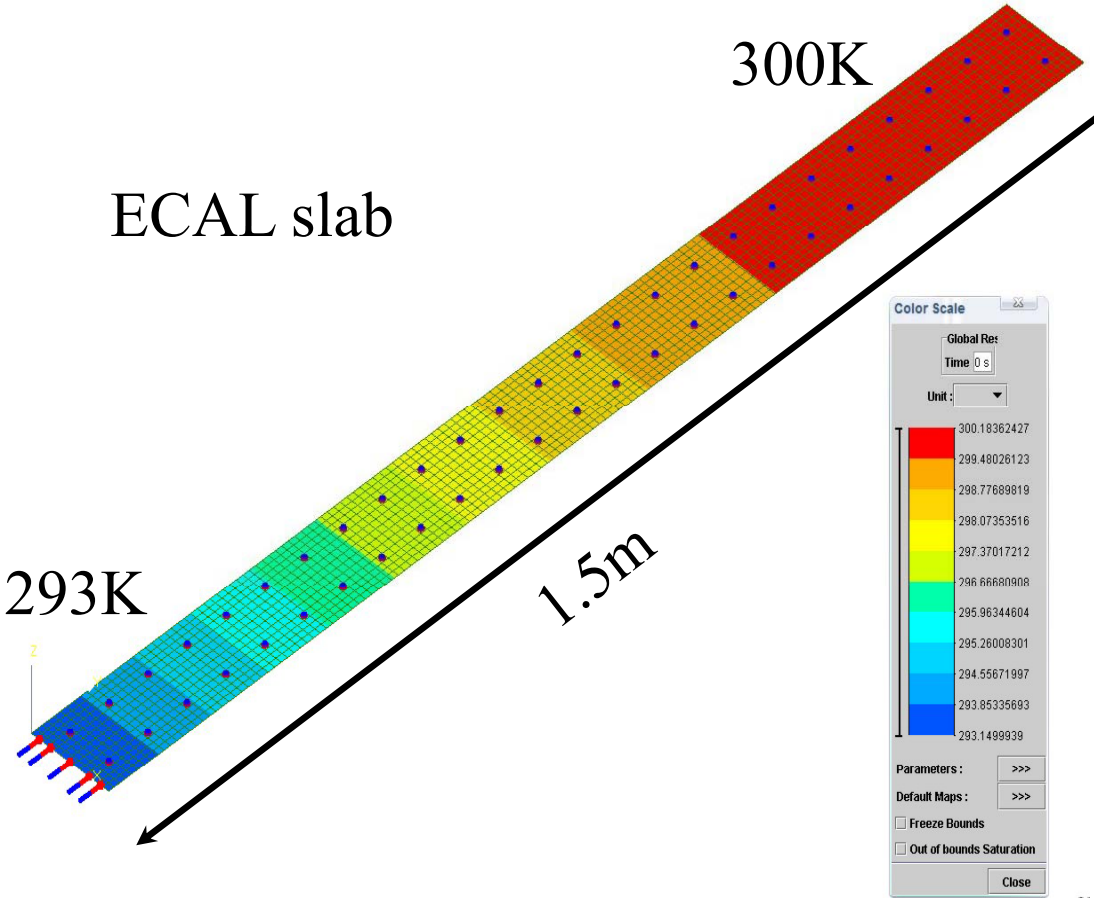
power/area = 44mW/m^2

Result: 0.36K is tolerable

SiPM gain will vary: 1.6%

but slowly, possible to calibrate

ECAL: Temperature Profile



Pessimistic estimate:

Heat transfer just in
- 500µm copper shield
- Tungsten is ignored

Result: 7K is OK.

Conclusion: Active cooling inside detection gaps is for E/HCAL avoidable by power pulsing and low power ASIC's

Outlook

- **Prototype** to test particle flow algorithm is at test beam
  Results will come, Prove of individual components
  ► influence the design
- **ECAL and HCAL system's for ILC** have been presented
  Dense calorimeters, high granularity, ► 100 million channels
  ► to be converted to technical prototypes
- **Alternative techniques** are under development
  e.g. ECAL: W-scintillator-SiPM ►took data at DESY-beam
  HCAL: Fe-RPC-digital readout ► took data at FNAL-beam
- **Power cycling, low power ASIC** are essential/promising ►25µW/ch
  to avoid active cooling in calorimeter gaps.
  ► experiments for thermal/electrical

Another ILC-talk tomorrow
by Marcel Demarteau

Thanks
to
CALICE
Calorimeter for ILC
and for your attention