

System aspects of the ILC-electronics and power pulsing

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Abstract

The requirements for the electronics of an experiment at the international linear collider (ILC) are driven by the bunch structure of the accelerator - short trains (1ms) with bunch to bunch lag of $0.3\mu\text{s}$ interrupted by long empty intervals (199ms) - and the precision physics. Based on developments of the CALICE-collaboration a system for high granular dense calorimetry is presented. The talk covers the system aspects

- of compact sensors as Si-diodes and multi-pixel Geiger mode photo sensors,
- of the electromechanics with components embedded into the PCB's,
- of integrating the functionality needed nearby the sensor into low power ASIC's,
- of a DAQ-chain, in which each channel triggers on its own and the data selection is installed into PC's and
- of calibrating the calorimeter.

With the high number of 100 million channels the power consumption and cooling have to be investigated carefully. Calculations demonstrate, that active cooling inside the calorimeters can be avoided. But essential for this goal is using the low duty cycle (0.5%) of the accelerator to power cycle the major consumers and designing an ASIC for low power ($25\mu\text{W}/\text{channel}$). For the power cycling a concept is developed, which keeps the current fluctuation local to avoid EMI-problems and to supply the in-detector electronics with DC-current through wires with moderate cross section.

Some of the ideas are already realized in a prototype for physics and component studies. The setup integrates 14 thousand channels and was installed for two month at CERN-testbeam. 200 million of electrons and pions are collected and 15T-Byte of data are stored. The data nicely show the details of a shower development needed to prove the particle flow algorithm for high energy resolution.

I. GENERAL CONDITIONS FOR THE ELECTRONICS DEFINED BY ACCELERATOR AND PHYSICS

In the accelerator ILC electrons and positrons will collide at energies above 0.5TeV. This allows high precision physics with heavy particles, but the electrons and positrons interact at low rate. Due to the superconducting acceleration the bunches are packed into 1 ms long trains interrupted by long empty periods of 199ms. During the trains the bunches are separated by $0.3\mu\text{s}$.

By using these features in the electronic design the system can be kept adequate and at some stages simple. From the electronics it is requested to follow the fast bunch-to-bunch structure ($0.3\mu\text{s}$) and even provide faster pulse analysis for signals,

for which time information improves the energy measurement. But fast signals appear only during the trains - 0.5% of the time. For the rest of the time the fast electronics is not needed. The data acquisition system can take the low occupancy and the long breaks between the trains as opportunity to minimize the infrastructure inside the detector.

The physics of e^+e^- -collisions on the TeV-scale also defines requirements for the design of the detector. To reach the aim for high precision measurements of the properties of the heavy particles new concepts and technologies have to be developed. As case study the decay chain of heavy particles into vector bosons and further into jets is used to formulate the detector requirements.

$$t, H \rightarrow Z, W \rightarrow \text{leptons or jets}$$

The detector design aims for distinguishing the involved vector boson by reconstruction of its mass even from the jets. This needs tracking, vertex detection and a high energy resolution even for jets:

$$\frac{\Delta E_{jet}}{E_{jet}} = \frac{30\%}{\sqrt{E_{jet}}} \quad (1)$$

To reach that goal a concept is studied to measure each individual particle of the jets and add the energies together to get the jet energy E_{jet} - the so called "particle flow algorithm" [1]. For charged particles the momentum measurement is more accurate while photons and neutral hadrons can only be measured by the electromagnetic or hadronic calorimeter.

Hadronic showers develop electromagnetic and hadronic sub-showers with different calibration constants. Therefore the CALICE collaboration aims for identification of these sub-showers and use them for e/h -compensation and for improving the energy resolution. Even identified neutrons by delayed energy deposition (few ns) is an idea to improve the energy resolution.

That translates into the requirements for the detector design:

- Separate the particles from each other before they hit the calorimeter.
That requires a large magnetic field and a large radius for the tracking.
- Track particles inside the calorimeter.
That requires a high granularity (100 million channels), small shower sizes within dense calorimeters and ns-timing to identify delayed processes.

e^+e^- -accelerators only generate a low radiation dose. So damages of the electronics caused by radiation are no issue for the major parts of an ILC-detector.

II. PROTOTYPE AT TEST BEAM

In the last years prototype calorimeters have been built for an electromagnetic (ECAL), an hadronic (HCAL) calorimeter and a tail catcher. They are constructed with similar absorber layers (W, stainless steel, Fe) and analogue readout sensors (Si, scintillators tiles, scintillator bars) as proposed for an ILC-detector and will be described in the following sections. Also alternative techniques with scintillators or Si-pixels[2] in the ECAL or resistive plate chambers for the HCAL are under development and have collected first test beam data.

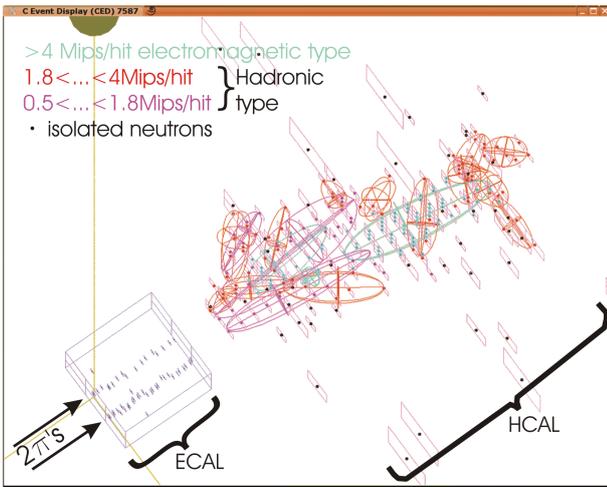
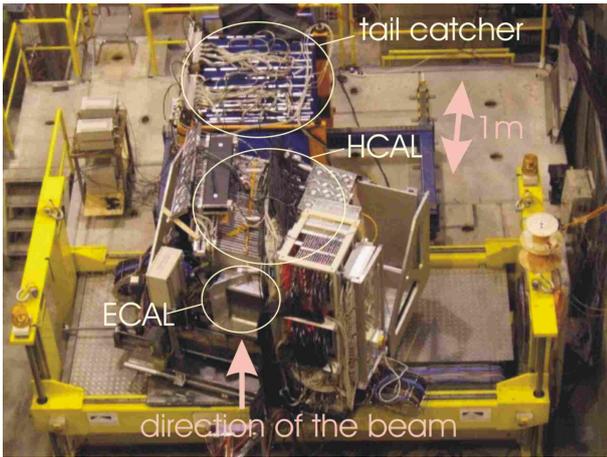


Figure 1: A test beam setup at CERN-SPS with an ECAL, HCAL and tail catcher.

Top: Setup on a movable stage allowing vertical and horizontal movements, rotating and sharing.

Bottom: An event of 2π 's hitting the setup. They deposited energy as minimum ionizing particles (Mip), as sub-showers of different densities and as spreading around neutrons.

At the CERN-SPS the three types of calorimeters have been located behind each other (figure 1-top). The readout was organized as common data acquisition system using the same type of electronics based on ASIC's with similar architectures[3]. During two months of operation 200 million particles and 15TByte of data have been recorded. A first look to the data shows al-

ready that details can be identified. Figure 1-bottom is a reconstruction of 2 pions hitting the calorimeter in the same event at a distance of 6cm. They passed the ECAL as minimum ionizing particles without any shower and generated in the HCAL high density showers of electromagnetic type, low density showers of hadronic type and isolated neutrons. These are the details needed to distinguish showers from nearby jet-particles and to compensate the different response to electrons and hadrons by software reconstructing and reweighting the sub-showers.

To see all these details the test beam setup has already 14 thousand channels and looks like an experiment on its own. In these prototypes of the calorimeters the electronics is located on the side of the active area, which would cause dead areas in a 4π -detector. Therefore to realize an ILC-experiment the system needs further developments and ideas, which will be described in the following sections.

III. SYSTEM DESIGN OF THE ELECTRONICS FOR THE HIGH RESOLUTION CALORIMETER

A. General concept

By the requirements described in section I the inner diameter of the calorimeter is defined by the tracker to be large. In order to have a low amount of dead material in front of the calorimeter the coil is situated around the calorimeter. Since the coil is expensive, its diameter and so also the outer diameter of the calorimeter is forced to be small. This geometry is sketched in figure 2 and indicates the contrariness of the two requirements.

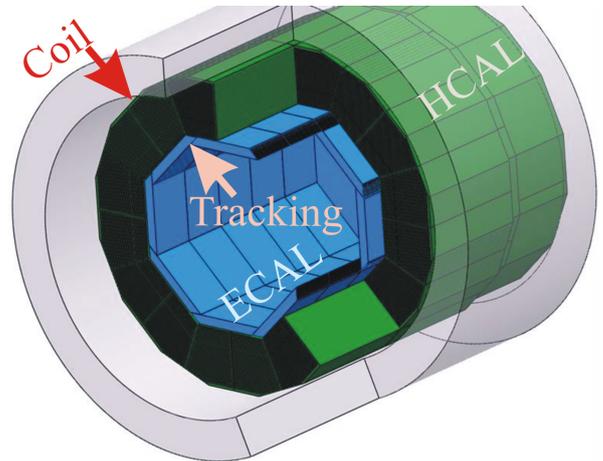


Figure 2: The geometry of a calorimeter inside an ILC detector

Therefore a dense calorimeter has to be constructed with high granularity (100 million channels). The CALICE-collaboration studies sandwich calorimeters with tungsten (W) as absorber for the electromagnetic calorimeter (ECAL) and stainless steel for the hadronic calorimeter (HCAL). To keep the calorimeter dense, the detection gap with active sensors and with electronics needs to be designed as thin layer. Electronics nearby the sensors is needed to allow a high granularity without

huge volume for the signal transfer. As consequence electronics has to be mounted inside the detection gaps.

These constraints for the calorimeter can be translated into requirements for the electronics:

- The first stage - the very front end (VFE) - has to be situated inside the detection gap close by the sensors and located inside the particle showers.
- A compact VFE is needed and requires the development of ASIC's.
- The VFE has to multiplex control and signal lines, to avoid huge routing of wires.
- Only small simple infrastructure e.g. cooling is allowed.
- Larger components have to be located at the end plates or into cracks as "end-gap" modules.

B. Electromechanics of the ECAL

The whole calorimeter is proposed as octagon (figure 3) with a length at the inner radius of 1.5m. The electromagnetic calorimeter (ECAL) is subdivided into trapezoid modules along each side of the octagon.

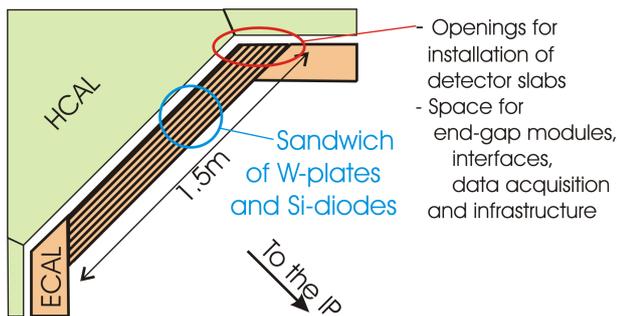


Figure 3: A corner of the octagonal calorimeter construction. The direction to the interaction point is the bottom right corner.

The ECAL is proposed as sandwich structure out of 29 absorber layers of 2.1mm thick W-plates. The sampling layers in between will house 80 million silicon diodes with a size of $0.5 \times 0.5 \text{ cm}^2$ and a thickness of $300 \mu\text{m}$. Since the edge of the octagon is shorter than the dimension along the beam line, a mechanics is foreseen, which allows access to the modules from a small surface of the trapezoid facing the outer surface of the octagon. This surface contains the openings to install 1.5m long slabs into a support structure and to connect all electrical signals so that the cabling is behind the ECAL. The installation of the slabs will have to be completed before the ECAL-modules are mounted to the surrounding HCAL.

The design of the slab (figure 4) has to aim for very thin layers of non-W material to keep the shower radius small and to optimize the separation of nearby particle showers. The stability of the slab is reached by building two detection layers around a W-plate. Any electrical connectivity is designed into $800 \mu\text{m}$ thick PCB's. Additional heat shields out of copper improves the heat transfer to the end of the slabs.

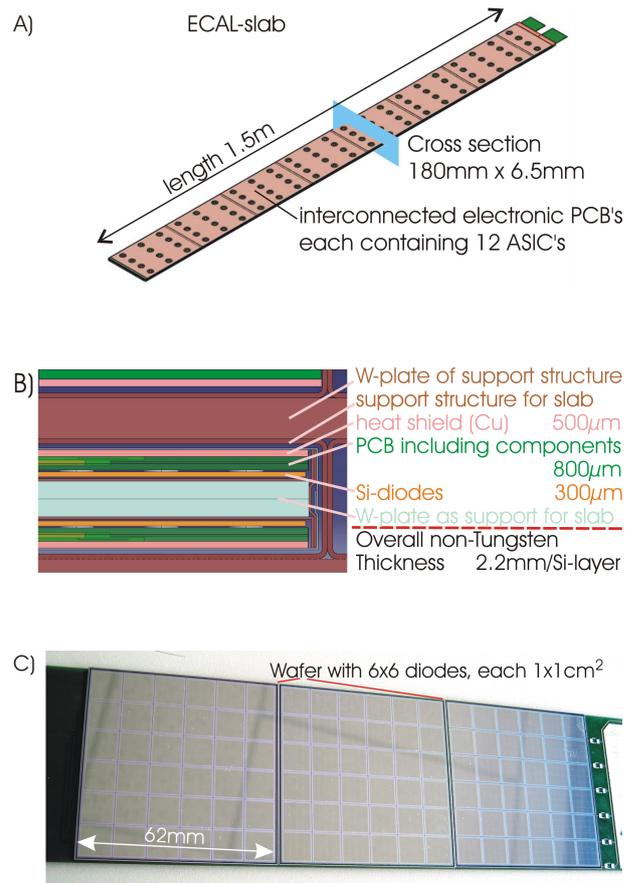


Figure 4: The ECAL-slab with its sensors and electronics. A) A three dimensional sketch B) A cross section of the slab at the indicated direction showing the internal composition C) The slab for the prototype used now in the test beams

The thin design of the gap does not allow additional height of the components in the VFE. Therefore they have to be embedded into the PCB (figure 5). Space for the ASIC's is gained by staggered layers, gluing the ASIC's to a lower layer and bonding of the die to an inner layer. That solution does not allow for additional components because the assembly would be expensive. So every functionality has to be provided by the one ASIC and any power-filtering has to be realized by the 8-layer structure of the PCB. The thickness of $800 \mu\text{m}$ is sufficient to support shielding, power-GND-filtering, analog and digital signal lines. To keep the yield of that special technology high the PCB's are kept at reasonable sizes and tested before assembling to large units. The 1.5m long structure is obtained by staggered edges at the PCBs and fixing them together with a drop of conductive glue on each signal line (figure 5).

The described electro-mechanic design with all its complication increases the Moliere radius of the shower just from 9mm for pure W to $\approx 14 \text{ mm}$.

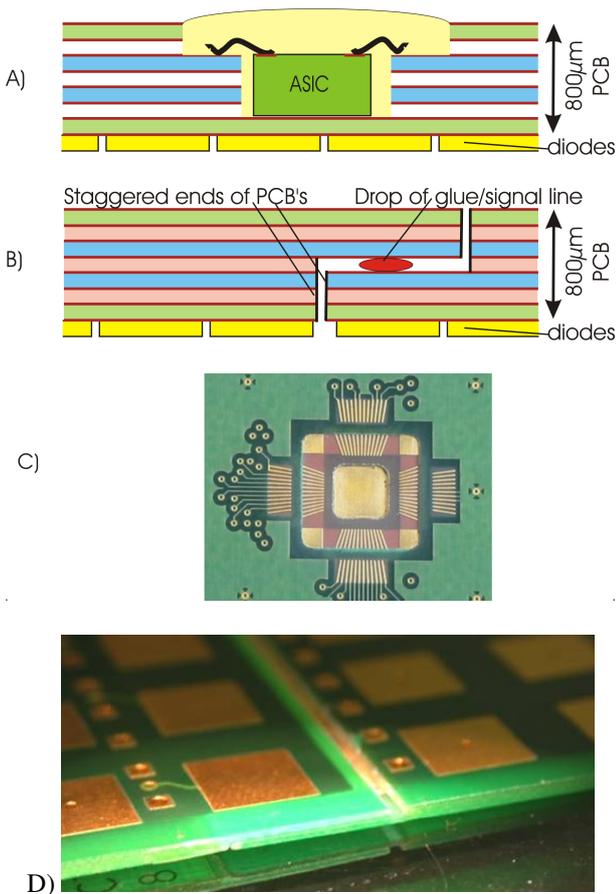


Figure 5: PCB's for the ECAL:
 (A) with embedded components,
 (B) glued together signal line by signal line to gain length without thickness increase,
 (C) a photograph of a test board with embedded ASIC's and
 (D) a photograph of the interconnection technique

C. Electromechanics of the HCAL

In the hadronic part of the calorimeter (HCAL) geometrical volumes and dimensions are larger and the showers spread wider, so that the constraints to sensor size and density are not so stringent. For the barrel part the end plates at $z=\pm 2.2\text{m}$ (z is the beam axis, with $z=0$ at the e^+e^- -interaction point) are accessible for maintenance and the HCAL-design should make use of it to keep the best long term performance.

The central part of the mechanical design consists of self supporting stainless steel half-octants (figure 6) with gaps, in which the active sensors together with the VFE can be slid in and out. The shower will be sampled after each 2cm of steel by $3\times 3\text{cm}^2$ sized sensors. Each gap in an half-octant has an area of typically 2m^2 and houses 2200 sensors. For the total barrel calorimeter that adds up to 2.5million channels and requires the use of ASIC's concentrating the functionality of the VFE into one chip. Thick components can be located at the end plates as "end-gap" electronics. The in-gap units are designed with standard sized PCB's pre-assembled in the workshops to reasonable sized modules. The full 2.2m length is achieved by sliding

a module into the gap and interconnect the next one mechanically and electrically with thin connectors before it is also slid into the gap. This allows later disassembling and re-installation, even if the endcap of an ILC-detector will not keep the full 2.2m clearance to pull out the electronics of one gap in one piece.

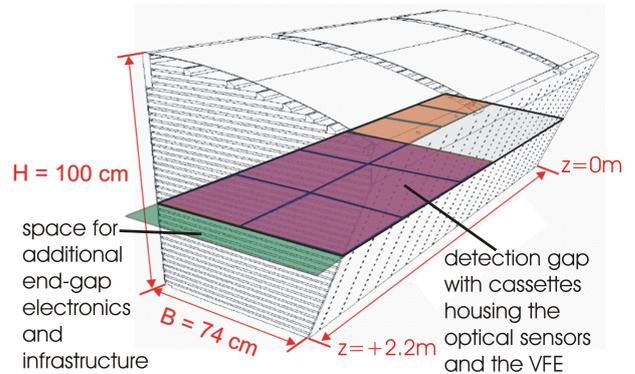


Figure 6: A half-octant of the HCAL, with the accessible end plate in the front of the picture and the symmetry at the interaction point on the back ($z=0$). For one detection gap the individual mechanical units are indicated and in the front the green part is for electronics outside the gap

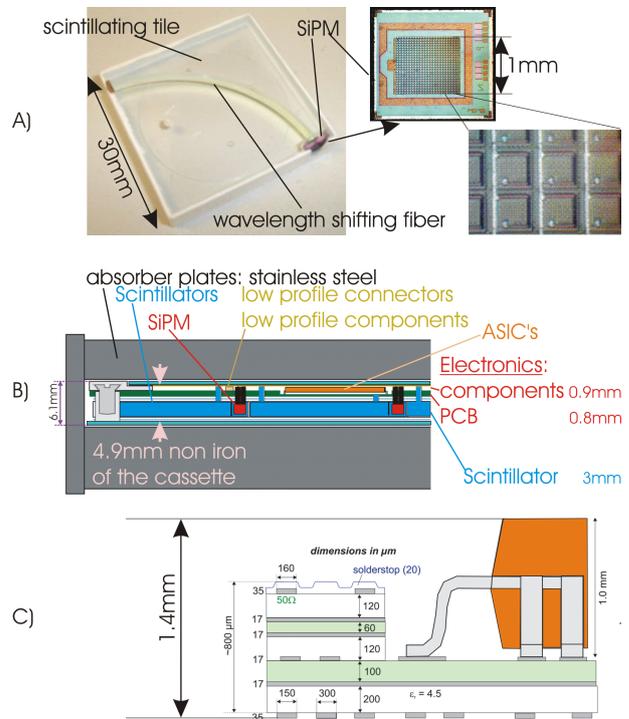


Figure 7: Components and design of the detection gap for the HCAL with scintillator readout
 A) A scintillator tile of $3\times 3\text{cm}^2$ with its optical readout components of a green wavelength shifting fiber and a SiPM [4] with its visible pixels
 B) Design of the detection gap
 C) Soldered components embedded into the PCB for a thin structure

As cost-effective technology for the sensors 3mm thick scintillator tiles can be molded. For a physics prototype they had been equipped with a wavelength shifting fiber (figure 7) to guide the light to a small photo detector. That technique is possible for such a high granularity calorimeter only since the multipixel-Geiger-mode diodes are available in large quantities. For the physics prototype 7608 SiPM's from MePhi/Pulser[4] are installed. For a final calorimeter studies are going on to ease the assembly. Molded scintillators already with pins for plugging them into the PCB or soldering the SiPM directly to the PCB are under investigation.

The density of the calorimeter is maximized by designing cassettes (figure 7) for the detection gap so, that the thickness of the materials other than stainless steel is minimized. Since the cover plates can be produced out of stainless steel only the inner height of 4.9mm counts as non absorbing material. The tolerances for sliding the cassettes into the gap, which have to be defined at a later stage, might add another millimeter. The components and its heights for the design of the cassette are shown in figure 7. A closed cassette with stainless steel cover plates and isolation foils to the electronics can guarantee the robustness. The active sensors take already 3mm from the gap so that for the electronics remains just 1.9mm. The 6-layer multilayer board for power-distribution, analog and digital signal lines with different impedances will also function as mechanical support for the sensors. It will take 0.8mm from the inner height of gap. Since the structure is 2.2m long distributed filtering components are assumed to be needed for the bias and the supply voltages and are on the market for the required maximum thickness of 0.9mm. The thicker ASIC's have to be embedded into the PCB and soldered to inner layers. The use of the packaged solder type versions will ease the pre-testing of the ASICs, the assembly and maintenance. Since the PCB's have already special design options we aim for standard sizes and use thin pluggable interconnects to combine them to cassettes and inside the ILC-detector to the 2.2m long modules. They also have to be embedded into the PCB.

D. The data acquisition chain

The low occupancy in e^+e^- -experiments and the low duty cycle of the ILC-accelerator (0.5%) allows a system (figure 8) without a global detector trigger. Each individual channel can identify its own hits and all the hit information can be sent out of the detector. There state of the art computers are able to fulfill the task of sorting the hits to events and of deciding, what data will be written to a mass storage. By that DAQ-scheme an additional layer of fast electronics and its heat production inside the detector is avoided, which would complicate the mechanics, electronics, cabling and cooling.

Due to the huge number of channels (100 million) the first data handling has to be performed within specialized ASIC's[3] located inside the detection gaps. Each of them will process and multiplex the signals from the surrounding sensors. Figure 9 summarizes the tasks of the ASIC on the example of the SPIROC, the chip for the SiPM-readout handling 36 sensors. The arriving analog signal will be fed into three amplification chains. A fast one will generate the self trigger by signal-above-

threshold. Its information generates the hold-signal for a time measurement and for storing the amplitude of the two other amplifiers. The shaping is adjusted to the latency of the hold and their different gain factors increase the dynamic range to around 16bit. These three information are stored into an analog pipeline with a depth of 16 triggers until the end of the bunch train. Then the most useful gain for each channel and trigger is selected. The amplitude and time information are slowly ($80\mu\text{s}/\text{Sample}$) digitized and put into digital memory until a request to send the data out. To minimize the required signal lines, the data (20kbits/ASIC/bunch-train) are sent out to only one line, which is even shared with a few other ASIC's using it after each other. The number of multiplexed ASIC's is limited to around 10 because also the speed of the data transfer is chosen as a compromise to power consumption to be 1Mbit/s and the data transfer has to finish before the start of the next bunch train.

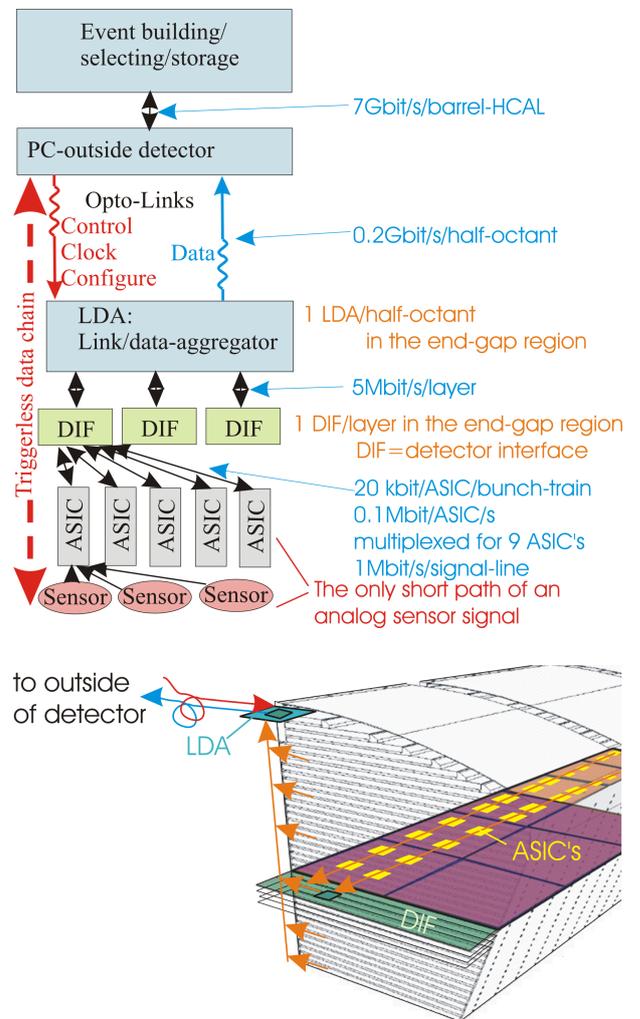


Figure 8: DAQ chain for the ILC experiment with a boot information stream from out of the detector PC's to the in detector sensors (top to bottom) and the information from the sensors about the e^+e^- -interactions in the opposite direction (bottom to top).
Top: As functionality with typical data rates.
Bottom: As locations at the HCAL half-octant

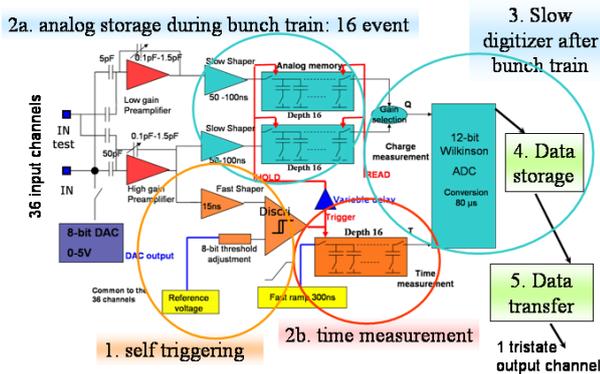


Figure 9: VFE-ASIC: The basic building blocks for the signal handling foreseen for the CALICE-type calorimeters. The boxes with the color gradients indicate major functionalities executed by the attached ovals. The numbers indicates a time order of the executed actions.

The further layers of electronics will be described in the context of the HCAL, but the concept also applies accordingly to the ECAL. The next stage of electronics is located at the end of the detection gaps (figure 8) called "detector interface" (DIF). Each DIF operates a few chains of ASIC's in one detection gap and organizes the multiplexing for the data transfer from the ASIC via the DIF to a local data aggregator (LDA) at the corner of each half-octant. Its functionality is the minimizing of connections out of the detector by formatting the data to optical fibers with moderate speeds ($>1\text{Gbit/s}$). The fibers are routed out of the detector and get connected via interfaces to standard computers for the event building. At the end of the chain the computer will write the data to a mass storage.

Through the same modules the necessary boot information, enumeration and timing of the bunches is distributed from the outside of the detector to the individual ASIC's. To avoid additional cabling to the end-gap region, these data links will also be used for the slow data transfers. So the outside PC's get also the masters for the slow setup, for the control and for the monitoring.

E. Calibration

The calibration of a detector is essential for the quality of the data generated by it. A good calibration procedure has to be established and designed into the system. The aim for CALICE is to settle the calibration scale to 1%.

For the proposed calorimeters the most critical issue is the gain of the SiPM. It depends strongly on the environmental parameters. For example the generated charge Q per energy deposit depends on the applied bias voltage V_{bias} and the temperature T :

$$\frac{1}{Q} \frac{\partial Q}{\partial V_{bias}} = \frac{70\%}{V} \quad (2)$$

$$\frac{1}{Q} \frac{\partial Q}{\partial T} = \frac{-4.5\%}{K} \quad (3)$$

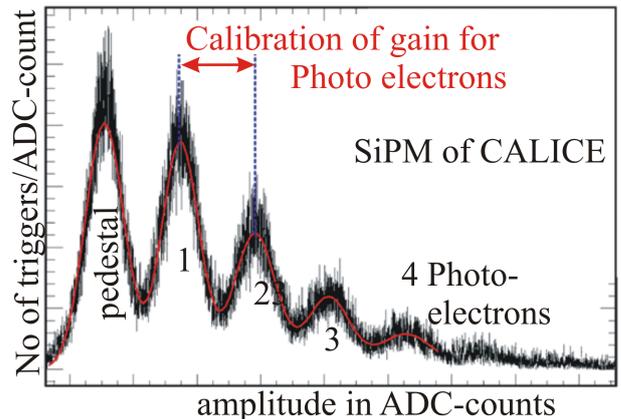


Figure 10: SiPM response to a low level light source.

Therefore the behavior of the environmental parameters have to be studied, measured and controlled (temperature see next section). For small remaining effects the data can be corrected on the measurements of the environment. The other way is to measure the gain directly per SiPM. SiPM's designed with low fluctuations of the gain from pixel to pixel and operated with low noise electronics offers the opportunity for gain measurement by themselves. The peaks for a few photo-electrons are visible in an amplitude spectrum (figure 10) as individual Gaussian peaks. The distance between the peaks can be used to calculate the gain.

As hardware for that measurement a fast light source is required, which sends a few photons during a short interval (few ns) to the SiPM. The VFE-electronics needs to trigger on the same signal from the DAQ as the light source to be synchronized to it or to trigger by itself with the ambitious threshold of half a photo electron. Both features will be offered by the next generation of ASIC's.

The technique gets complex since each SiPM needs the light source and a few million of them will be installed. Also the thin detection gap is already filled up with a lot of components and the light source adds further parts. Therefore the CALICE collaboration is studying two approaches.

In a first version - used now at the test beam - the light of a strong LED's is distributed to many SiPM's. In that approach the LED's can be located outside of the detection gap as part of the "end-gap"-electronics and its intensity can be monitored. The drawback of that technique is, that optical light guides have to be rooted to each individual SiPM, which is a labor intensive job.

In another approach individual LED's are located inside the detection gap for each SiPM. Since the design of the detection gap leaves only a thin layer for the electronics the LED has to be located in a hole of the PCB and to be soldered upside down (figure 11). The first test board is just manufactured. The main problem to be looked at, is the EMI-cross talk from the pulsed LED nearby the photo sensor. A PCB with a low impedance power-GND system and low amplitude pulses is prepared, which allows different test methods. The measurements

just started and will provide information for further steps of the development.

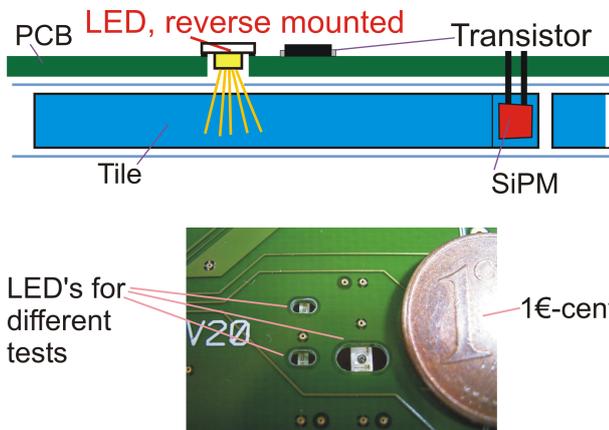


Figure 11: A LED mounted into a hole of a PCB, shining through a scintillator to a nearby SiPM

The stability of the signals from the Si-diodes of the ECAL and the ASIC's are expected to be much better. To watch them on a short time scale, a charge injector is integrated into the ASIC. The monitoring of the calibration for the whole calorimeter will use minimum ionizing particles through each cell and reconstruction of the mass of decays from identified particles. That needs statistics and therefore longer measuring periods.

IV. POWER AND COOLING

A. Power cycling

The aim of the electromechanic design is a dense calorimeter. Therefore any space for infrastructure has to be minimized with great importance inside the detection gaps. Since power and according cooling needs space for cables and tubes any power consumption should be reduced to a minimum. To realize a calorimeter with 100 million channels under this constraint for space, any saving on the power budget has to be considered. The aim is to keep for the DAQ-electronics located inside the detection gaps the power as low as $25\mu\text{W}/\text{channel}$. The first ASIC's for that goal are designed and submitted. These very low power consumption is reached by designing the ASIC's and their functionality to the needs of the system.

The ILC-accelerator offers due to its duty-cycle of 0.5% - 1ms bunch-trains every 200ms - and the low cross section for e^+e^- -interactions opportunities for power savings:

- The fast analog electronics can be switched off during the breaks between the bunch trains. The ASIC design realized that, by switching current sources off on the demands of an external logic signal synchronized to the bunch trains. The analog parts are switched on early enough to stabilize before the first bunch arrives and can be kept on during the whole time of analog signal handling including the digitization. A duty cycle for the electronics of 1% is reached, by which two order of magnitudes in power are saved.

- The needs for the digital electronics will be kept low, by adapting the speed to the low amount of data. A transfer speed of 1Mbit/s is a reasonable compromise between power and limitations to the multiplexing. To cope the whole data volume of a detection gap space and connectors for a few signal lines (5-8) has to be provided.

Carefully minimizing the currents low mean power consumption is reached. Table 1 summarizes the mean currents and their peak values during the bunch trains.

Table 1: Current consumptions of the power cycled VFE-electronics

Consumer	number of channels	Mean current	Current during bunch train "Peak current"
Single channel		$7.5 \frac{\mu\text{A}}{\text{channel}}$	$750 \frac{\mu\text{A}}{\text{channel}}$
HCAL			
HCAL-Layer	≈ 2200	$17 \frac{\text{mA}}{\text{layer}}$	$1.7 \frac{\text{A}}{\text{layer}}$
Total per sub-detector			
HCAL, barrel	2.5million	2kA	20A
ECAL, total	80 million	60kA	600A

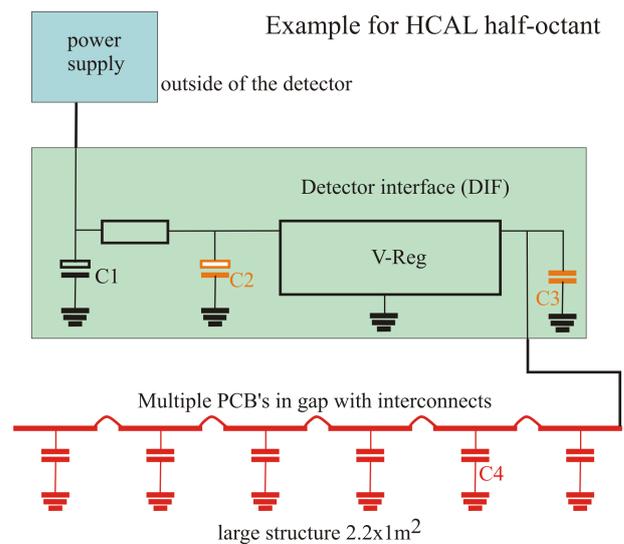


Figure 12: Concept for the power cycling. Local charge storage at the DIF and inside the detection gap stabilize the current supplied from the outside of the detector to a DC-current.

The total mean current looks feasible. But that is a fact of the power cycling and shows its importance for a solution of a high granularity calorimeter. The consequence is, that the huge total currents should be kept locally and by that distributed to a lot of lines entering the detection gaps. On the other side the hardly accessible electronics with strong space constraints inside the detection gap should be kept simple. Therefore a concept (figure 12) is developed, in which the charge is transferred as DC-currents from the outside of the detector to the DIF nearby the detection gap. There a large amount of charge can be stored (C2) before the voltage gets stabilized for the operation of the sensors and of the ASIC's inside the detection gap. After the

voltage regulator again charge can be stored in the DIF (C3) and inside the detection gap (C4), to accomplish the reaction time of the voltage regulator and the charge transfer time into the detection gap as discussed in the following.

This concept of stable DC-current from the outside keeps all fluctuations in the sub component itself. The absorber plates of the calorimeter acts as shields for the electromagnetic interference (EMI) and protects the calorimeter itself and the other subdetectors. Also the cables for the DC currents can be chosen thinner than for solutions with current pulsing with high amplitudes to the outside. But additional components are installed in the end-gap region and they will produce additional heat.

The impacts on the electronics will be described on the example of the HCAL. The actor of the power pulsing are the ASIC's themselves. Controlled by a logic signal they switch the current of the main consumer, the analog part, off. Since the travel time for signals over the 2.2m long PCB's is 15ns - around half of the speed of light - some charge has to be stored inside the detection gap in the capacitors C4. They have to be chosen large enough, so that the voltage drop is small enough, until the the DIF can react by increasing its supply current. A typical power-GND plane structure of a PCB (50 μ m distance) has a capacitance of 70pF/cm². This buffers a bit of charge and is intrinsic to the design. With 9cm² per channel and the peak current consumption from table 1 the voltage drop in the first 15ns would be

$$\Delta V = \frac{750\mu A/channel \cdot 15ns}{70pF/cm^2 \cdot 9cm^2} = 19mV \quad (4)$$

Whether that voltage drop already is tolerable, will be evaluated during the further development. But with three 200nF capacitors per ASIC the voltage drop could be reduced below 1mV. Such components are available with a thickness of 650 μ m and fit inside the detection gap of the HCAL.

Another concern to be looked at in the detection gap is the DC resistivity. The major contributions are the six interconnections between the PCB's, each might have a typical resistance of 10m Ω per contact for the GND and for the power. Here the peak current of 1.7A (table 1) is relevant. But due to the distributed sensors the current is continuously reduced along the path and can be reduced by a factor 2 for the calculation. So the voltage drop at the end of the gap would be 100mV. During the bunch train it can be assumed as a DC-current and constant voltage drop. So it will not harm the system as much as the discharge of capacitors. But that effect could also easily be reduced by using a parallel row of pins, which would anyway be nice for redundancy of the power connections. 10 parallel pins would still be an easy installation for a 1m wide structure, but the experience will guide the necessary effort.

Typically after the first 15ns the DIF will act. At first charge will be taken from a capacitor C3 after the voltage regulators. This capacitor has to supply currents for the time until a voltage regulator can act. Fast designs would do so in 1 μ s. A comfortable low voltage change of 5mV can be realized with 40 ceramic capacitors C3 adding up to 340 μ F distributed over the 1m width. For the long time of the bunch train, 2ms, capacitors C2 before the voltage regulators can store the charge. There the voltage drop can be much larger and 3.4mF composed out of 10 SMD

tantal capacitors would generate a 1V voltage drop, which can slowly be recharged during the long break. Of course that nearly triangular voltage pulse has to be supplied as overvoltage from the power supply and produces heat at the DIF.

But there the heat of 45mW/layer can be cooled away with a limited effort and will be a minor heat source compared to other installations in the end -gap region. The additional heat production there of (1V+1V+0.5V) \times 17mA=45mW is comfortably estimated with a mean current of 17mA and with contributions of a voltage drop of 1V for the pulse, 1V at the regulator and 0.5V as safety margin at the resistor.

The power pulsing seems to be solvable by storing charge in capacitors. Further effort will go on in combination with experiencing the behavior of the CALICE electronics. The special items to be looked at will cover the impact on the performance of the calorimetry and finding components with sufficient lifetime and reliability.

B. Cooling of the detection gaps

The motivation to develop ASIC's and a concept with very low power consumption was to avoid active cooling of the detection gaps. Because of the huge number of detection gaps and, because only thin layers of low density material are allowed inside the calorimeter, a cooling system with liquids would be space consuming, cost driving and risky. Therefore in the following it will be calculated, what temperature drops build up by just using the absorber plates as passive heat conductors. Of course they have to be cooled at the end, near the DIF's (figure 8).

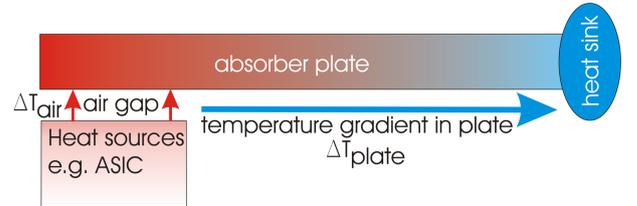


Figure 13: Heat flow for heat sources located in the detection gap. Heat flow from source via air to the absorber plate and inside that plate to the cooled end of the plate.

The heat sources for the HCAL are the ASIC's with 25 μ W/channel but also the dark current of the SiPM with 15 μ W, 0.3 μ A at 50V. The model for the calculation is sketched in figure 13. The heat has to flow first from the source, e.g. an ASIC, to the absorber plate. Counting around $A_{ASIC}=4cm^2$ as active area for an 36-channel-ASIC and using as other inputs for the calculation a heat conductivity of air (N₂) of $\lambda_{N_2}=24mW/Km$ and an overestimated thickness of the air gap of $d_{air}=1mm$ the temperature drop

$$\Delta T_{gap} = \frac{1}{\lambda_{N_2}} \times 36P_{channel} \times \frac{d_{air}}{A_{ASIC}} = 0.1K \quad (5)$$

would still be marginal.

The other contribution to temperature rises is the heat transfer inside the absorber plate. For the HCAL the three parameters of the stainless steel plate describe the contribution to the thermal behavior: Thickness $d_{steel}=2\text{cm}$, heat conductivity $\lambda_{steel}=15\text{W/Km}$ (typical, but largely depending on the steel) and the heat capacity $\kappa_{steel} = 3.7\text{MJ/m}^3\text{K}$. The geometry for the HCAL can be simplified by three assumptions:

- The detector is nearly symmetric around the beam pipe and no heat will flow along each circle.
- Radially is the calorimeter a sandwich. There are too many gaps to build up an effective heat flow. The flow will be neglected.
- The remaining direction z with effective heat flow is parallel to the beam line.

The mathematical equations - derived from energy conservation and heat-flow proportional to the temperature gradient - collapse to a one dimensional time dependent differential equation. It can be solved for the temperature T at the geometrical position z and the time t as Fourier-evolution with exponential time behavior. The boundary conditions are defined by the geometry of the HCAL, which is symmetric at the transversal plane ($z=0$) through the interaction point and cooled at the end plates at $z = \pm L_{HCAL}$ with $L_{hcal} = \pm 2.2\text{m}$:

$$T(t, z) = \frac{\text{power/area}}{2\lambda_{steel}d_{steel}} \cdot \left\{ (L_{hcal}^2 - z^2) + \sum_{\text{all } \alpha} A_{\alpha} e^{-\frac{t}{\tau_{\alpha}}} \cos(2\pi\alpha \frac{z}{L_{hcal}}) \right\} \quad (6)$$

$$\alpha = \frac{2n-1}{4} = 1/4, 3/4, 5/4, \dots$$

$$\tau_{\alpha} = \frac{\kappa_{steel}L_{hcal}^2}{4\pi^2\lambda_{steel}\alpha^2}$$

$$A_{\alpha} = \text{the Fourier amplitude defined by } T(t=0, z)$$

The power/area is the heat from the ASIC and the SiPM for 2200 channels/ 2m^2 : 44mW/m^2 . The time development of the temperature is very slow. The slowest component ($\alpha=1/4$) develops with a time constant of 5.6 days and for the next terms 0.6 days, 0.2 days, This slow temperature development for the HCAL is shown in figure 14. The starting condition at $t=0$ was set to a homogenous temperature $\Delta T(0, z) = 0\text{K}$.

The slow behavior has the disadvantage of long times for stabilisation after maintenances of the detector, but allows also measurement, calibration and correction for the time development. The general shifts in the gain of the SiPM's are expected to be smaller than 1%, because the temperature change itself is small (0.36K) even after long heating times.

For the ECAL a numerical approach delivered a temperature profile of 7K (figure 15). That approach has put only the copper shield in as heat conductors and neglected the W-plate. So it is close to a worst case estimate. Since the Si-diodes are not so sensitive to temperature even the 7K are tolerable.

The temperature calculations for ECAL and HCAL show tolerable values even without liquid flow cooling inside the absorber gap. Required is a cooling at the end of the gaps, but

these areas can be reached by infrastructure without large interference with the performance of the calorimeter. This simple solution for the cooling is only possible due to the low power design of the ASIC's and the effort to power cycle the analog parts of the VFE.

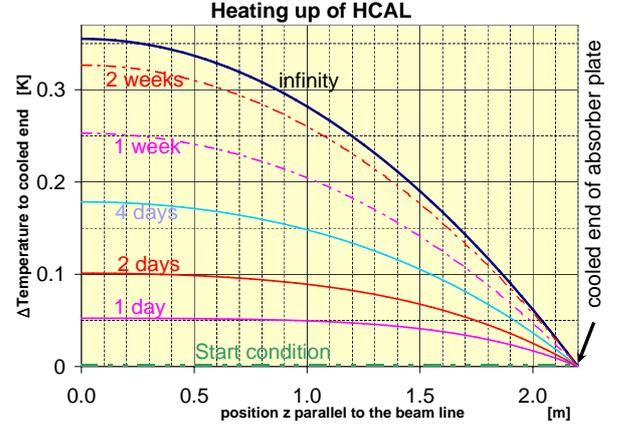


Figure 14: Temperature development of the HCAL. z parallel to the beam axis, at $z=2.2\text{m}$ is the absorber structure cooled and at $z=0$ is just the symmetry of the plane through the interaction point with no heat flow.

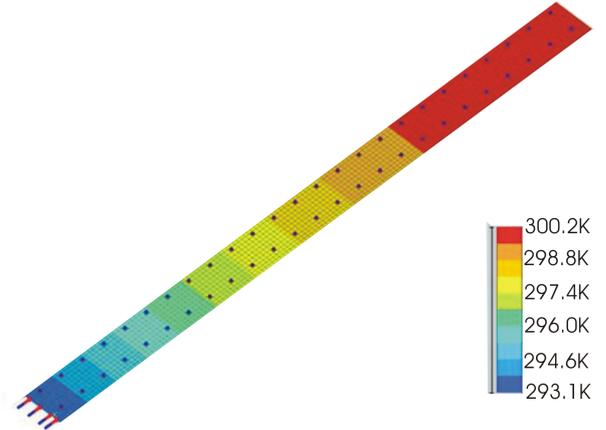


Figure 15: Estimation of the temperature profile of an ECAL slab. It is 1.5m long

V. OUTLOOK

The CALICE prototype calorimeter system has collected 200 million events showing already that details of the showers are visible. The studies on the particle flow algorithm and the system design for the high granularity calorimeter will continue and look promising. In the future the developed ideas and the

results from the test beam measurements have to be evaluated into real designs for an ILC-detector.

This work will also be influenced by alternative experimental studies with different readout architectures for high granularity calorimetry. For ECAL W-Scintillator-SiPM and W-Si with digital pixel readout are under study. A steel with resistive-plate-chambers and with digital readout for the HCAL is an alternative, which now is being prepared for a large scale test beam seetup.

As the next steps more of the ideas will have to be proven by experiments and the design has to be put together with the other sub detectors into a coherent technical design report for a detector at ILC.

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