Design of an integrated particle detector-cell based on latchup effect

Alessandro Gabrielli[1], Danilo Demarchi[2]

[1] Physics Department of Bologna University & INFN Bologna, Italy,
[2]Chilab Laboratory, Electronics Department, Politecnico di Torino, Italy
Email: alessandro.gabrielli@bo.infn.it URL: http://www.bo.infn.it/~gabriell

Abstract

The paper describes an innovative idea for a silicon pixel detector. The principle is based on latchup effect that is common in to-date CMOS technologies working in a radiation environment. A prototype was constructed in the past with commercial components and here is described in detail an integrated version of the design. In principle the detector has low triggering and dead time, can operate at room temperature, does not require a high voltage power supply and is intrinsically tolerant to radiation. As a latchup-based detector can be constructed using state-of-the-art CMOS technologies, here it is presented a design of a prototype that will be implemented on a commercial 0.35 µm Bi-CMOS technology and tested at Electronics Department of Torino Politecnico.

Conclusions

In principle an integrated version of a latchup-based detector could be interesting in terms of spatial resolution, triggering and dead time. Plus, it requires neither a high voltage power nor a biasing current. In addition, cell power consumption is negligible when the thyristor is off and the cell also works at room temperature. Moreover, it is intrinsically radiation tolerant since this can be fabricated with state-of-the art, low resistivity technologies. Out signal does not require charge/current amplifiers and analog-to-digital converters normally embedded in front-end modules; the latchup-based detector's out signal is self-noiseless, digital, robust and stable.

According to the features described above the application fields may range from beam monitors to heavy ion selectors. Of course, the latchup susceptibility of the proposed cell needs to be confirmed, investigated and finely tuned. The challenge is the sensitivity.

The design

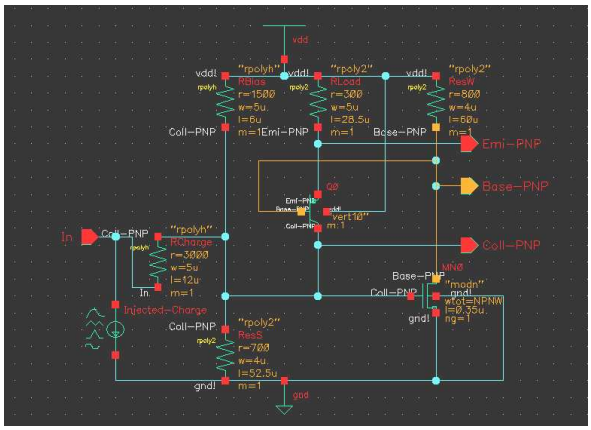
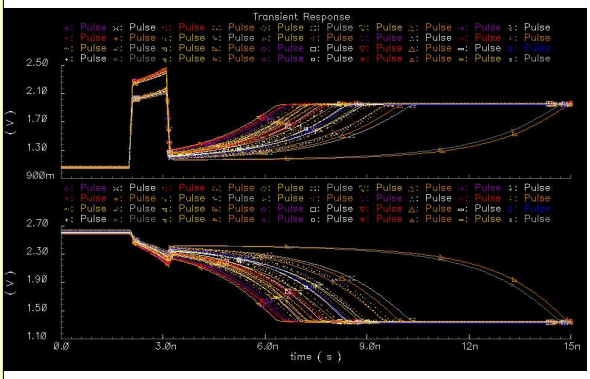


Figure 2 mixed-mode Bipolar-MOS circuit

The simulations



Monte Carlo simulated sensitivity up to 280uA × 1ns = 0.28pC.

The circuit has been Monte Carlo simulated, and other investigations are ongoing, to choose the best parameters in term of cell pre-bias and polysilicon layer used for resistors. These choices will manly affect the final layout. The figure shows one of the main representative Monte Carlo simulations. The above curve in the figure is the injected stimulus and the below plot is the output port Base-PNP that saturates towards ground when the cell ignites. The circuit has been stimulated via a charge pulse of the order of a fraction of pC, i.e., a current of some uA that flows for some ns. The injected charge, by passing through the biasing resistors, provides the cell with the required extra biasing voltage drop to start latchup ignition. The output spread accounts for the technology mismatches of the fabrication process. In ay case, the circuit works even though with different ignition speed, from 3 to 12 ns after the stimulus. The simulations have not been stressed till he highest sensitivity of the cell, they have been carried out in order to get a quite-balanced circuit to test with different stimuli to get inspirations for new prototypes.

The latchup effect

Single Event Effects (SEEs) are caused by the charge deposited by a particle with over-threshold energy within microelectronics devices. Due to a potential permanent hazard in CMOS devices, one of the main SEEs is the well-known Single Event Latchup, SEL [1]. The latchup effect is based upon injected charges within microelectronics devices, whatever their origin. The only general requirement for a striking particle to ignite SEL in a given device is the minimum value of the deposited charge along its path. Following latchup ignition, the sensitive cell retains the position of the crossing particle by means of a self-locking thyristor. This provides a noiseless, digital, robust and stable signal until the whole system has been powered off. In CMOS devices the stimulated ignition of latchup effects caused by external radiation has so far proven to be a hidden hazard; however here it is proposed as a powerful means of achieving the precise detection and positioning of a broad range of particles.

Latchup is the ignition of a pn-pn or np-np parasitic structure created in conventional CMOS technologies. Fig. 1 shows a pn-pn structure on a p-type substrate silicon formed by two parasitic pnp (Q_1) and npn (Q_2) bipolar transistors. The transistors are locked together in a thyristor-like positive feedback loop. R_S and R_W stand for the substrate and well distributed resistors respectively. A series resistor R_L is also located between the OUT contact and VDD in order to limit the current produced by latchup ignition. R_L induces a reasonable output voltage drop at the OUT pin, which can be easily read. Otherwise voltage is at VDD level when the thyristor is off. The latchup effect [2] involves several steps [3], [4]. First, the small transient well (substrate) current must be sufficiently high to forward bias the Q_1 (Q_2) base-emitter junction. This requires a sufficient drop in voltage in the well (substrate) distributed resistor R_W (R_S). Second, the amplified current from Q_1 (Q_2) must be high enough to turn on Q_2 (Q_1) by forward biasing its base-emitter junction via the substrate (well) current. This current may lead to a significant voltage drop in the substrate (well) distributed resistor R_S (R_W). Then the Q_2 (Q_1) transistor can turn on to allow the current flowing in the well (substrate) to keep forward-bias conditions on the Q_1 (Q_2) transistor until the whole thyristor reaches a standing latched state. Q_1 may then lead Q_2 to saturate or, similarly, vice-versa, as long as the product of the current gains of the two transistors is greater than 1. The latchup condition must not only be sustained but also controlled within the substrate and well regions for a minimum amount of time to allow the detector readout process to take place [5], [6]. The cell proposed as the sensitive element in a latchup-based detector should be sized small enough to have a reasonable spatial resolution as a detector element for use in physics experiments [7].

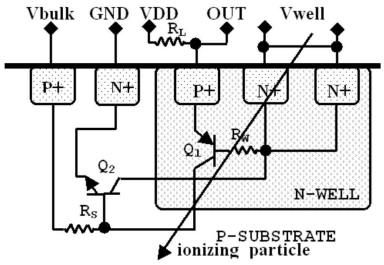
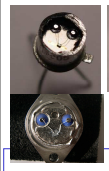


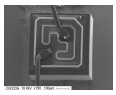
Figure 1: cross-section layout of a p-substrate cell

REFERENCES

[1] F. W. Sexton, IEEE Tran. Nucl. Sci., 50 (2003), 603
[2] A. H. Johnston, IEEE Tran. Nucl. Sci., 44 (1997) 2367
[3] A. H. Johnston et al., IEEE Tran. Nucl. Sci., 37 (1990), 1886
[4] G. Bruguier et al., IEEE Tran. Nucl. Sci., 43 (1996), 522
[5] E. C. Sangiorgi et al., IEEE Tran. CAD, 4 (1985), 561
[6] C. Feigna et al., IEEE Tran. Elec. Dev., 36 (1989), 1683
[7] S. Antinori et al., IEEE Tran. Nucl. Sci., 51 (2004), 2941
[8] A. Gabrielli, El. Lett., 41/11 (2005), 25
[9] A. Gabrielli, Meas. Sci. Technol., 17 (2006), 2269

The past studies



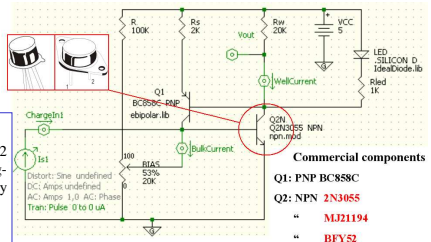


It was proved that:

- under three different tests the circuit, by stimulating the Q2 transistor with daylight, with electrons in a scanning-electron-microscope and via a current pulse, ignited in any case,

- the greater the injected charge, the quicker the response,

- a charge sensitivity of the order of **1 pC can be achieved via discrete components [9] .**



Commercial components

Q1: PNP BC858C
Q2: NPN 2N3055
" MJ21194
" BFY52
" 2N2222A
R_X: multiturn variable resistors

The design of the integrated prototype

Previous investigations indicate that the recognizable charge might be comparable to that collected into to-date detectors. In fact, a prototype made up of discrete components was designed, constructed and exploited and the tests with daylight, electrons, via a current pulse generator and with a laser beam showed a charge sensitivity of the order of 1 pC [8-9]. It is expected to scale the charge sensitivity with an integrated version of the prototype. This is the reason why a new prototype is under design via a commercial AMS 0.35µm BiCMOS technology. Moreover, here a mixed-mode Bipolar-MOS circuit is designed and it is going to be submitted. The circuit is basically composed of a p-channel bipolar and a n-channel MOS transistors, plus some biasing resistors. In addition, the resistors are made via resistive polysilicon provided by the technology. The choice of the transistors are based upon the technology features and models.

Design parameters		
Parameter	Sweep	Geometry
Resistor Rs	700 Ω	4×52 µm layer 2-poly
Resistor RL	250÷350 Ω	5×28 µm layer 2-poly
Resistor RW	800 Ω	4×60 µm layer 2-poly
Resistor RBias	1.4÷1.6 kΩ	5×6 µm layer h-poly
VDD	3.3 V	
Resistor RCharge	3.0 kΩ	5×12 µm layer h-poly
Input Charge	150÷350 fC	

The two circuits shown in Fig. 1 and 2 differ from form Q_1 transistor that is a planar PMOS in Fig. 1 while it is a vertical bipolar PNP in Fig. 2. The principle remains the same as the two transistors are locked in the same positive feedback loop. The charge here is collected in the base-emitter region of the bipolar and in the gate area of the NMOS transistor. For this reason, in principle, a thick detector is not required. As the bipolar transistor will be fabricated vertically while the NMOS is planar, it is expected that the two transistors retain also a different sensitivity due to the different technology implementations. The BJT might be mainly sensitive to deep charge despite the planar NMOS that might be ignited via surface injected charge. The combination of the two transistor could provide a balanced sensitivity of the entire cell.