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A first-level track trigger architecture for Super-CMS

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We present a first architectural study of a first-level hardware track trigger for CMS at SLHC. The design of a hardware track trigger at 10^35cm-2s-1 is challenging. A primary constraint on implementation will be power consumption within the detector, in turn driven by the data transmission bandwidth to off-detector electronics. We therefore emphasise the minimisation of the data flow through local filtering of track candidates on the detector. The architecture presented does not comprise a stand-alone track trigger, but uses identified muon and calorimeter trigger objects to seed track-matching within an integrated first-level system.

Summary

The Super-LHC (SLHC) proposal would increase the luminosity of the LHC machine by a factor of ten, to 10^35cm-2s-1. Since this is also likely to require a change to the bunch structure of the machine, the incoherent background in the LHC detectors could exceed that observed at LHC by up to a factor of twenty. The ability to trigger efficiently on high-pt physics signatures, with good control of rate, is therefore of paramount importance, and it is clear that the first-level hardware trigger systems designed for LHC will need to be upgraded. One promising route to maintain trigger performance is to incorporate tracking information into the first-level hardware trigger decision. Algorithms including track information for refinement of trigger object identification and pt measurement are already in use in the very first stages of the CMS high level trigger. Data bandwidth (and the associated on-detector power consumption) is likely to be a key constraint in the implementation of such a hardware system. We present here an architecture combining several elements of on-detector and off-detector data reduction, while preserving sufficient track information to maintain the performance of the muon and calorimeter triggers at a similar level to that expected at LHC. We do not propose a full stand-alone track trigger, but maintain the concept of triggering primarily on lepton, photon and jet objects. The proposed architecture makes use of the stacked detector layer concept defined in previous design studies, allowing an effective geometric pt-cut on track candidates. An on-detector data reduction step is performed on track stubs found in two such layers, using outer and inner radius detector stacks; this step includes the flagging of track stub multiplicity, allowing a simple isolation criterion. The final inter-stack correlation step is performed off detector after seeding by candidate objects from the muon and calorimeter systems, allowing a substantial reduction in the required data processing capacity. This system also has the potential for further rate reduction by correlation of the z-vertex of trigger objects in multi-object signatures.

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