The TOTEM Front End Driver, its Components and Applications in the TOTEM Experiment

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Abstract

The TOTEM Front End Driver, so-called TOTFED, receives and handles trigger building and tracking data from the TOTEM detectors, and interfaces to the global trigger and data acquisition systems. The TOTFED is based on the VME64x standard and has deliberately been kept modular. It is very flexible and programmable to deal with the different TOTEM sub-detectors and possible evolution of the data treatment and trigger algorithms over the duration of the experiment.

The main objectives for each unit are to acquire on-detector data from up to 36 optical links, to perform fast data treatment (reduction, consistency checking, etc.), to transfer it to the next level of the system (via the Slink64 interface), and to store data on request for slow spy readout via VME64x or USB2.0. The TOTFED is fully compatible with CMS and permits TOTEM to run both standalone and together with CMS. The TOTEM Front End Driver, its components and applications in the TOTEM experiment are presented in this paper.

I. INTRODUCTION

TOTEM (Total Cross Section, Elastic Scattering and Diffraction Dissociation) [1] is an experiment dedicated to the measurement of total cross section, elastic scattering and diffractive processes at the LHC. The full TOTEM detector consists of Roman Pot Stations (RPS), Cathode Strip Chambers T1 (CSC) and Gas Electron Multipliers T2 (GEM). The T1 and T2 detectors are located on each side of the CMS interaction point in the very forward region, but still within the CMS cavern. Two Roman Pot stations are foreseen on each side of the interaction point at 220 m and 150 m. Each Roman Pot station consists of two groups of three Roman Pots at a distance of a few meters to obtain a sufficiently large lever arm to establish co-linearity with the LHC beam for the tracks prior to generating a level one trigger for the corresponding event. Each Roman Pot contains 10 silicon strip detectors with 512 strips read out by 4 VFAT2 readout chips.

Future experiments in High Energy Physics, such as TOTEM for the LHC at CERN, raise the demand for high performance data processing and Data Acquisition Systems (DAQ). Multilevel filtering DAQ architectures require fast buffering for intermediate storage of raw data while the event is processed in various levels.

II. GENERAL SPECIFICATIONS

The general requirements are that the three TOTEM detectors should be able to operate as a sub-detector of CMS. They need to provide in-time trigger inputs, which can generate a global trigger for the CMS experiment. This is particularly difficult for the Roman Pots at 220 m from the interaction point. The detectors should also be triggered by the general CMS trigger, and their data should be incorporated into the CMS data acquisition.

A. Trigger partition and trigger generation

TOTEM will be allocated one timing partition out of 32. It will receive its trigger and timing information for all three detectors from this partition. The Timing, Trigger and Control (TTC) system adopted is the one developed in common for all LHC experiments. Events are synchronized with the 40.08 MHz bunch-crossing clock of the LHC machine. Currently it is foreseen that TOTEM provides 16 inputs out of 128 to the global trigger box of CMS. Of these 8 are allocated to the Roman Pots, 4 to the T1 detector and 4 to the T2 detector. The trigger signals are generated independently for the three TOTEM detectors. Whether they are forwarded as such to CMS or first put into coincidence prior to sending them to CMS is still under discussion.

Because of the stringent latency requirement on the trigger coming from the Roman Pots at 220 m a special rack was foreseen at an optimal location in proximity of the global trigger box of CMS while minimizing the cable length. Apart from the electronics treating the trigger signals coming from the TOTEM detectors, this rack will also house part of the readout cards of the Roman Pots and perhaps also of T2 and T1 detectors.

III. TOTEM ELECTRONIC SYSTEM ARCHITECTURE

Figure 1 illustrates the use of the TOTFED in the TOTEM electronic system [2]. The following are the main components of the system: Front End Electronics (FE), Optical Interface to Front End Driver (FED), Parallel Interface (S-Link64) and Front End Readout Link (FRL) to CMS DAQ system. In an effort to standardize across different detectors, TOTEM opted to use the same front end chip VFAT2 [3] in several detectors. The VFAT2 will be used in the Roman Pots and in the GEM detector (T2) and in the CSC detector (T1). The VFAT2 chip is read out by means of the Gigabit Optical Link (GOL) chip.

Both components were developed by the PH-MIC group at CERN: the GOL chip has been around in its final form for some time; the VFAT2 recently developed has its first application in TOTEM Hybrids. The GOL chip, which serializes data, can operate at 800 MHz or 1600MHz (for effective data rates of 640 Mbit/s and 1280 Mbit/s) and can drive a laser for an optical link.
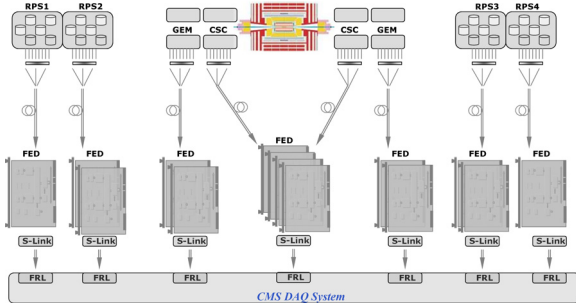

Figure 1: Use of TOTFED in TOTEM Electronic System

The VFAT2 has been designed in 0.25μm CMOS has two basic functions. The first (Trigger) is to provide fast regional hit information to aid the creation of a LV1 trigger and the second (Tracking) is for providing precise spatial hit information for a given triggered event. It has 128 identical channels. The VFAT2 will read out all the TOTEM detector channels.

IV. TOTEM FRONT END DRIVER

The CMS data acquisition system contains 512 Front End Readout Links or FRL [4] of which some fraction will be allocated to TOTEM. Each of these FRLs is capable of taking a maximum average data rate of 200MByte/s or 2kByte/event at a maximum CMS LV1 trigger rate of 100 kHz. Based on these data rates 8 FRLs will be located to the Roman Pot system, 8 to T2 and 4 for T1.

A. Functional Block Diagram

The TOTEM Front End Driver (TOTFED) functional blocks are shown in Figure 2. The general blocks are: Optical Receiver Modules (OptoRX12); CMC Transmitter, based on the S-Link64 interface; VME64x Interface; USB Interfaces; MAIN and MERGER Controllers with associated SPY Memory Buffer and Clock distribution circuits.
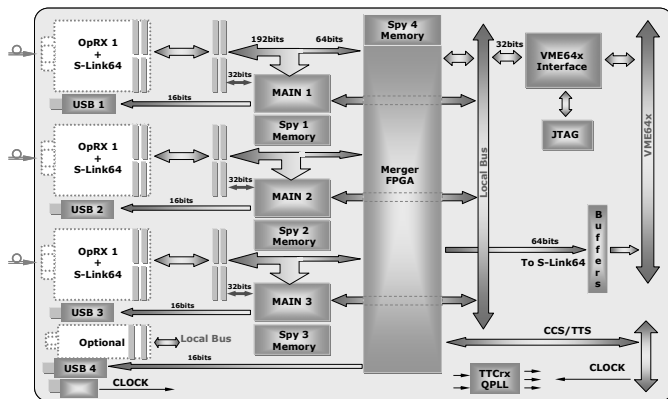

Figure 2: TOTFED Functional Block Diagram

The CMS ECAL group has developed the Data Concentrator Card (DCC) [5]. The board has 72 optical 800 Mbit/s inputs implemented in 6 NGK 12-Channel Receivers.

This board is very close to the full GOL count for the Roman Pots (72) and about twice the GOL count of the GEM detectors. However, the information content of the TOTEM GOLs is much higher: the TOTEM data density is such that only 9 optical channels would completely saturate one Slink64, thus requiring one DCC for each 9 channels – an extremely inefficient solution. Therefore a new module has been designed using the previous development as much as possible.

B. Design Strategy and Components

The TOTFED has been designed as a modular device. It is built from a set of mezzanine cards plugged onto a main motherboard known as the "VME64x Host Board". The expensive optical components are mounted solely on mezzanine cards, so that they can be tested separately and preserved if the motherboard is defective. Motherboards can be equipped with a fraction of the total number of mezzanines, and some of the mezzanines can be different depending on the application. For example, the base configuration for the CMS Preshower application has three OptoRX12 mezzanines associated to a single S-Link64 (and FRL) but it is possible to incorporate a further mezzanine card to aid data suppression prior to the S-Link64 [6]. For the TOTEM application the incoming data are distributed over three FRLs. The TOTFED is intended for operation in a VME environment in the experiment but is also equipped with USB ports to allow standalone operation. This is being implemented largely based on previous CMS Preshower work [7]. A general overview of the TOTFED is presented in Figure 3.
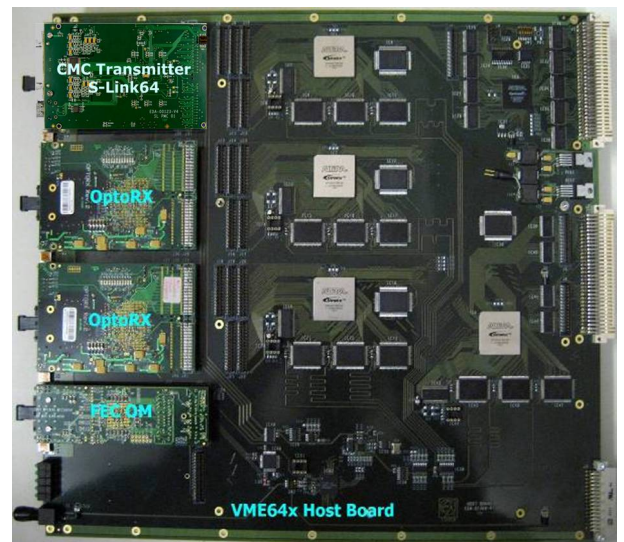

Figure 3: TOTFED Overview

The VME64x Host Board is in 9U VME64x format. It is a motherboard that accepts different mezzanine modules. It has PMC connectors for three OptoRX12 modules and three other sets of PMC connectors for optional use. The MAIN and MERGER functional blocks are implemented in FPGAs from the Altera Stratix family. Every OptoRX12 has its associated

MAIN controller connected via a 192bit bus. The MERGER shares part of this bus: 64bits from each MAIN controller. The VME64x Interface is implemented in a further FPGA from the Altera Cyclone family and is configured as a bridge between the VME and Local Bus.

The VME64x Host Board includes the TTCrx [8] ASIC with associated chipset for receiving the TTC signals and distributing the decoded information across the board. The TTC signals are provided to the TTCrx optically and/or electrically. For the optical interface with the TTCrx, an associated optical receiver is used. Concerning the electrical interface, an additional connector in the back side of the card is used. The same connector is used to provide an extra flag that signals possible buffer overflow (trigger throttling signal). On top of every OptoRX12 it is possible to plug-in a dedicated CMC Transmitter module, which connects the TOTFED to the DAQ system. There is also a possibility to connect a fourth CMC Transmitter module on the VME J2 connector and additional rear adapter.

Flexible JTAG programming interface is used for reconfiguring all the on-board FPGAs (in a variety of ways), including those hosted by the mezzanine modules.

The OptoRX12 is a general purpose plug-in module used for reception of optically transmitted data by gigabit applications. It is based on a 12-channel optical receiver and an FPGA from the Altera Stratix GX family with embedded hardware de-serializers qualified for data rates up to ~3.2Gbps. The FPGA embedded de-serializers are compatible with the Gigabit Ethernet protocol/encoding. For the interconnection with the VME64x Host Board, the module incorporates an electrical interface (using five 64-pin PMC type connectors). The electrical interface comprises dedicated pins for powering, clocking, configuration via JTAG as well as a large number (280) of lines driven from the FPGA's I/O pins. This large number of lines provides the de-serialized data from all 12 channels in parallel. Although the total number of interconnections is large, the physical dimensions of the OptoRX12 were kept relatively small (115mm x 75mm) allowing up to three of these modules to be plugged into a VME64x Host Board340mm x 360mm). Figure 4 shows a photograph of the module. Details about the OptoRX12 can be found in [9].

Figure 4: The OptoRX12 mezzanine module

V. DATA FORMAT

Data from TOTEM detectors presented to the OptoRX12 module inputs are formatted by the VFAT2 chip. The format is defined as in Figure 5.
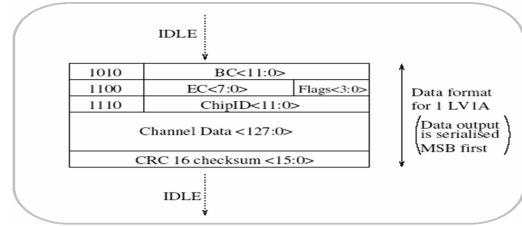

Figure 5: VFAT2 Data Format

The total length is 192 bits, where: BC<11:0> is Bunch Counter number; EC<7:0> Event Counter; Flags<3:0>; Chip ID<11:0>; Data<127:0>; CRC 16 checksum<15:0> and four control bits for the beginning of the frame. For multiple triggers, consecutive frames are emitted one after the other - one for every LV1A request.

When an event fragment is ready to be transmitted to the DAQ, the TOTFED encapsulates the data according to the common CMS data format [10] shown in Figure 6 and writes the data into the corresponding S-Link64 port.
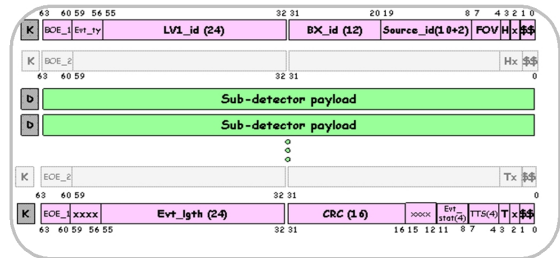

Figure 6: CMS Common Data Format

The CMS DAQ format includes, in addition to the actual sub-detector payload, information such as event type ('Evt_ty'), event number ('LV1_id'), bunch crossing number ('BX_id'), event length ('Evt_lgth'), data source identifier ('Source_id'), CRC information etc. The TOTFED events are transmitted to the CMS DAQ through the attached CMC Transmitter modules.

VI. TOTFED APPLICATIONS

The modular principle on which TOTFED is designed allows it to be used in different applications. Its main use is in the TOTEM readout system, where it is the general unit. It collects the data from on-detector front end electronics, perform intermediate storage for slow readout and transfer formatted data to the next level of the DAQ system. One readout crate contains a number of TOTFED dedicated to the corresponding detector (four for the Roman Pots and two each for T1 and T2 detectors). A sketch of the readout crate is shown in Figure 7.
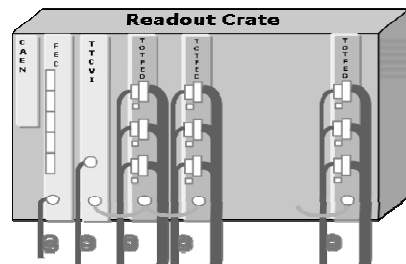

Figure 7: TOTEM Readout Crate

The second application of the general TOTFED building blocks will be in the TOTEM trigger system. The trigger bits for T1 and T2 are transmitted optically; therefore it is convenient to use the same OptoRX12 mezzanine module. For the Roman Pot system this is not possible because of the propagation delay limitation, so it is foreseen to use electrical signal transmission using LVDS signal lines. Using the VME64x Host Board not fully equipped with OptoRX12 mezzanine modules, trigger information is received and managed - applying different algorithms – before being sent to the global trigger system. A sketch of the trigger crate is shown in Figure 8.
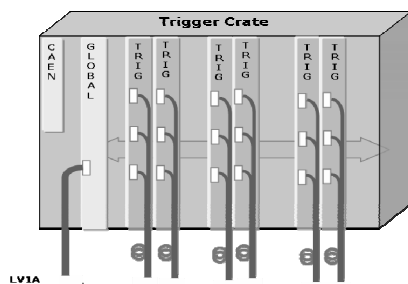

Figure 8: TOTEM Trigger Crate

VII. SUMMARY

The TOTEM Front End Driver prototype was successfully built and tested. The close collaboration with the CMS Preshower group enabled its fast development. The OptoRX12 module was designed by this group. Later on the first prototype of the CMS Preshower data concentrator card, so-called ES-DCC (see details in [6]) was successfully operated in a beam test during the summer of 2007.

It is worth mentioning that the VME64x Host Board could easily be adapted for use by future LHC systems. The board has flexible clock circuitry which allows changing the internal frequency for storing and transferring incoming data. The latest generation FPGAs permits implementation of the new optimized algorithms via remote reconfiguration system.

Several pre-series examples of both the VME64x Host Board and OptoRX12 modules have been produced. The aim is to finish the full production by early 2008.

VIII. REFERENCES

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