Electronics and Sensor Study with the OKI SOI process

TWEPP-07, Sep. 5, 2007

Yasuo Arai (KEK)

KEK Detector Technology Project : [SOIPIX Group, http://rd.kek.jp/project/soi/]

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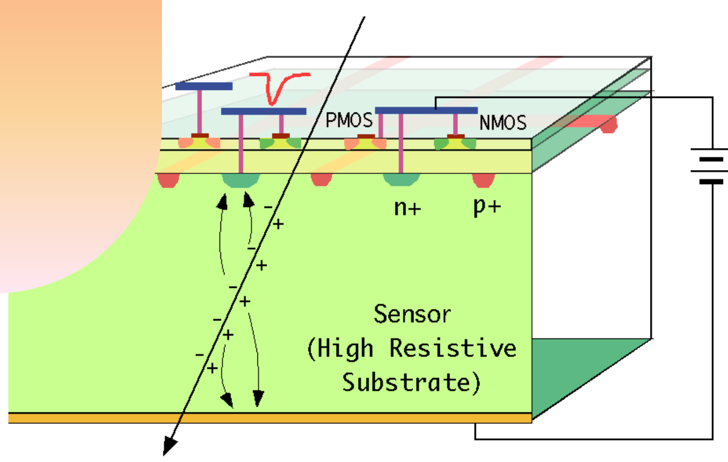
KEK, JAXA[A], U. Tsukuba[B], TIT[C], Osaka Univ.[D], U. Hawaii[E], SLAC[F],
OKI Elec. Ind. Co.[G],

OUTLINE

- SOI Device
  - History of SOI
  - Features of FD-SOI
- SOI Pixel Detector
  - Progress of SOI Pixel R&D
  - FY05 MPW Results
  - TCAD Simulations
- FY06 MPW Run
  - Preliminary Results
- Summary



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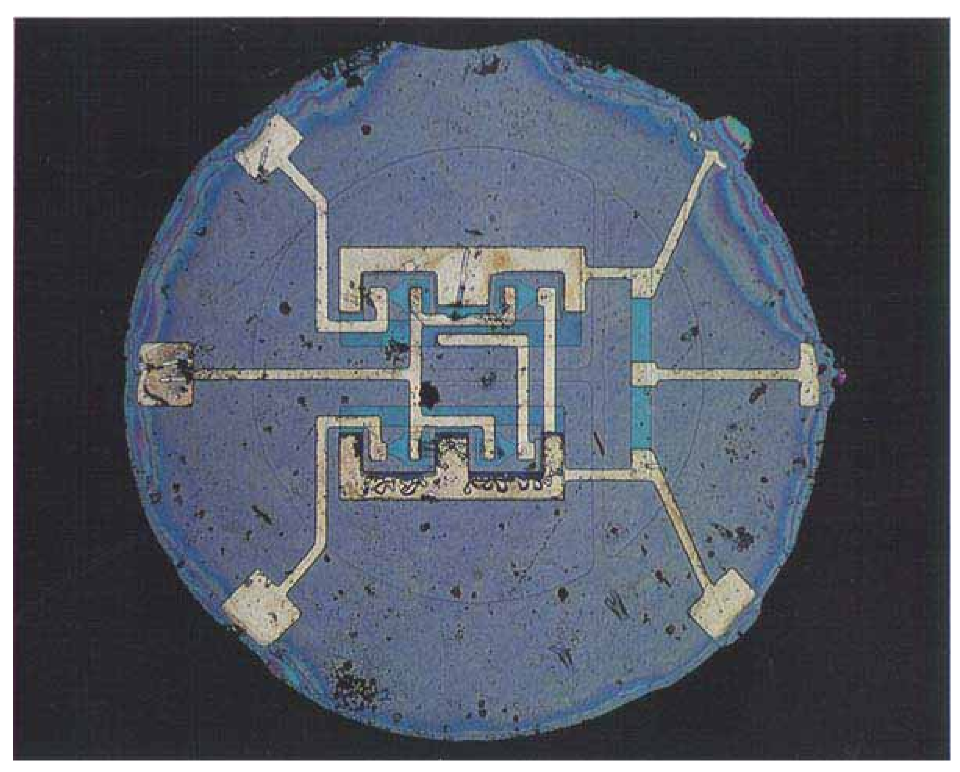
History of SOI (Silicon-On-Insulator)

First Planar IC (1959 R. Noyce)



Most ICs are built on Bulk Si substrate.

Each transistor is isolated by reverse-biased p-n junction

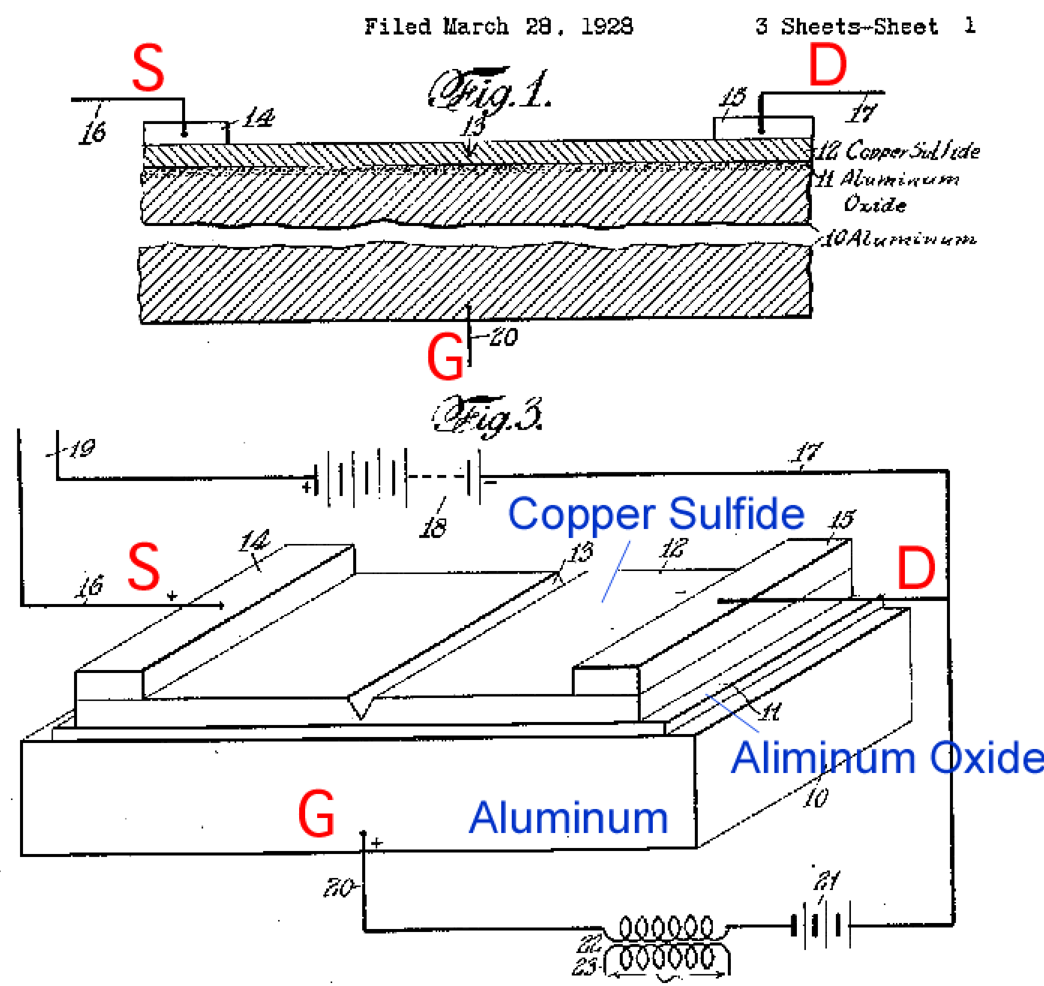
Bulk Si Technology

Historical FET Patent (1928)

J. E. Lilienfeld
(Poland, 1882-1963)

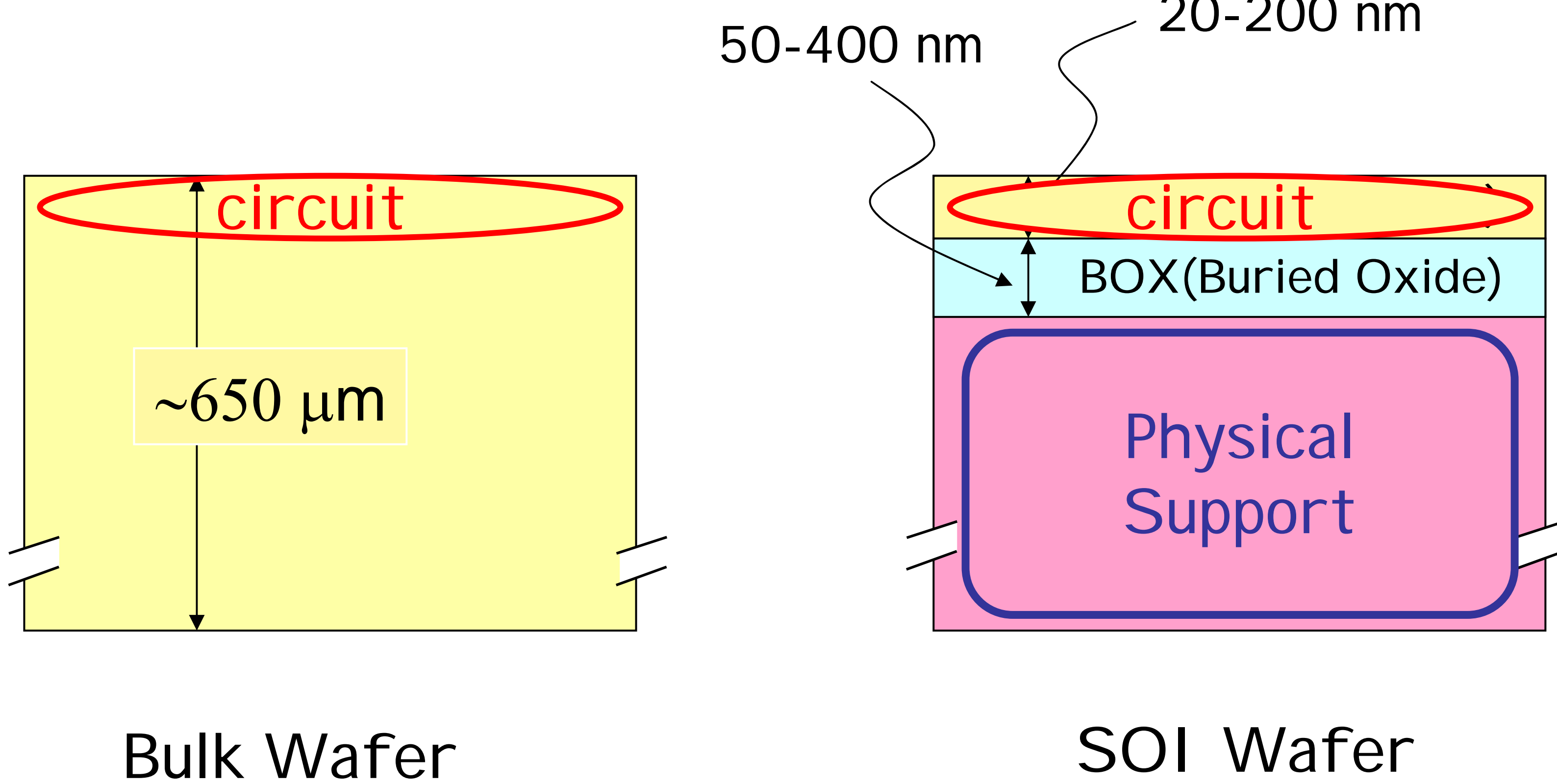
Transistor is built on a thin Si Film supported by an Insulating Substrate.

(Prototype of SOI)



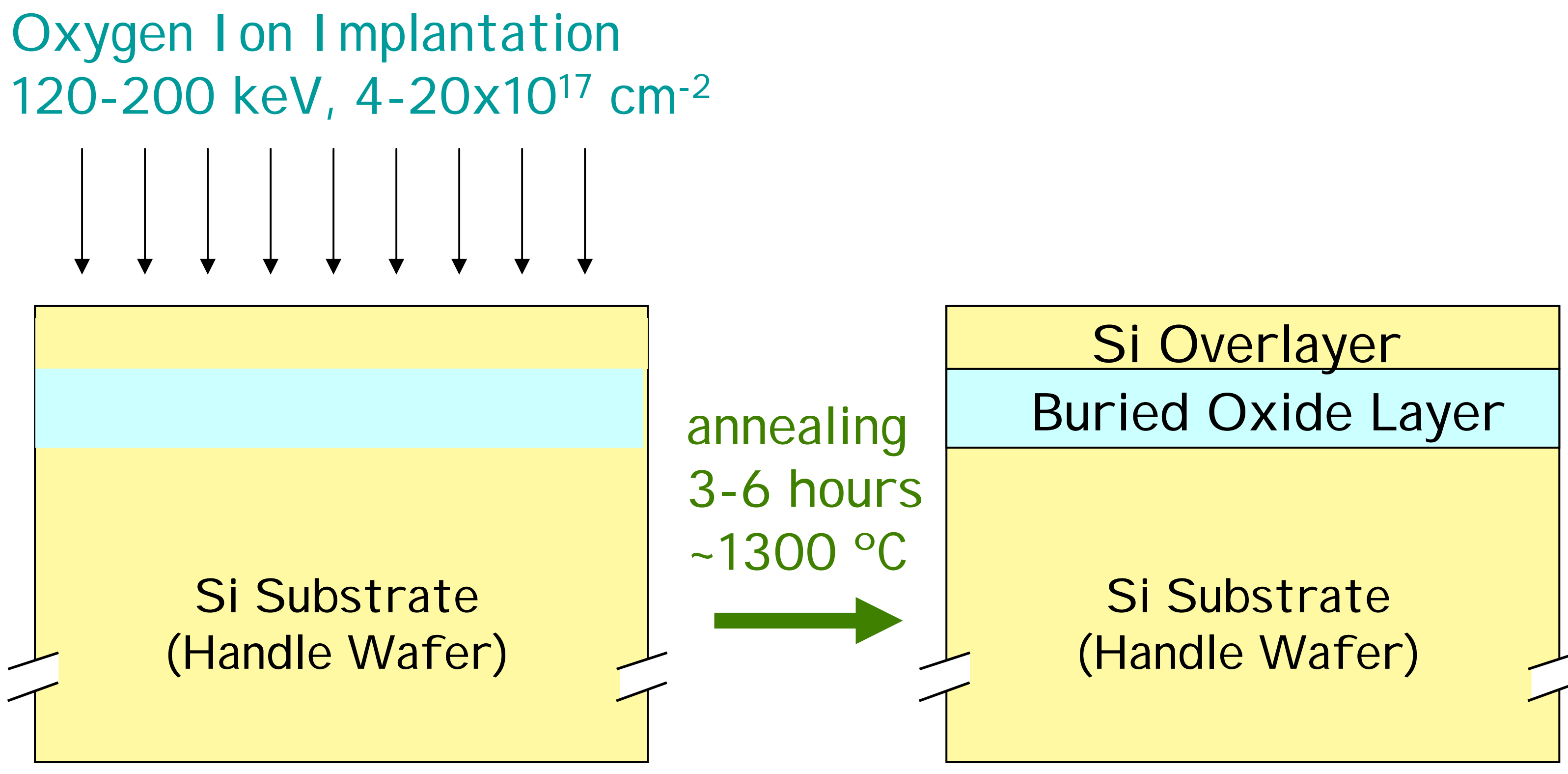
Unfortunately, No Evidence that this device was build and worked.

Bulk and SOI Wafer



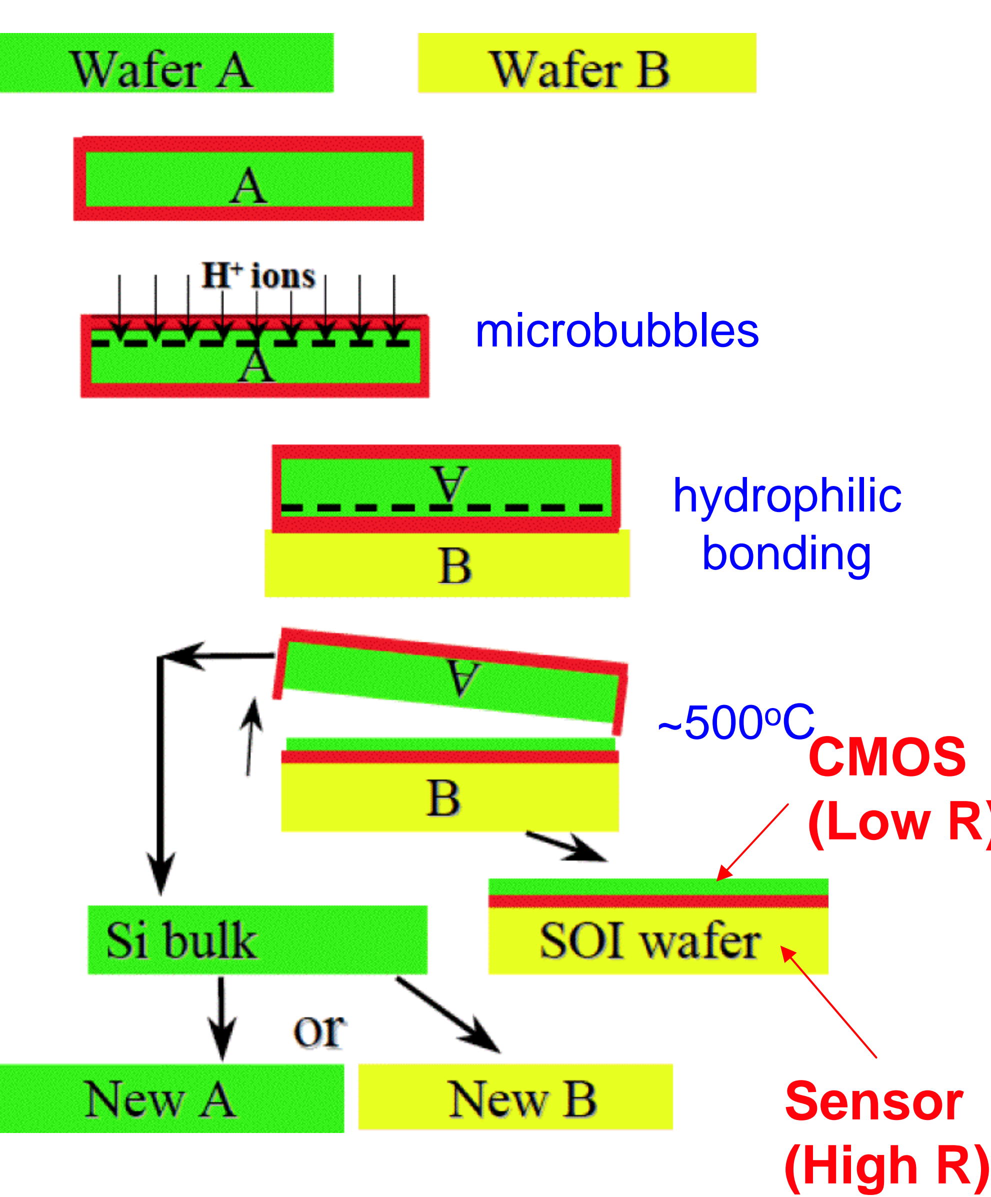
First SOI Wafer for Integrated Circuit

SIMOX (Separation by Implanted Oxygen)
K. Izumi (NTT Japan, 1978)

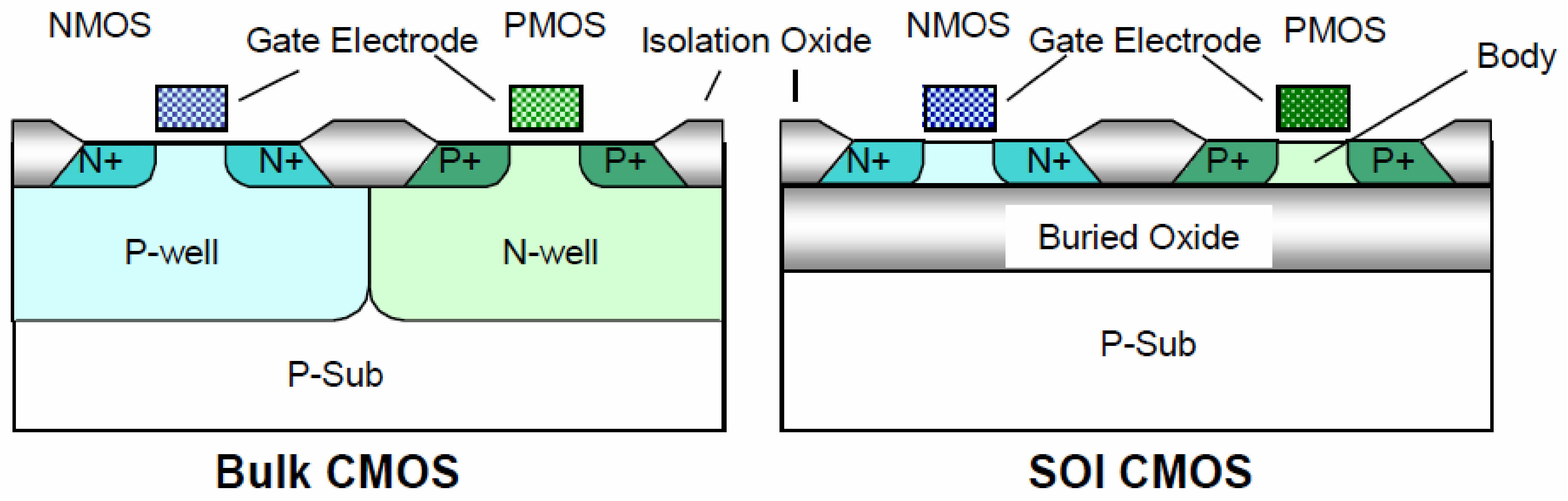


UNIBOND™ Process (1995, France LETI) -> SOITEC

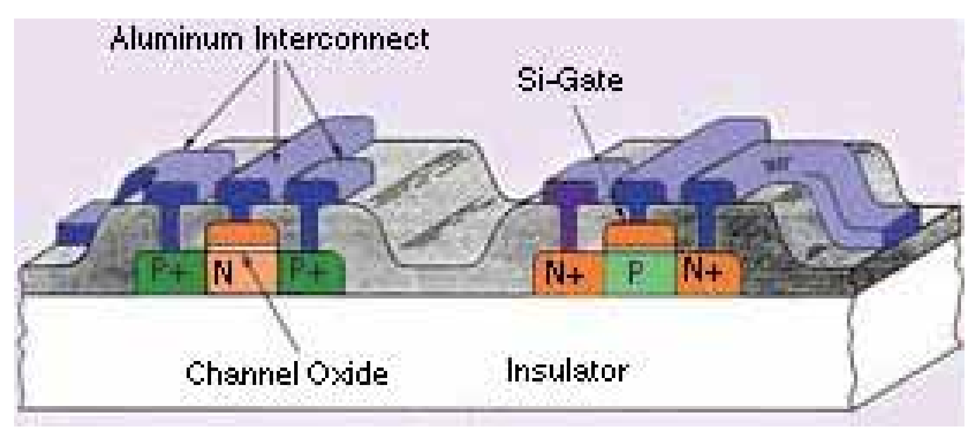
1. Initial silicon wafers A & B
2. Oxidation of wafer A to create insulating layer
3. Smart Cut ion implantation induces formation of an in-depth weakened layer
4. Cleaning & bonding wafer A to the handle substrate, wafer B
5. Smart Cut - cleavage at the mean ion penetration depth splits off wafer A
6. Wafer B undergoes annealing, CMP and touch polish => SOI wafer complete
8. Split-off wafer A is recycled, becoming the new wafer A or B



Bulk CMOS vs. SOI CMOS



In SOI, Each Device is completely isolated by Oxide.



PD-SOI vs. FD-SOI

PD-SOI (Partially Depleted)

◆Thick SOI thickness (T_{SOI})
~100-200nm

◆Depletion layer < T_{SOI}

◇Large floating body effect

◇High drive Current by kink effect

→ High speed application

FD-SOI (Fully Depleted)

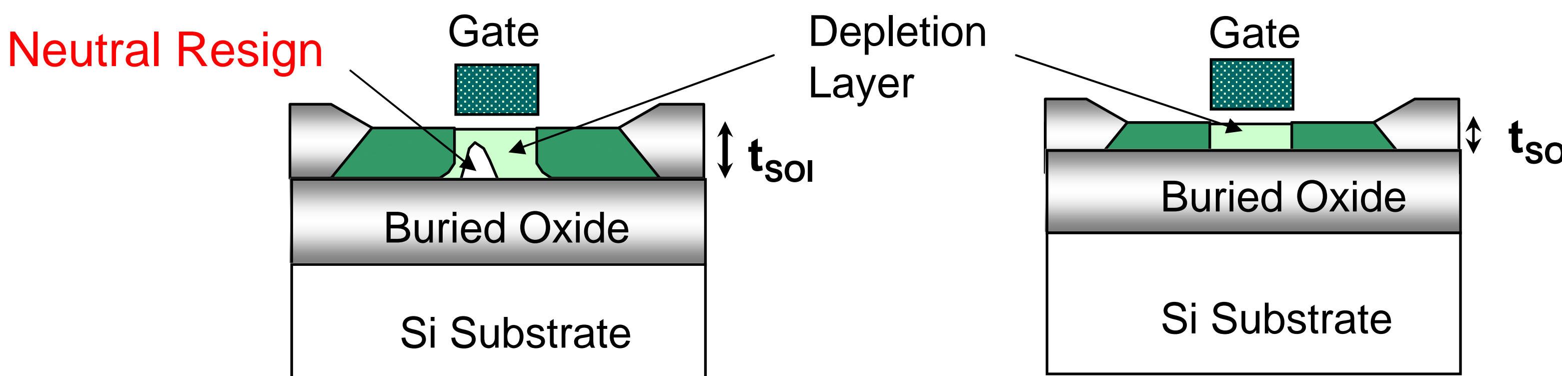
◆Thin SOI thickness (T_{SOI})
< 50nm

◆ Depletion layer > T_{SOI}

◇Less floating body effect

◇Steep subthreshold slopes

→ Low power application



FD-SOI has advantage in performance under very low voltage operation.

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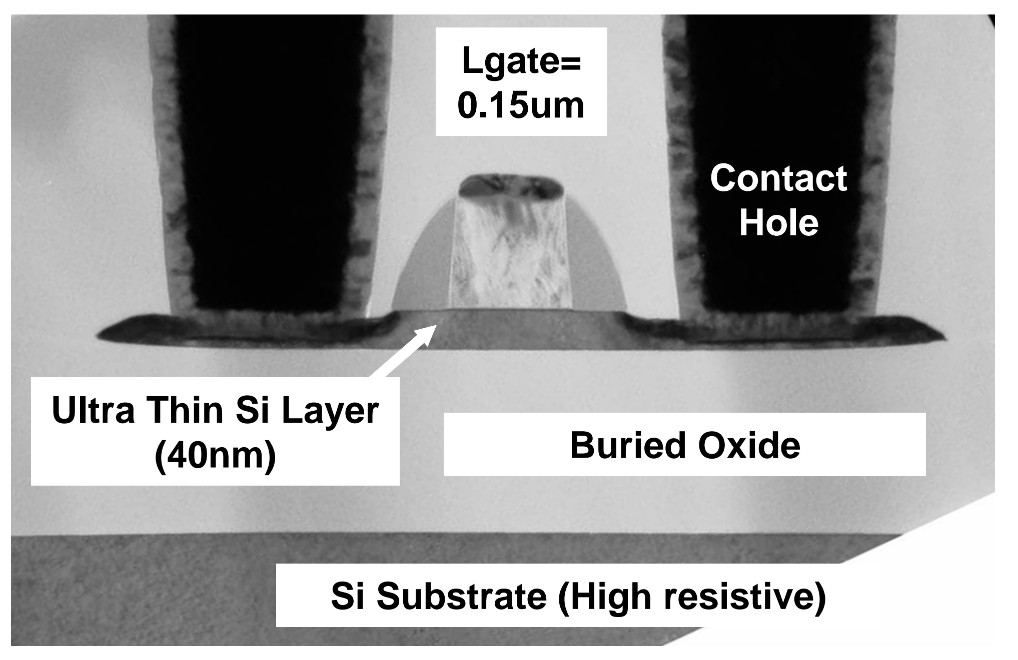
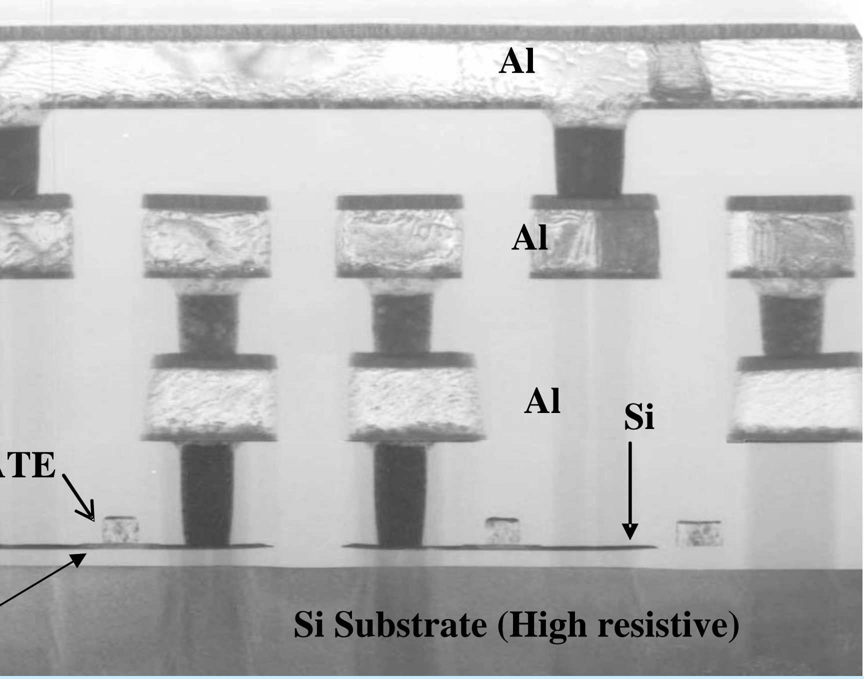
FD-SOI Structure



Close up of MOSFET

Cross Sectional SEM Photograph



Ultra Thin Si Layer (40nm)

Cross Sectional View of FD-SOI Device

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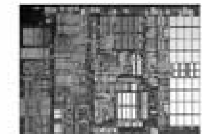
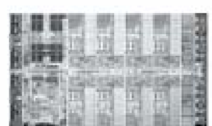
Current Status of PD-SOI and FD-SOI

◆ PD-SOI (Partially Depleted)

High-speed microprocessors

- IBM: PowerPC , mainframe CPU's, Wii(Nintendo), Xbox
- Free scale: PowerPC
- AMD: Athlon processors
- Sony (with IBM and Toshiba) : Cell, PS3

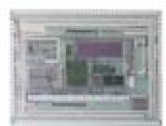




◆ FD-SOI (Fully Depleted)

Low-power application

- Oki: solar cell watch, long-wave RF decoder



Technology Node option beyond 32nm, Next 3D Tr. (R&D)

- Intel, many major companies

At present, only Oki has an experience of mass production of FD-SOI

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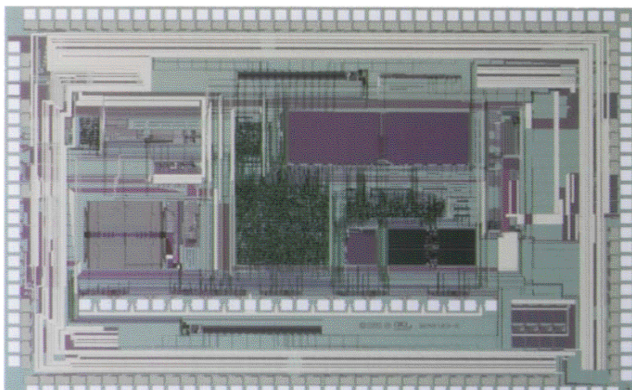
FD-SOI LSI Products for Consumer Market

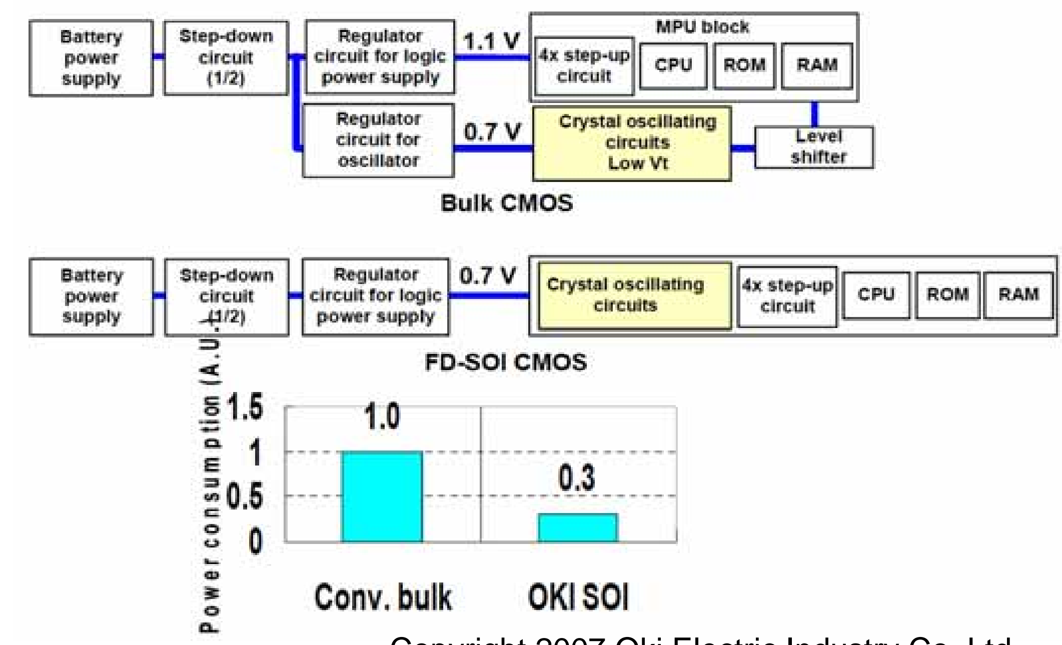
Radio Controlled Solar Watch



http://www.casio.co.jp

This Watch-LSI includes
MCU, SRAM, MROM, Power Unit,
LCD Driver etc in One-chip.

70% Power reduction compared with bulk device



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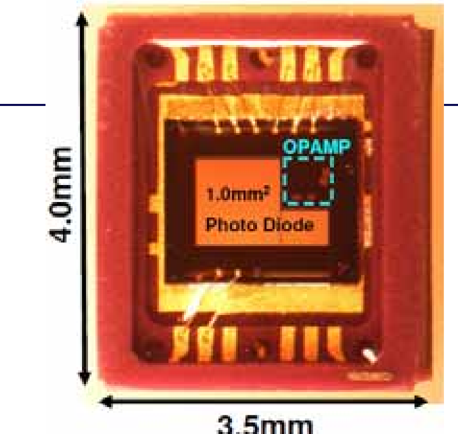
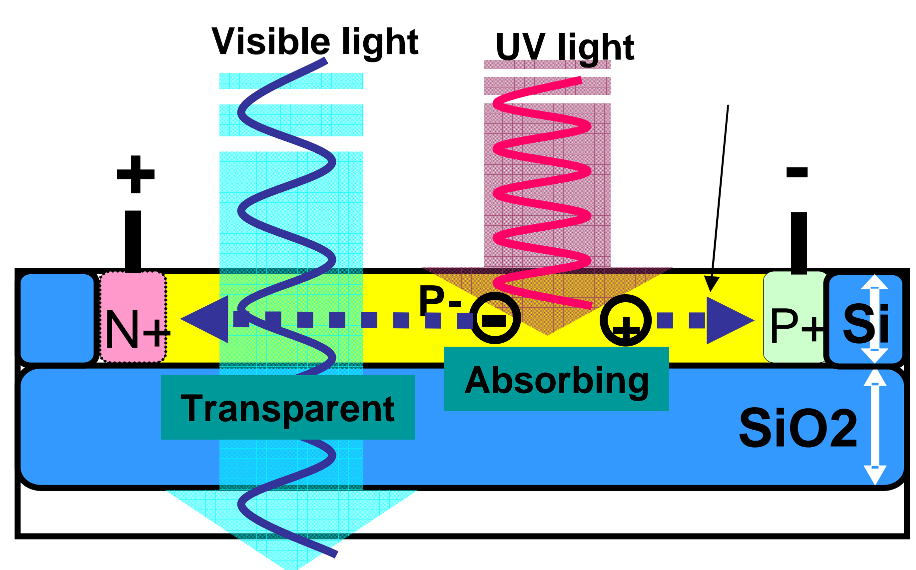
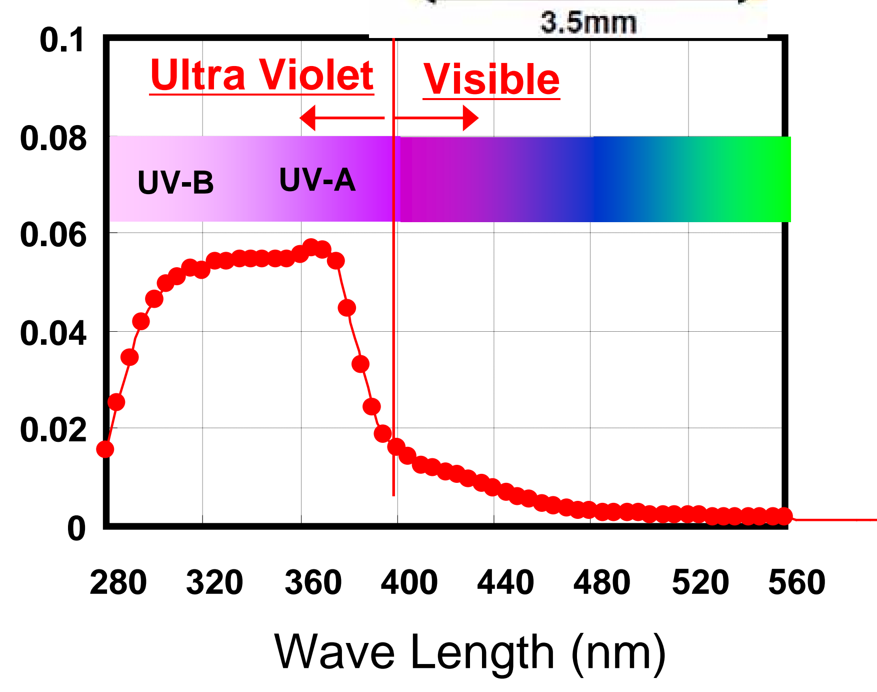
FD-SOI UV Sensor



- ✓UV selective without external filters
- ✓On chip analog / digital circuits
- ✓Very high uniformity



Principal Schema



Spectral of FD-SOI Photo-Diode

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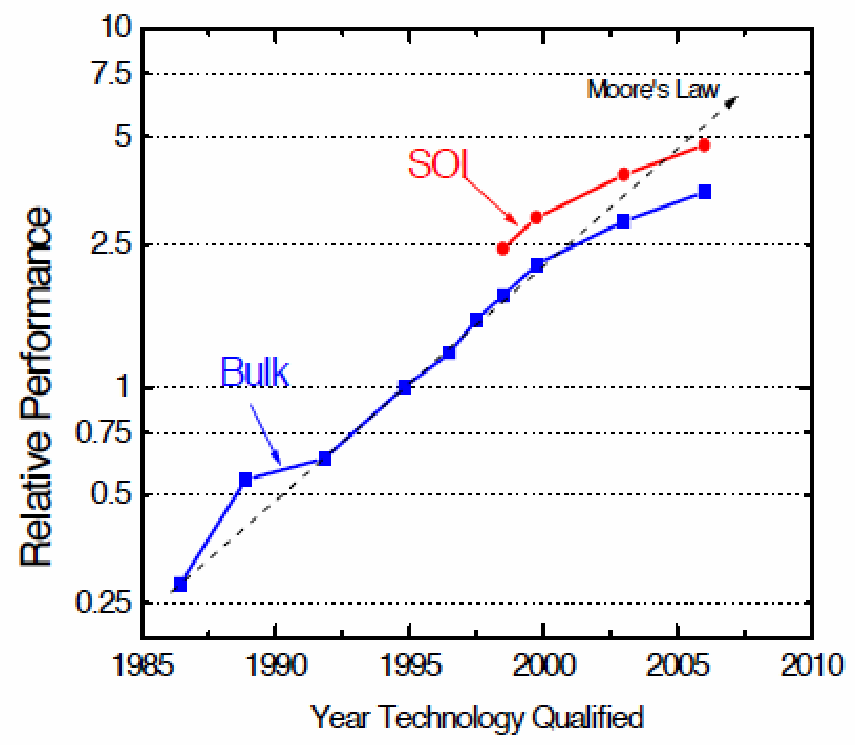
Features of (FD-)SOI

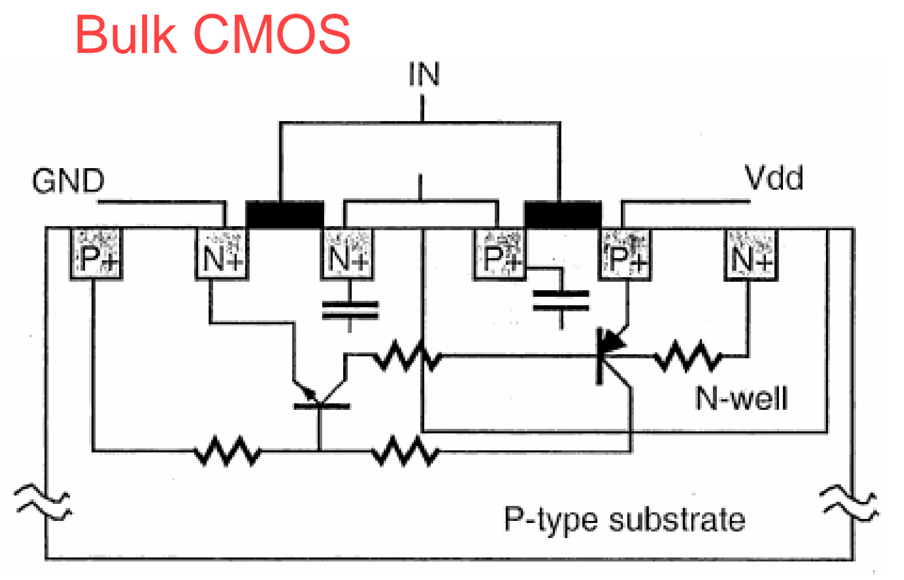
- Full Dielectric Isolation :
  Latchup Free, Small Area,
  Good Circuit Isolation
  No Back Bias Effect
- Low Junction Capacitance :
  High Speed
- Steep Subthreshold Slope
  Low Power
- No Kink Effect
  Good for Analog Desugn
- Less Impurity in Body
  Good Vth Matching,
  Less 1/f Noise



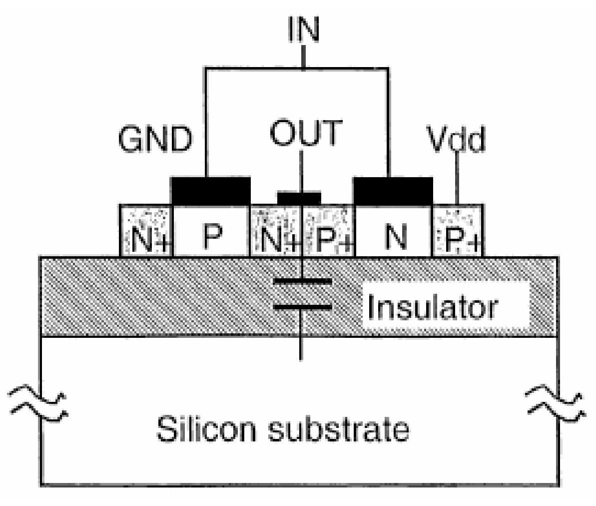
- No Well junction, Thin Film :
  Low Leak,
  Low Vth Shift (High Temp).
- Small Active Volume :
  High Soft Error Immunity
- TID compensation by Back Bias

Latchup Free Structure

Bulk CMOS



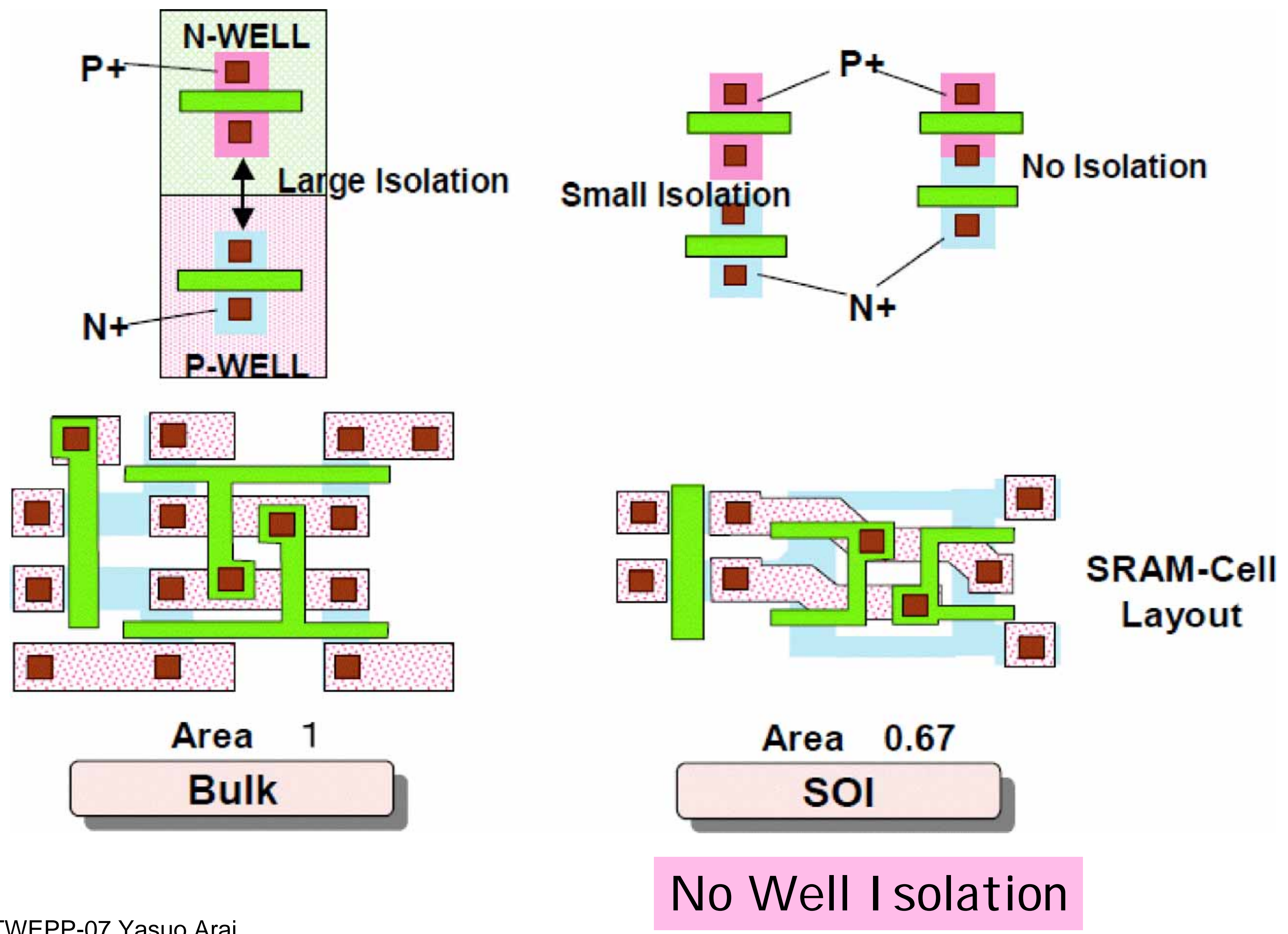
SOI CMOS



(Ref. 'SOI Technology' by Jean-Pierre Colinge, Springer)

No Parasitic PNPN Structure

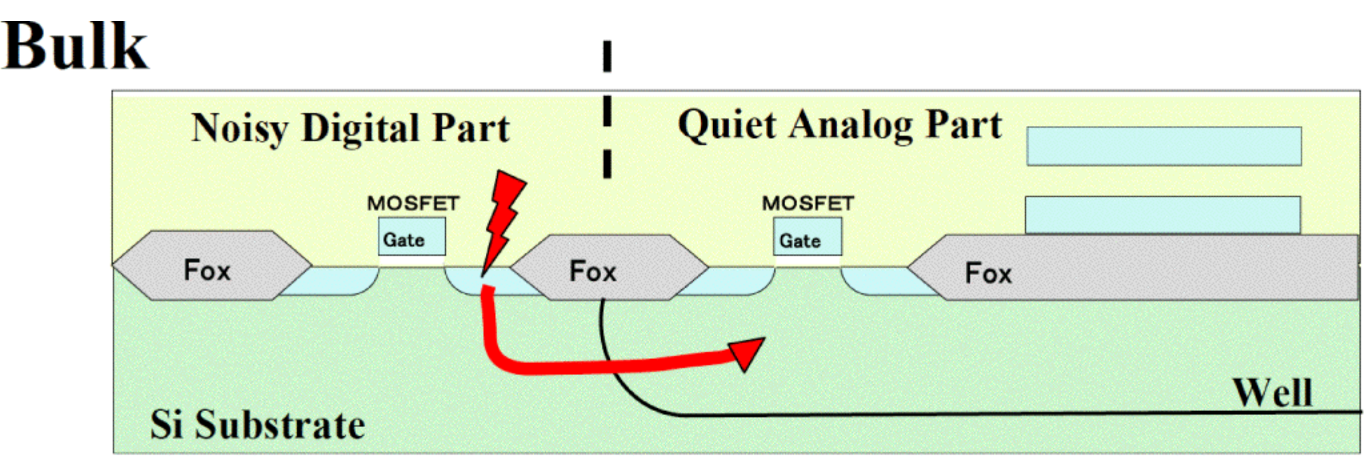
Area reduction by SOI

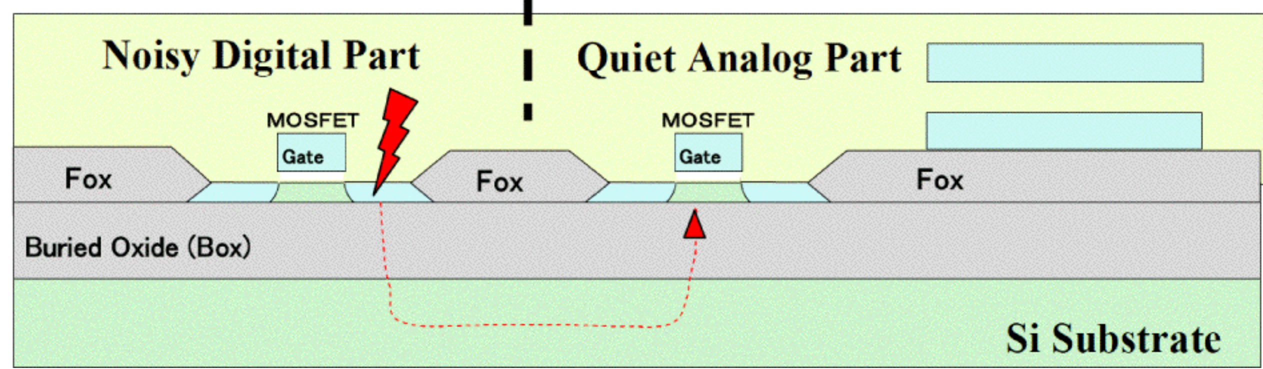


No Well Isolation

Isolation between Analog and Digital Part

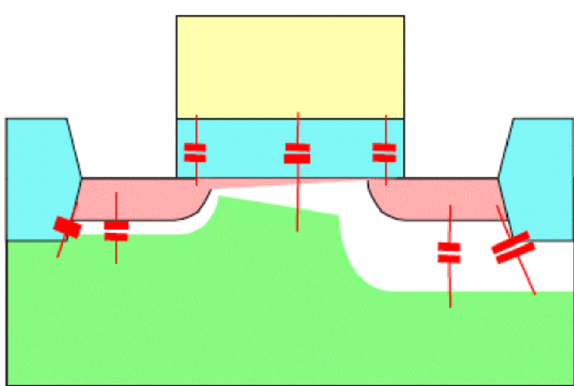
10-40dB lower than Well isolation of Bulk, when High-Resistive Substrate is used



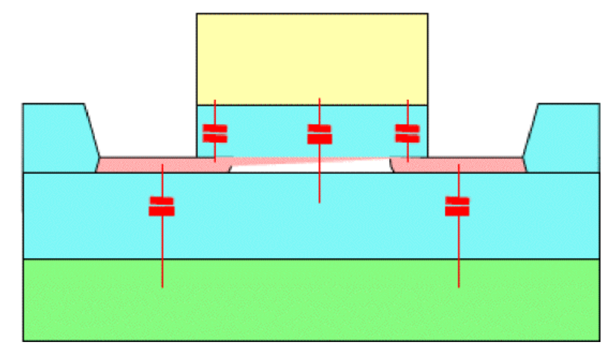


Smaller Junction Capacitance

Bulk



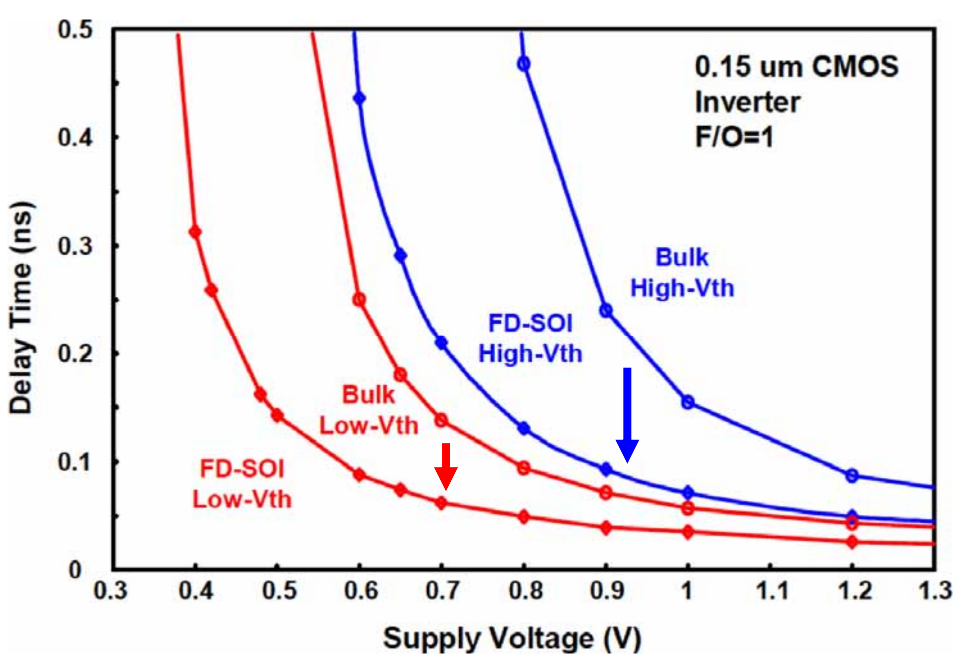
SOI



Cj is 1/10 of Bulk technology.

Gate Capacitance is 30-40% Lower.

High Speed / Low Power



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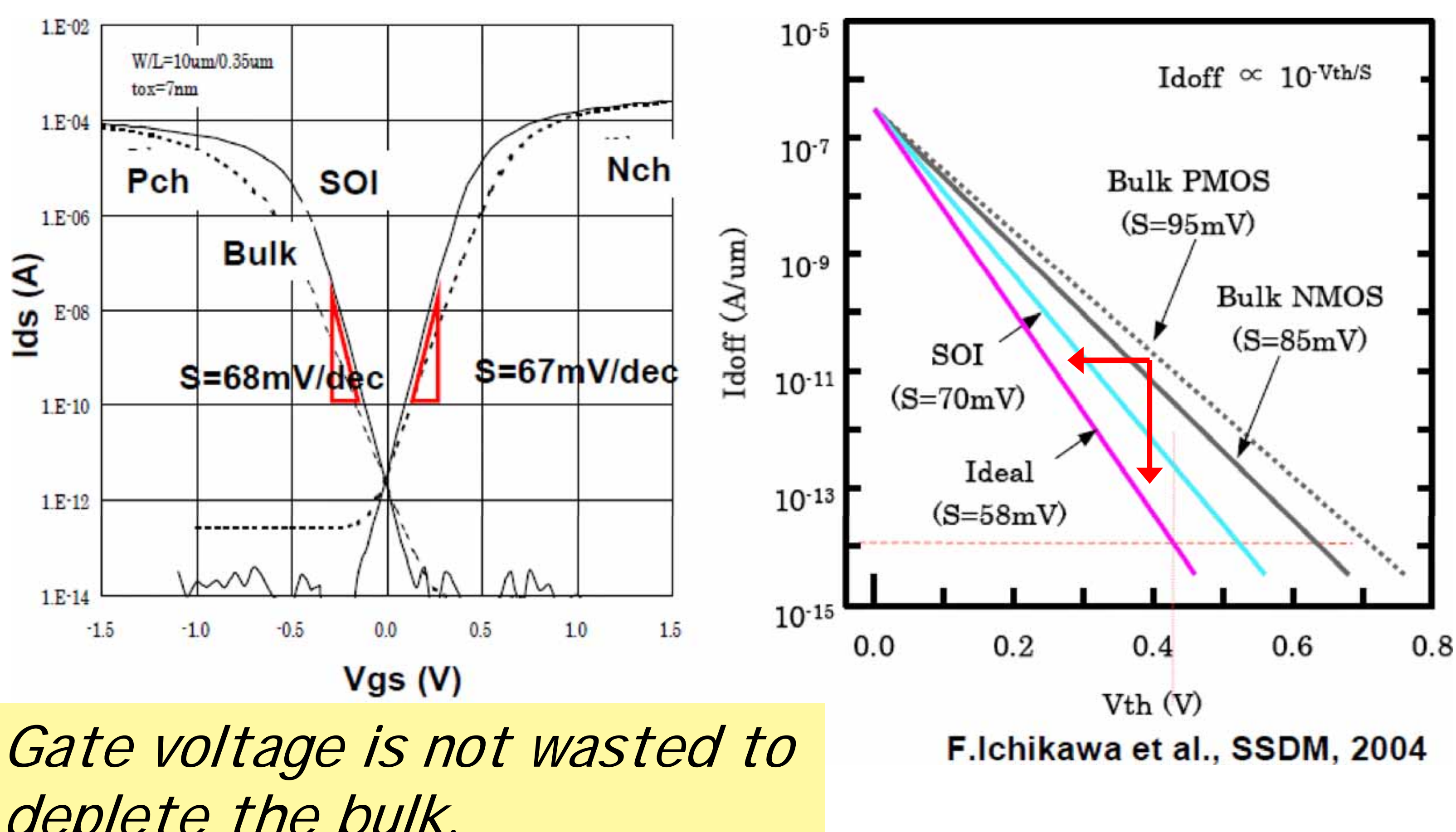
Steep Sub Threshold Slope



Gate voltage is not wasted to deplete the bulk.

Lower Threshold (Leakage Current) is possible without increasing Leakage Current (Vth).

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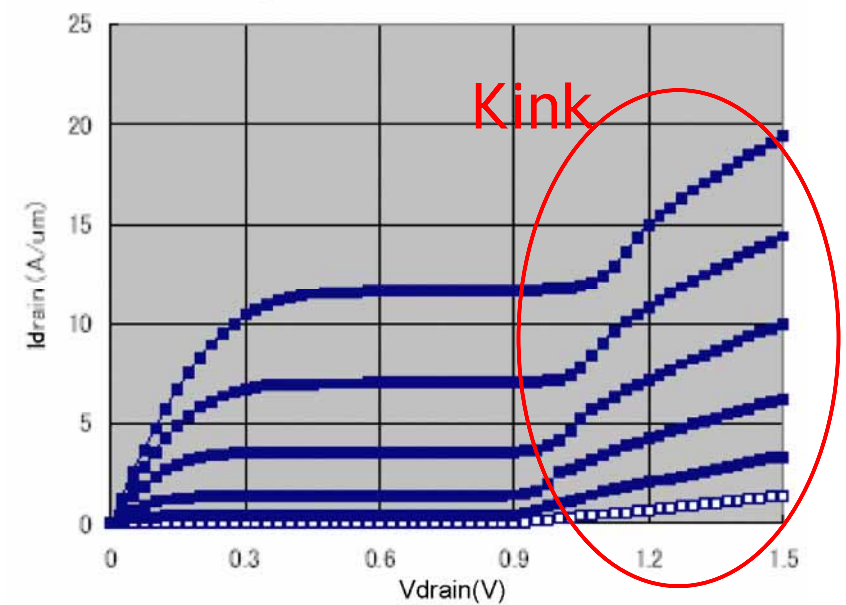
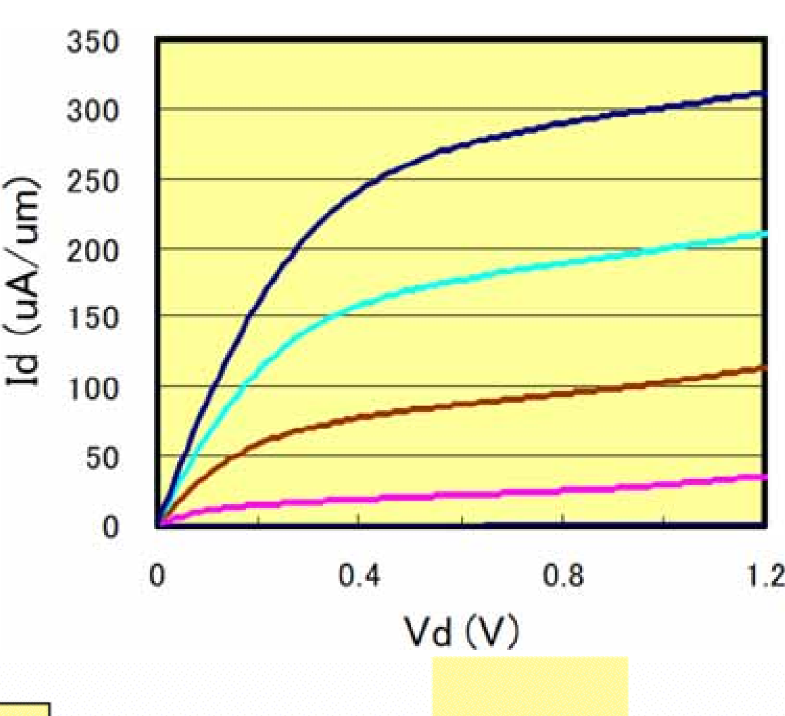
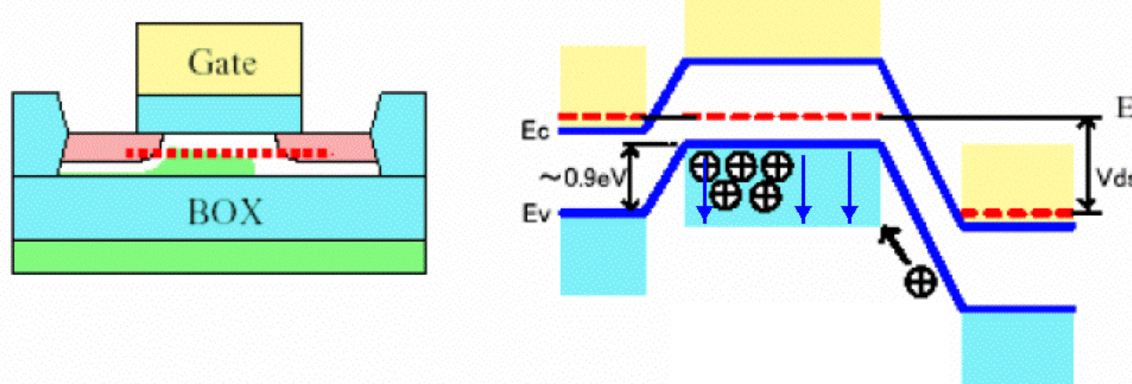
Kink Effect on PD-SOI and FD-SOI

FD-SOI (good for analog)





Impact Ionization create electron-hole near the drain, and increase floating body potential.



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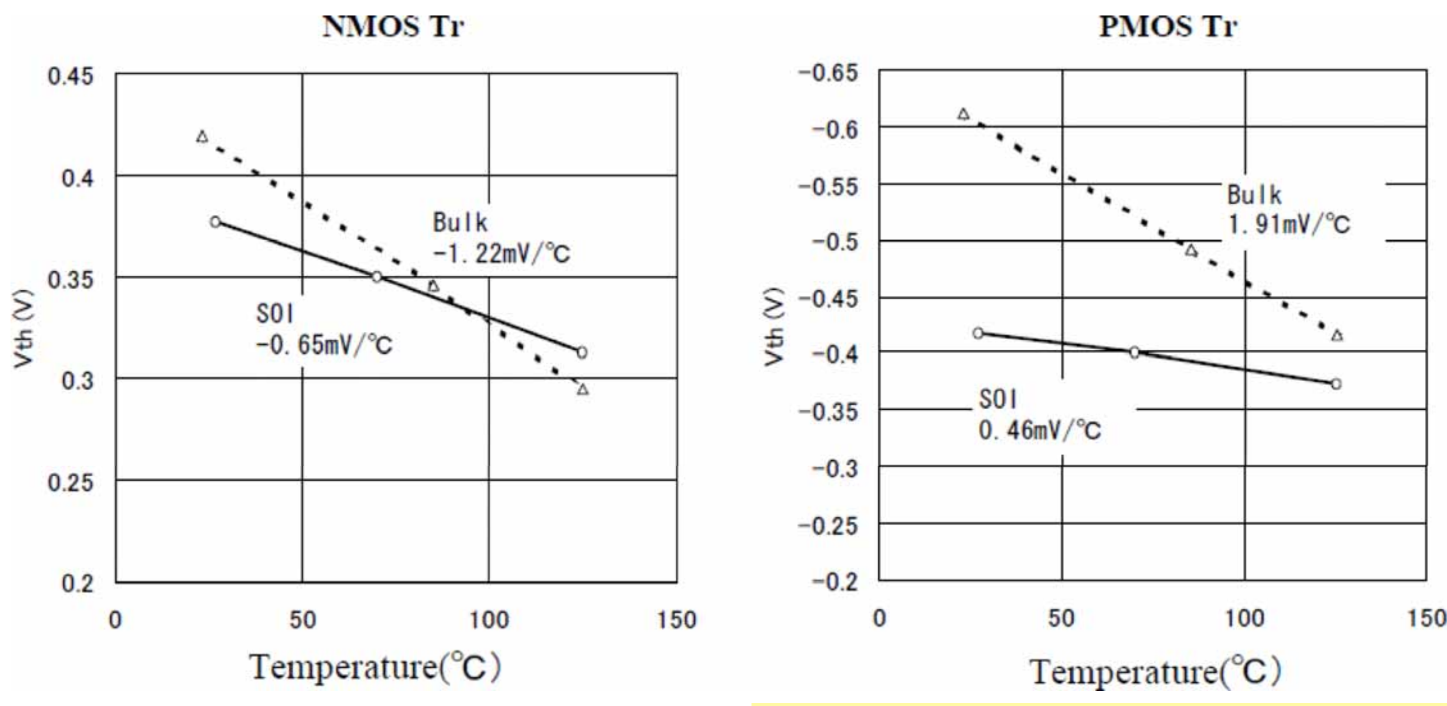
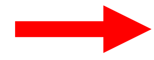
Small Temperature Dependence



due to less change in depletion width

No latchup, Less leakage, Less Vth shift



FD-SOI can be operated in more than 300 C.

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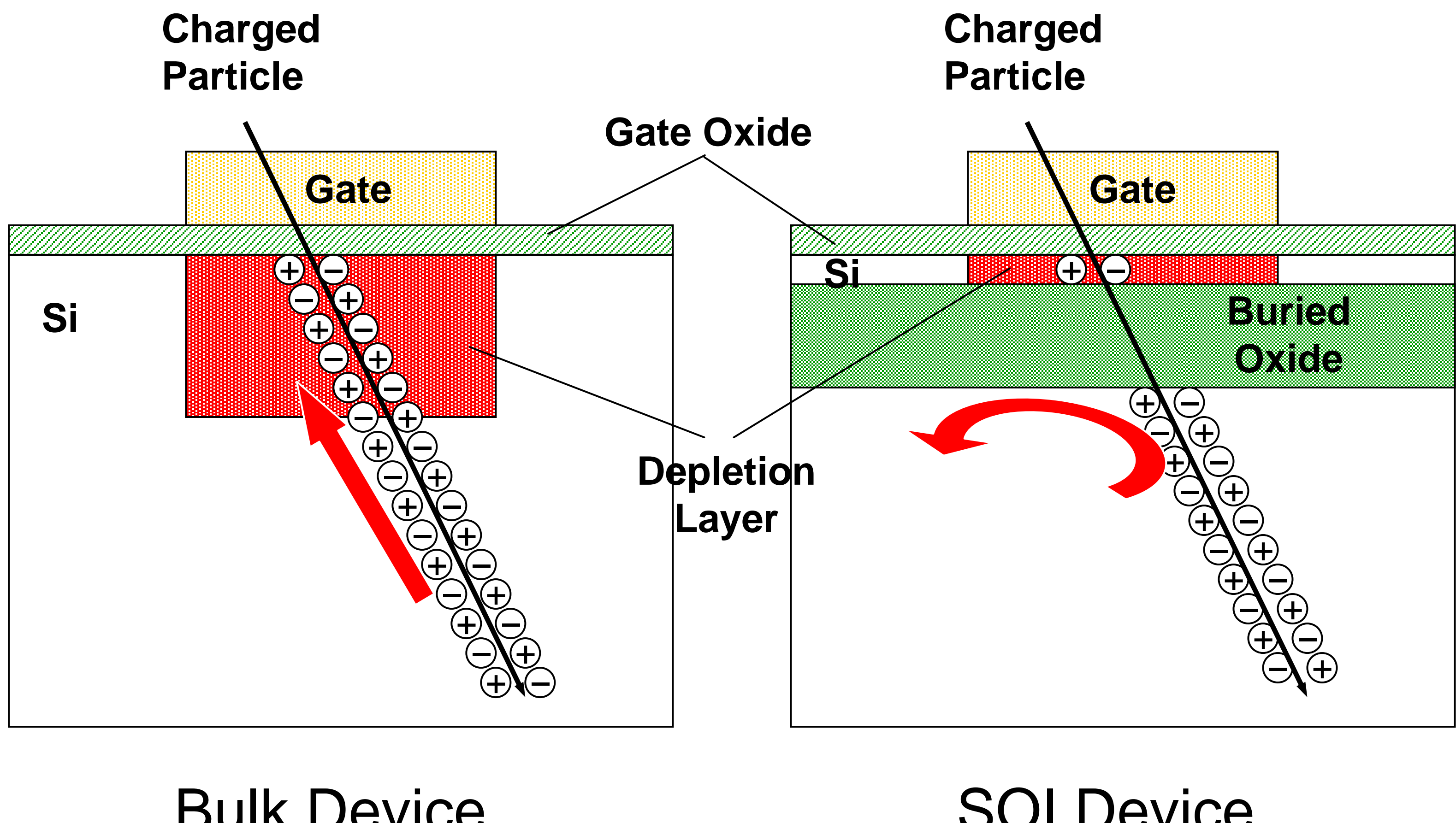
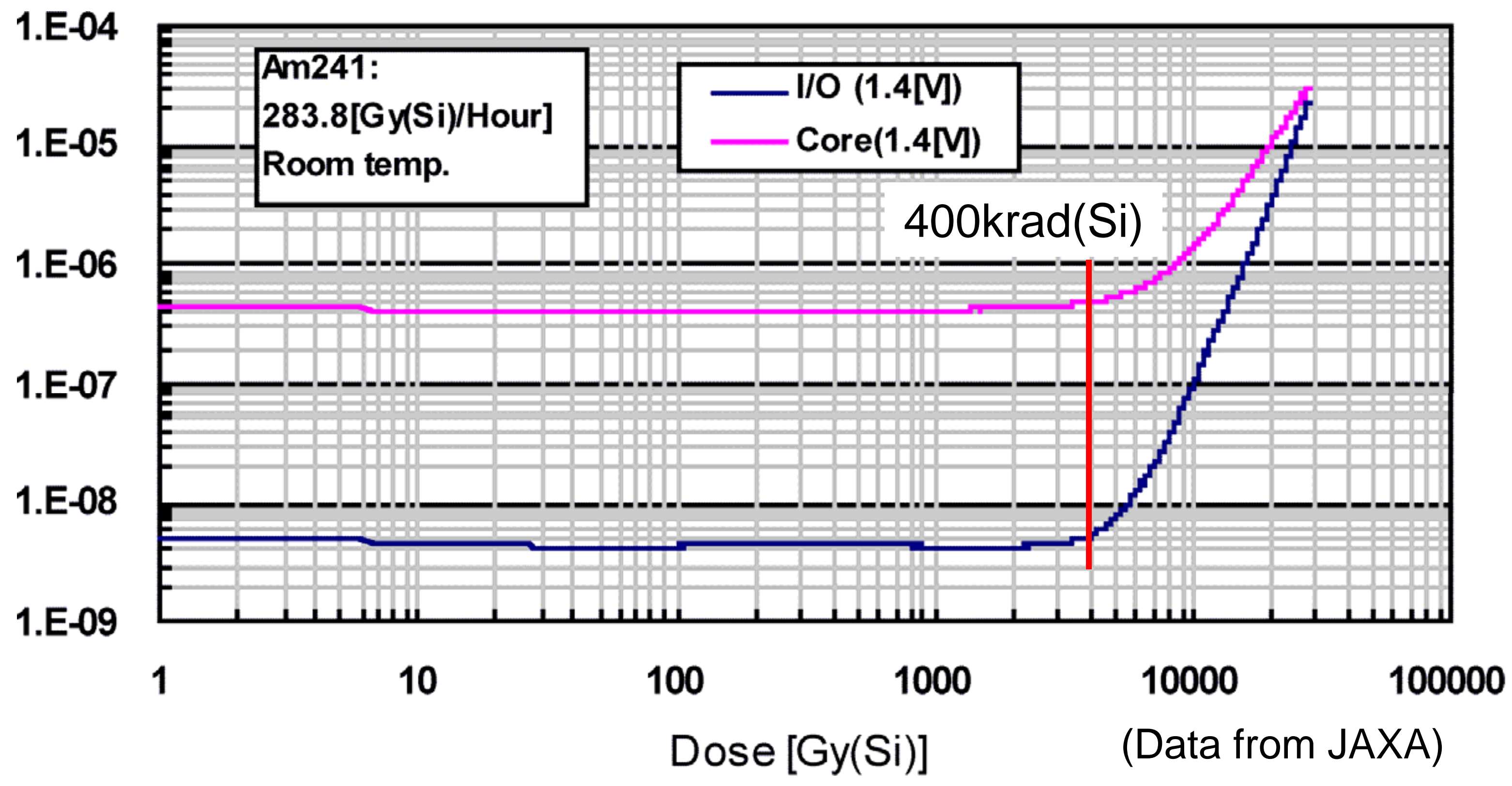
High Soft Error Immunity



Higher soft error immunity due to ultra thin body Silicon.

Total Ionizing Dose

OKI 0.15um FD-SOI



Moderate TID Immunity (enough for space applications).
Charge trapped in BOX shifts Vth.

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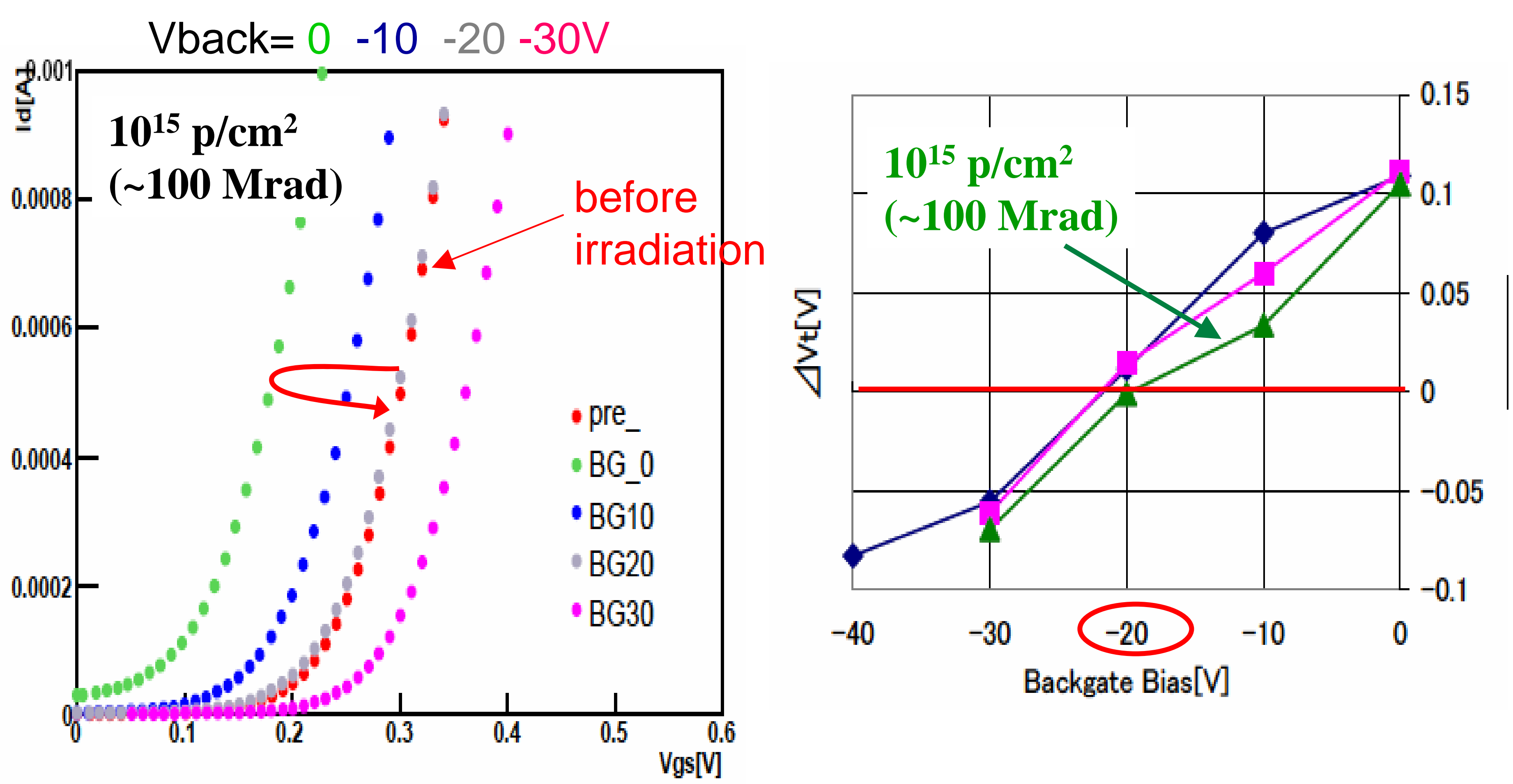
TID(2)

Leak Current and V_{Th} resumes to nearly original value by biasing back side even in 100Mrad.



Summary of this section

- FD-SOI technology has many attractive features:
  Latchup Free,
  Radiation Hardness,
  High Temperature Operation,
  Low Power, ...
  for use in High Energy and Space applications.

but the substrate Si is a simple physical structure

Can we integrate Radiation Sensor?

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Progress of SOI Pixel R&D

Many people are seeking
an ideal pixel detector

High-R Semiconductor Sensor

with

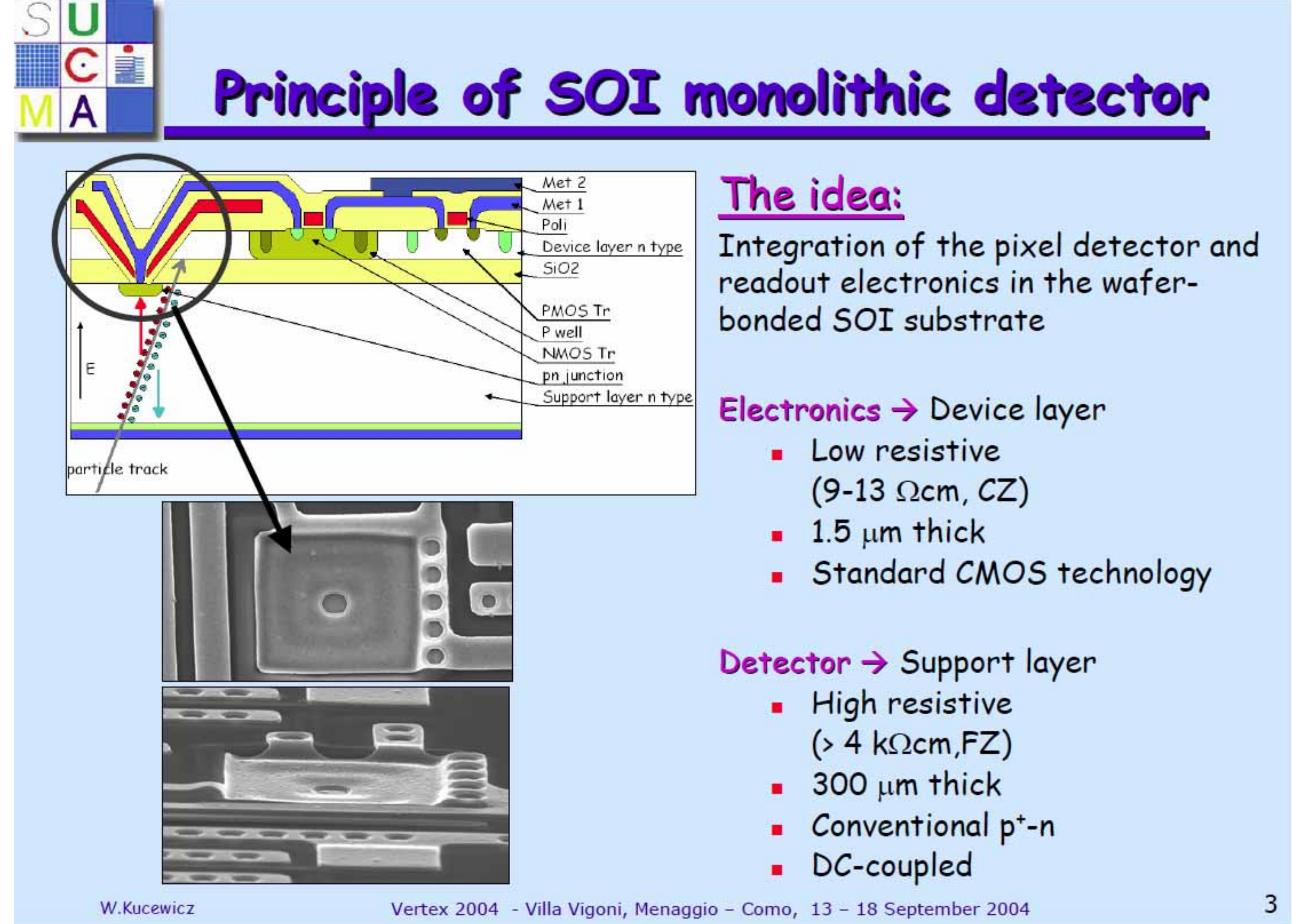
Fully Integrated Amp. and R/O logic

using

Commercially Available Technology

SOI Monolitic Detector!

Pioneering work by SUCIMA



Technology is not so advanced (~3μm technology at Lab.).

KEK SOIPIX R&D History

'05.5: Propose SOI Pixel R&D to KEK Detector Technology Project (Generic R&D).

7: Start Collaboration with OKI Elec. Co. Ltd. for SOI detector R&D .

10: 1st TEG submissions in OKI MPW (Multi Project Wafer) run with *0.15μm* technology.

'06.3: Processes of the 1st TEG were finished.

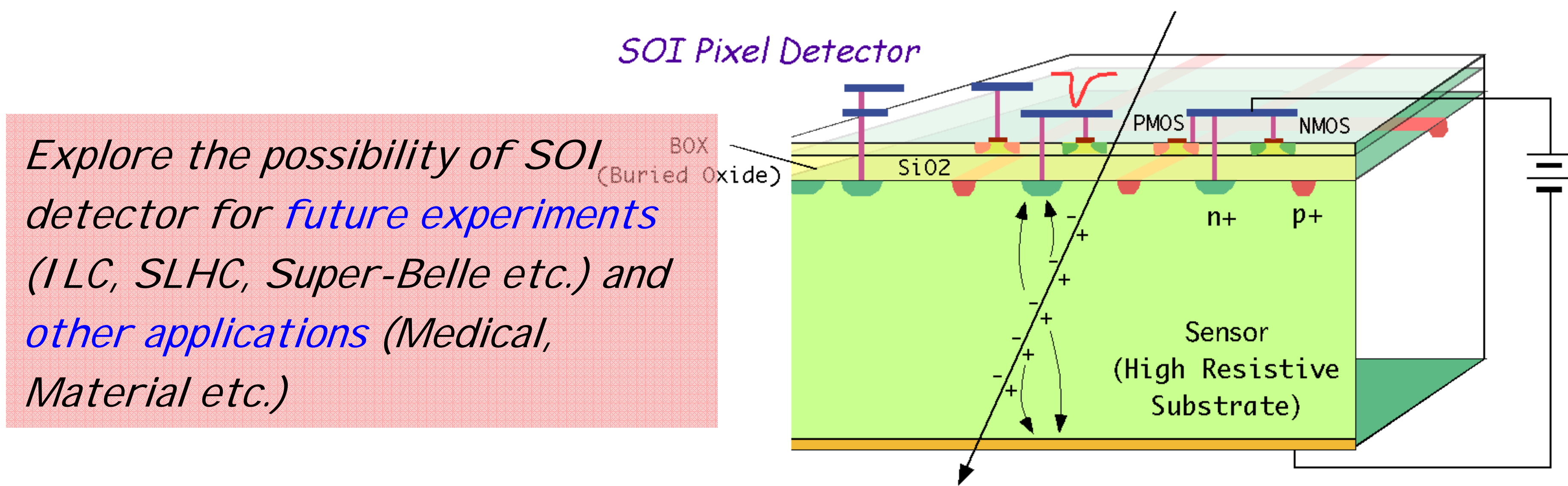
4-8: Good response to Light and β-ray was confirmed.

12: 2nd TEG Submissions hosted by KEK with 17 designs.

'07.4 : Process of the 2nd TEG was finished.

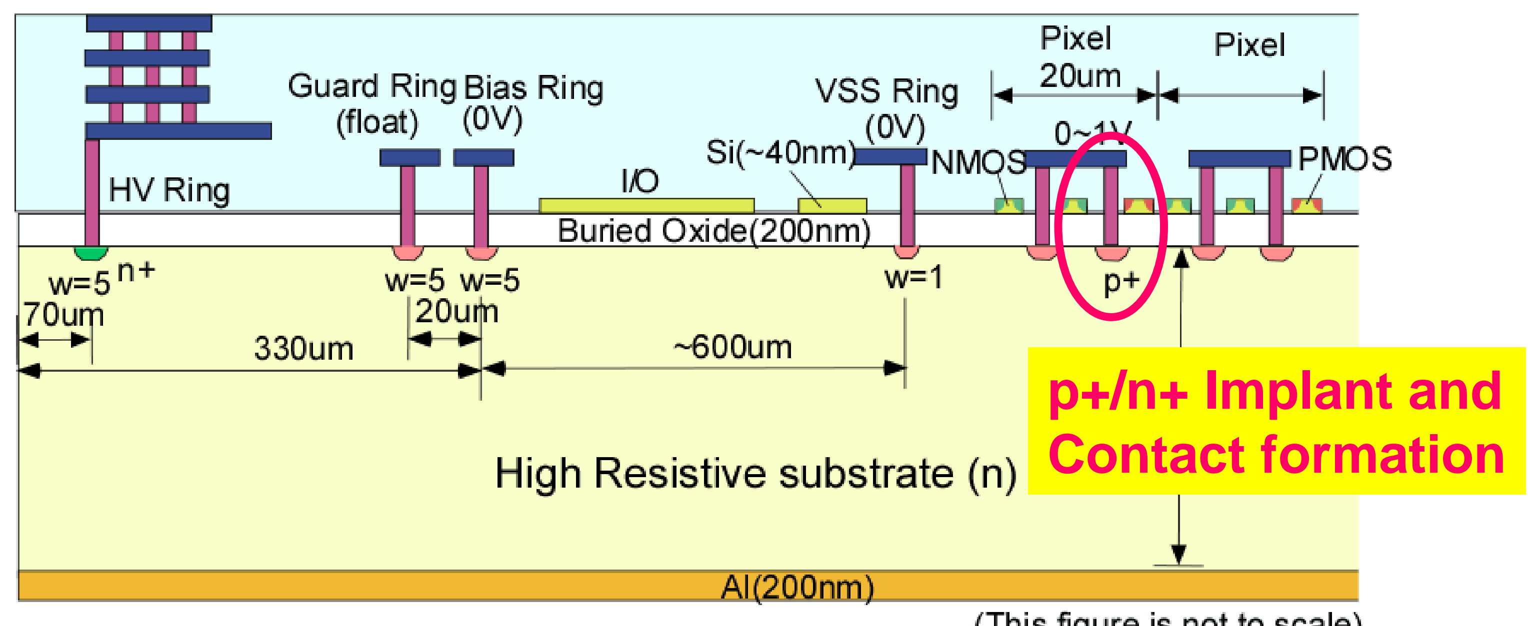
Features of SOI Monolithic Pixel detector

- Bonded Wafer (High Resistive Substrate + Low Resistive Top Si).
- Standard CMOS Electronics (NMOS, PMOS, MIM Cap etc.).
- Monolithic Detector, No Bump Bonds (Lower cost, Thin Device).
- High density (Smaller Pixel Size is possible).
- Small capacitance of the sense node (High gain V=Q/C)
- Industrial standard technology (Cost benefit and Scalability)

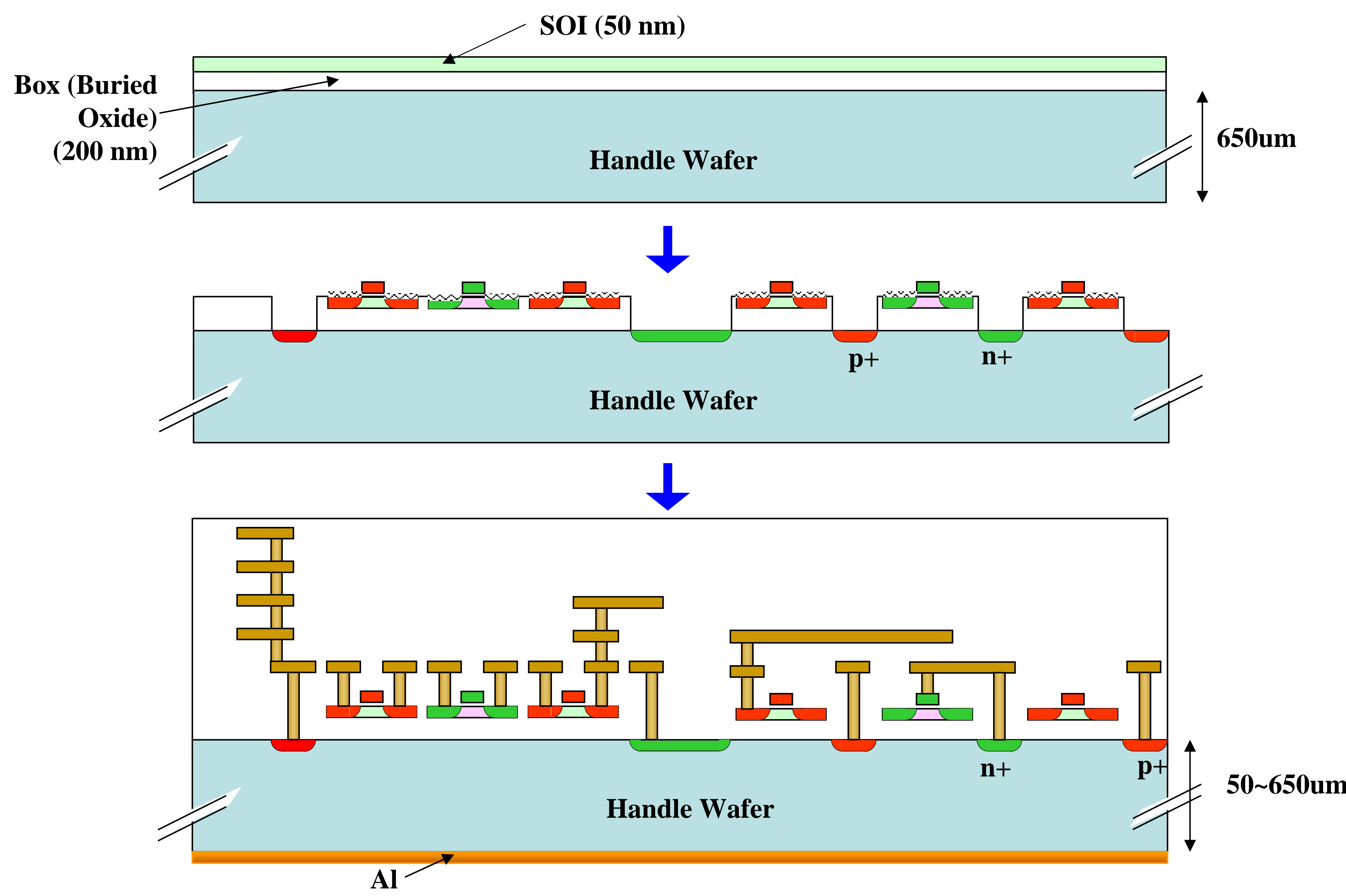


SOI Pixel Process

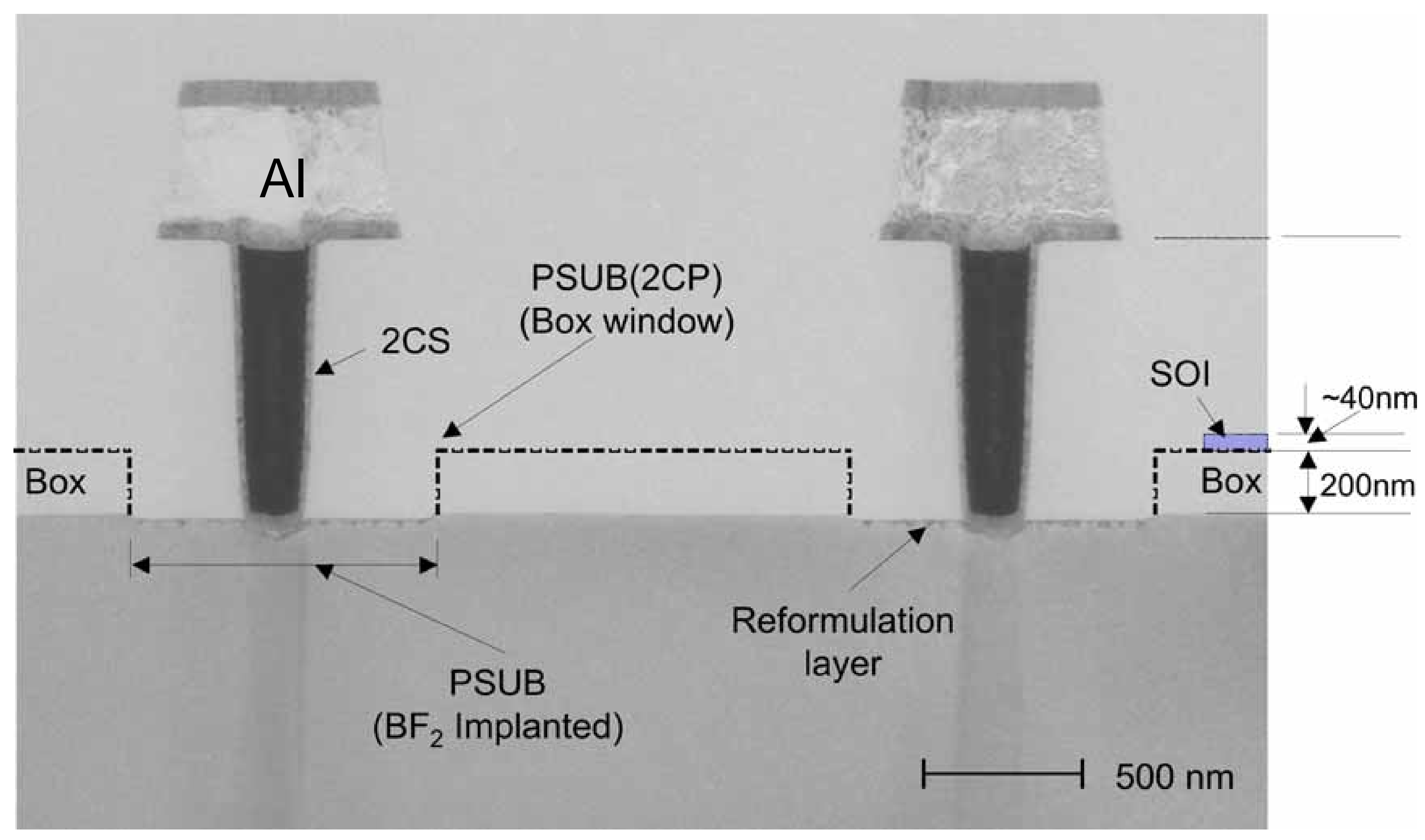
Process	0.15μm Fully-Depleted SOI CMOS process, 1 Poly, 5 Metal layers (OKI Electric Industry Co. Ltd.).
SOI wafer	Wafer Diameter: 150 mmϕ, Top Si : Cz, ~18 Ω-cm, p-type, ~40 nm thick Buried Oxide: 200 nm thick Handle wafer: Cz、 700 Ω-cm (*n-type)*, 650 μm thick (SOITEC)
Backside	Thinned to 350 μm, and plated with Al (200 nm).



SOI Pixel Process Flow



Metal contact & p+ implant



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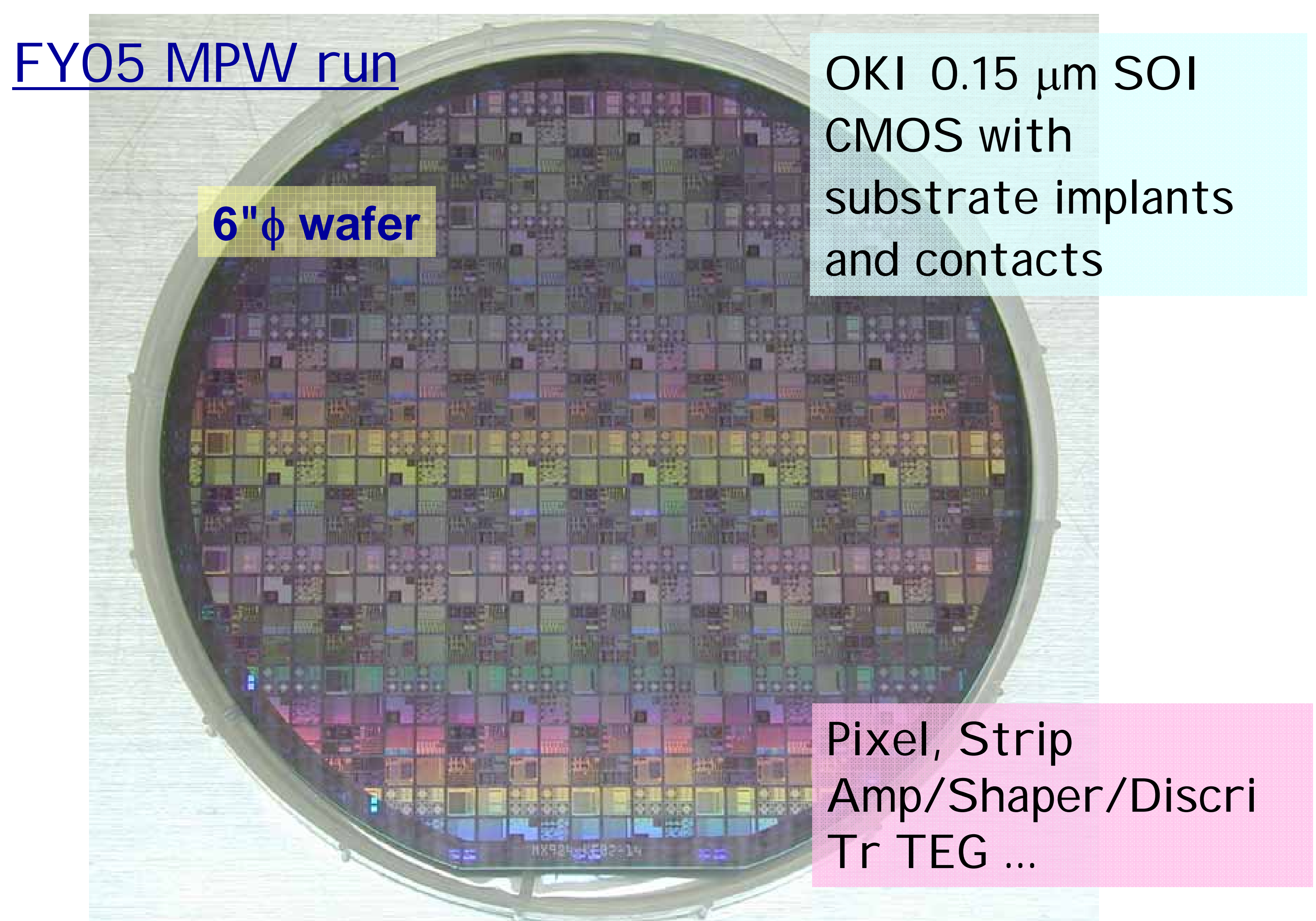
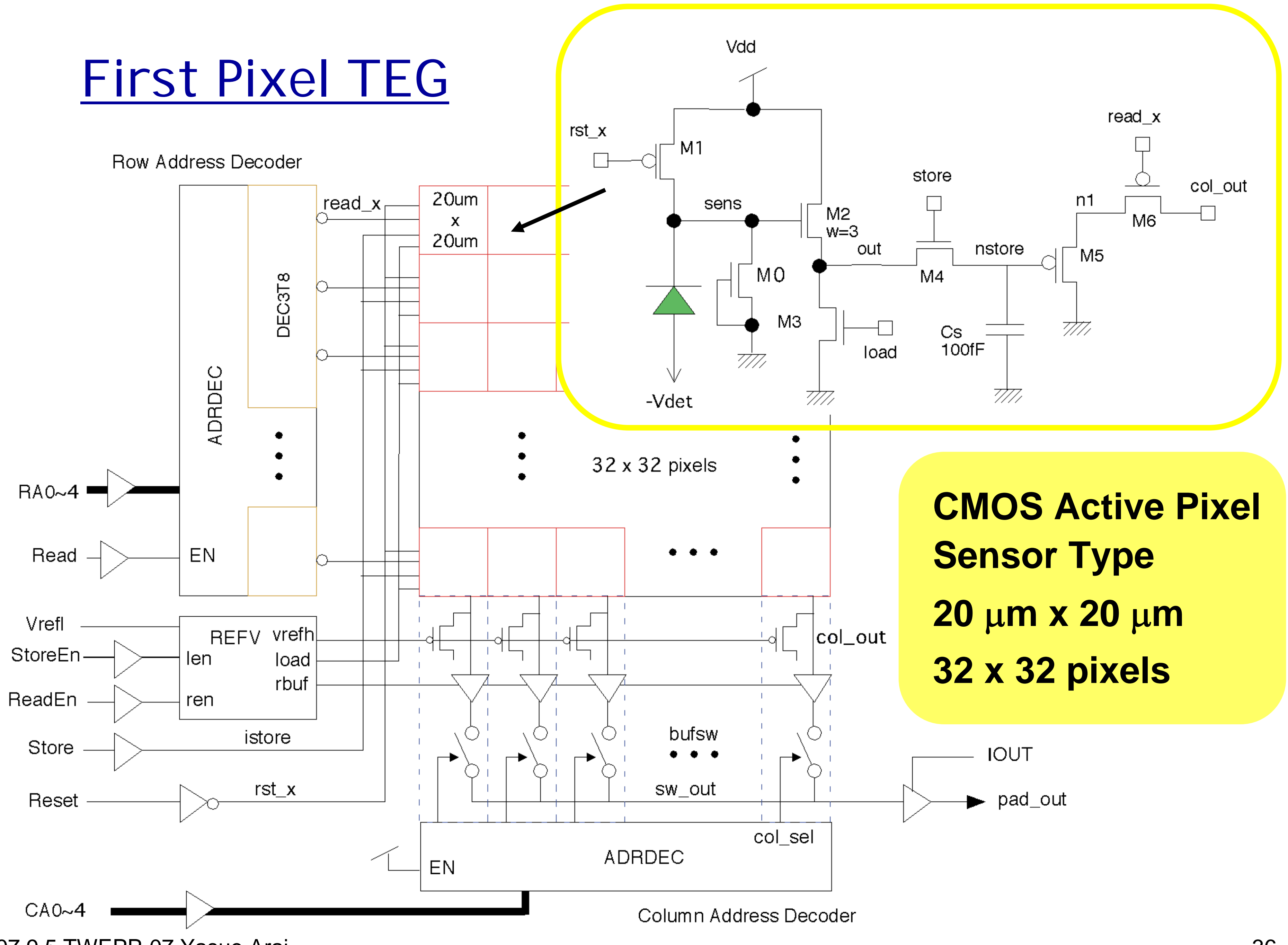

FY05 MPW run
6"ϕ wafer
OKI 0.15 μm SOI
CMOS with
substrate implants
and contacts
Pixel, Strip
Amp/Shaper/Discri
Tr TEG …

First Pixel TEG

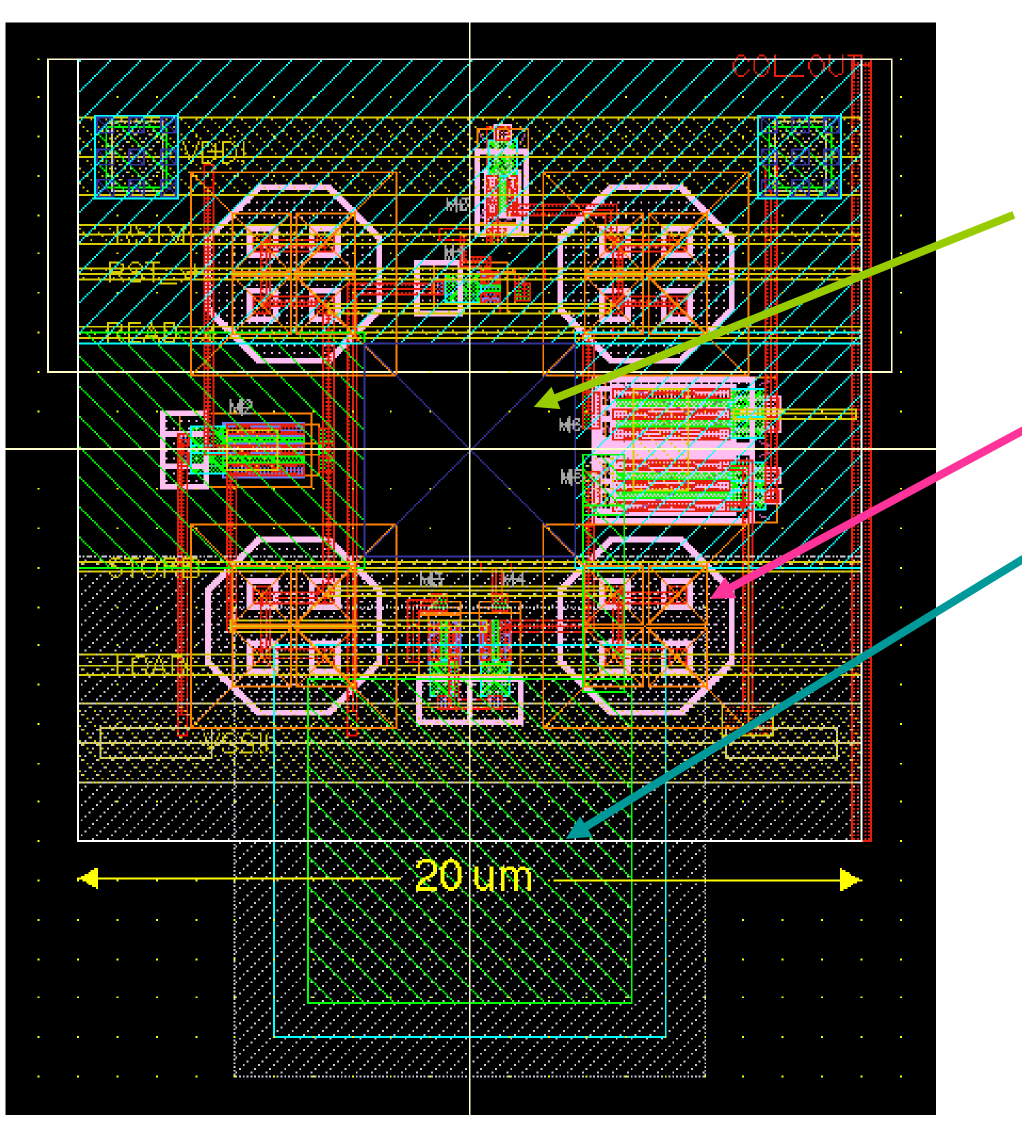


CMOS Active Pixel Sensor Type

20 μm x 20 μm

32 x 32 pixels

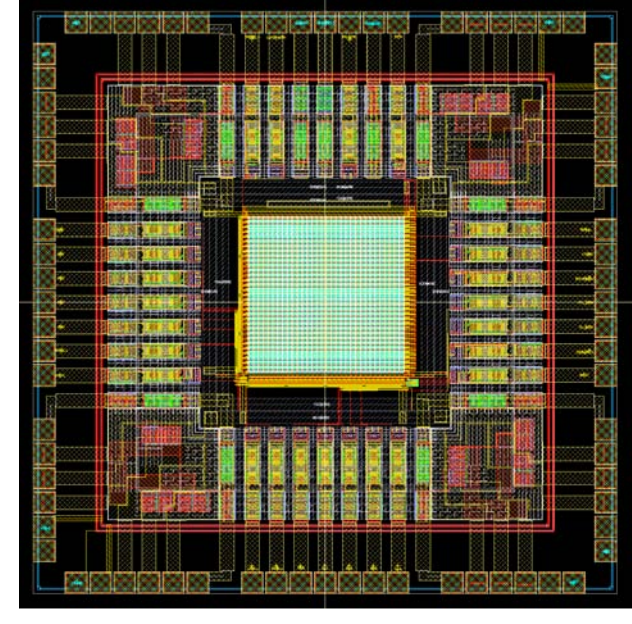
Pixel Layout



Window for Light Illumination ($5.4 \times 5.4\ um^2$)

p+ junction

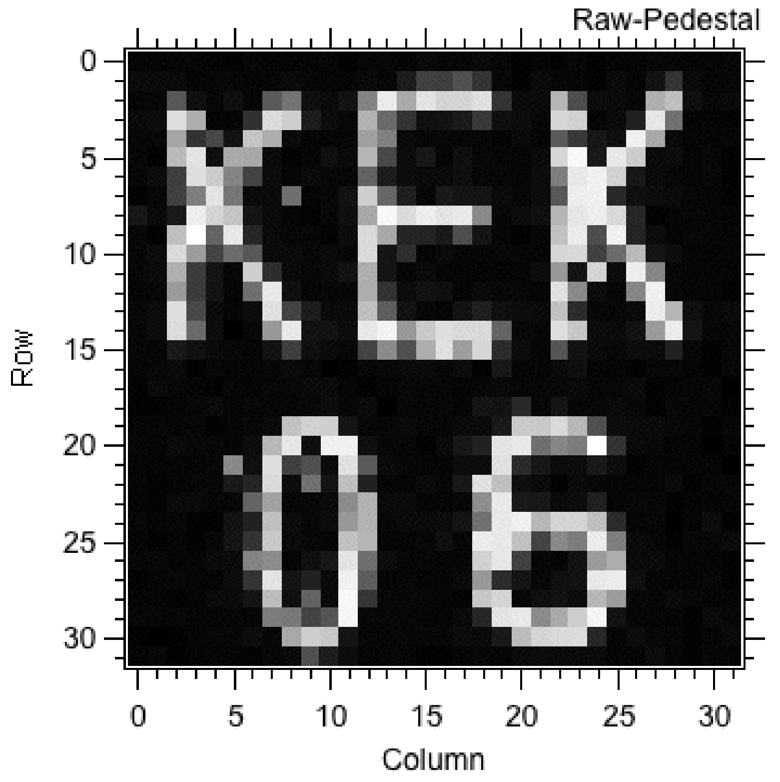
Storage Capacitance(100 fF)



$2.5 \times 2.5\ mm^2$

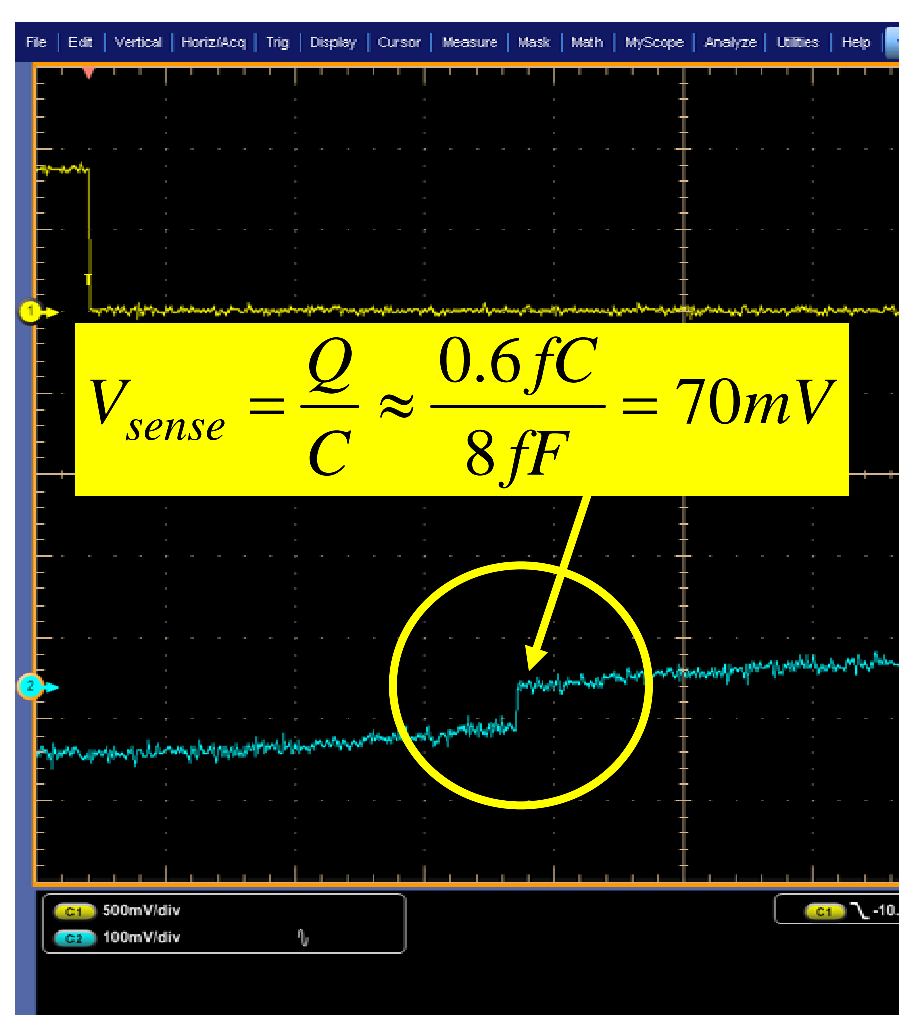
Laser Image

32x32 image view with 670nm Laser and plastic mask



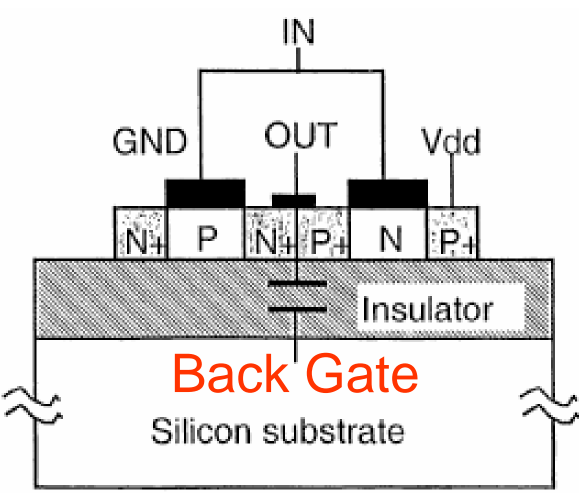
Vdet = 10 V, Exposure Time = 7 ms

β-ray (^{90}Sr) Signal

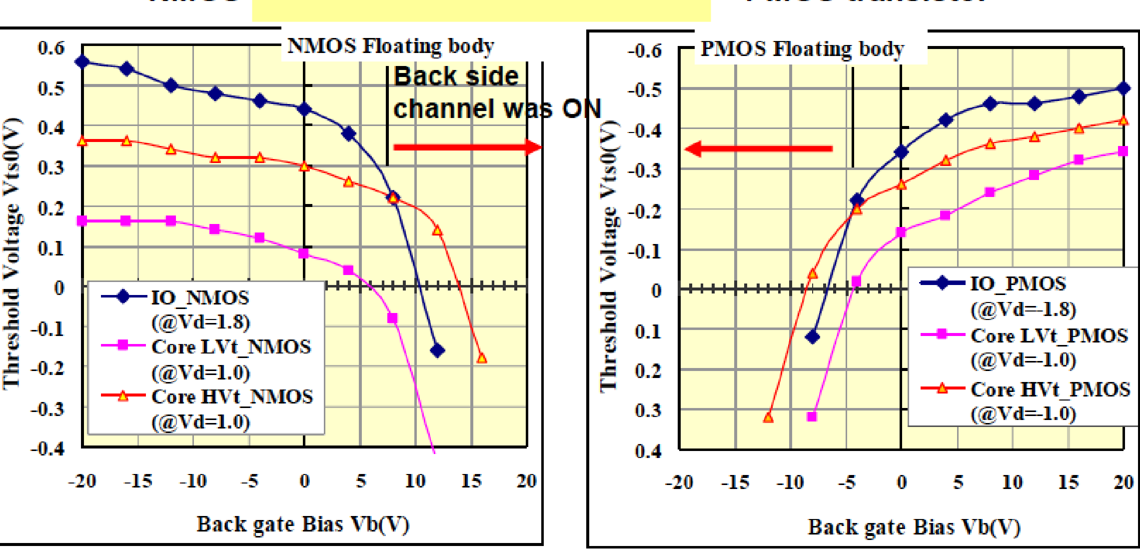


$$V_{sense} = \frac{Q}{C} \approx \frac{0.6\,fC}{8\,fF} = 70mV$$

Back Gate Effect



NMOS Threshold Variation PMOS transistor



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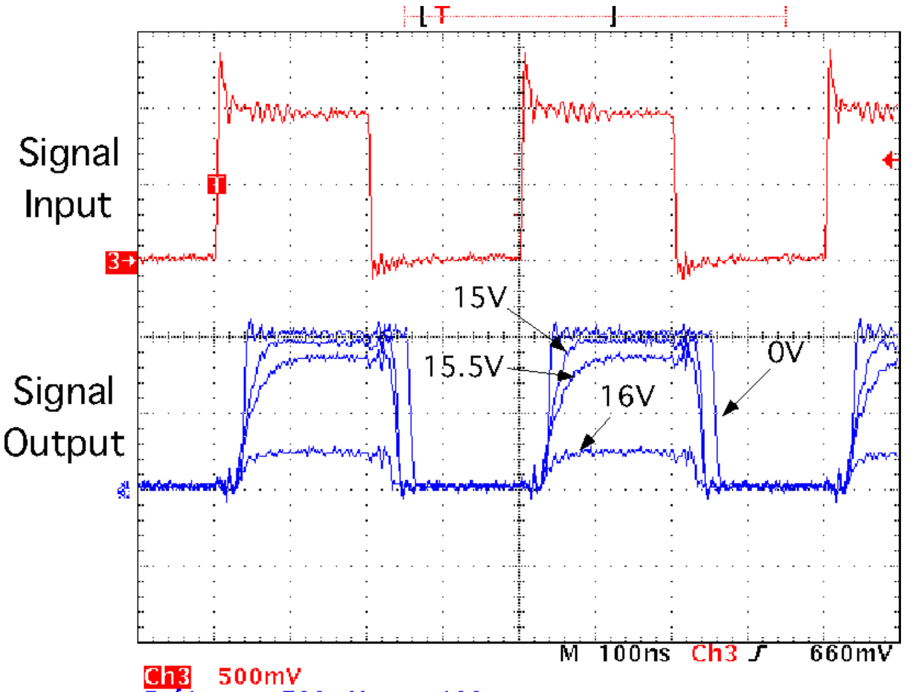


Substrate Voltage act as Back Gate, and change transistor threshold.

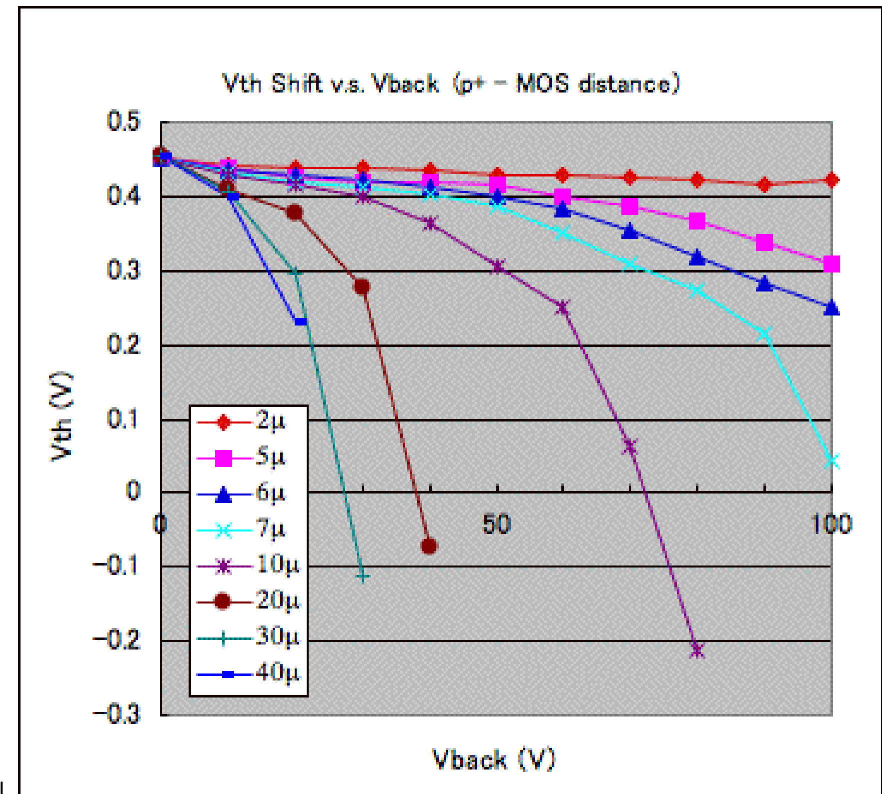
Signal disappeared at V_{det}=16V due to the back gate effect.

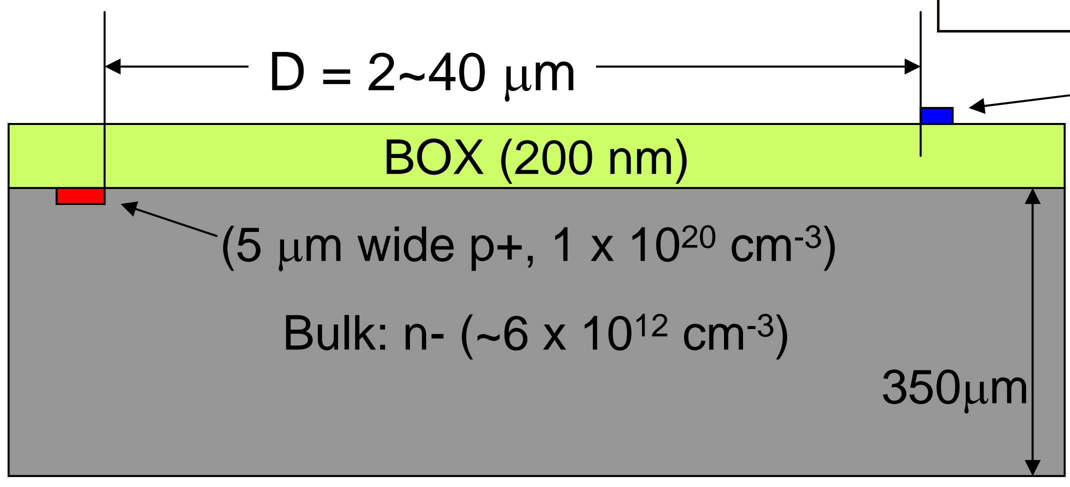
TCAD Simulations

ENEXSS :

3D TCAD Simulator developed by SELETE Consortium Japan.

Back Gate effect can be reduced by placing p+ implant near transistors.

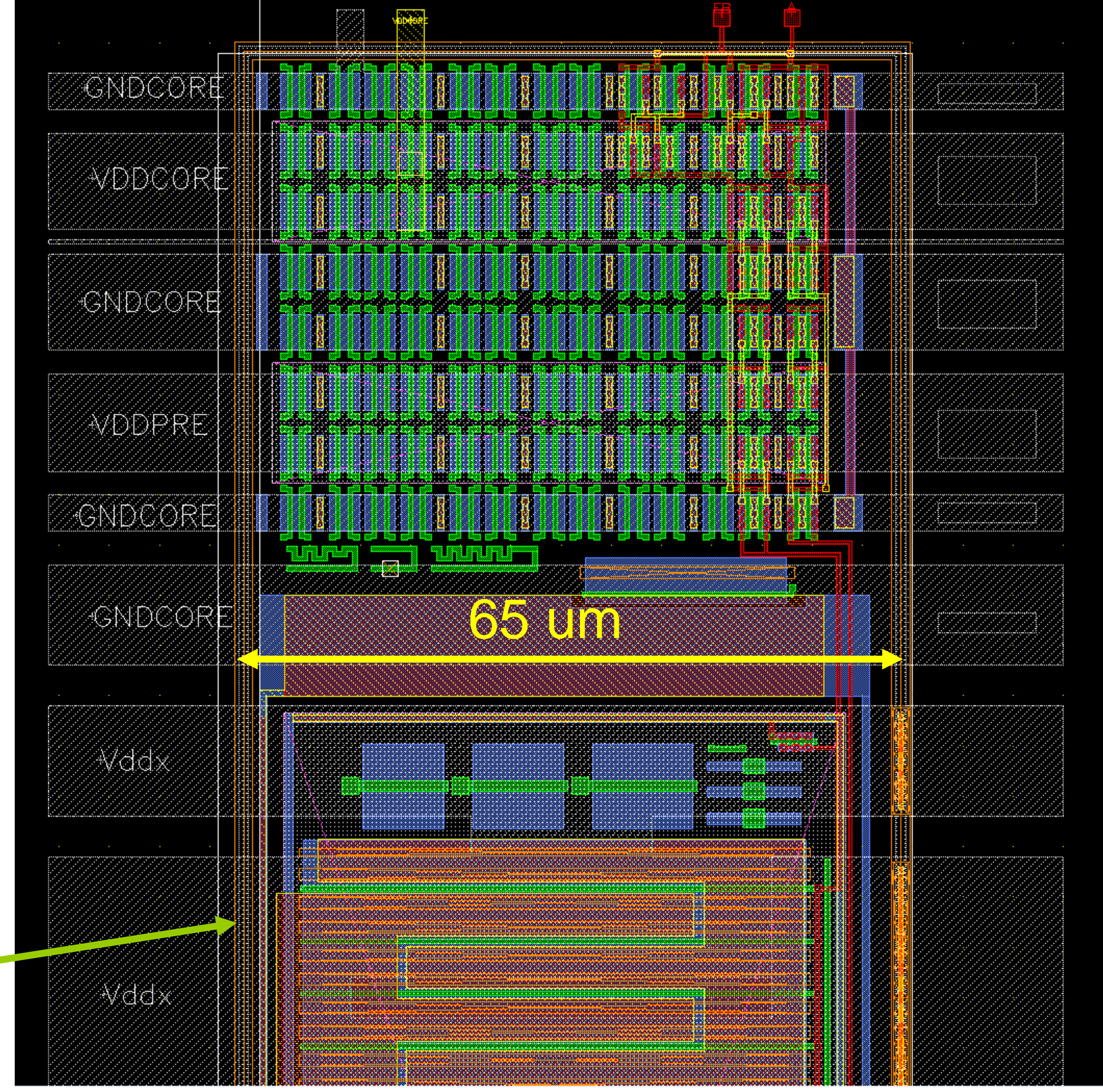




p+ Guard for I/O Buffer

It is hard to re-design I/O buffers, so we just surround the buffer with p+ ring.

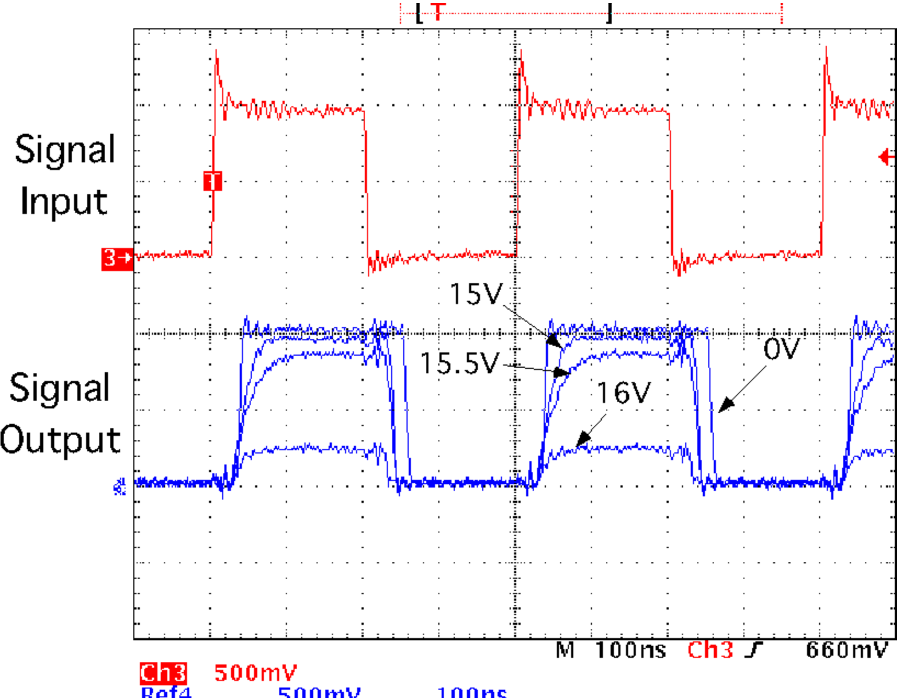
p+ ring

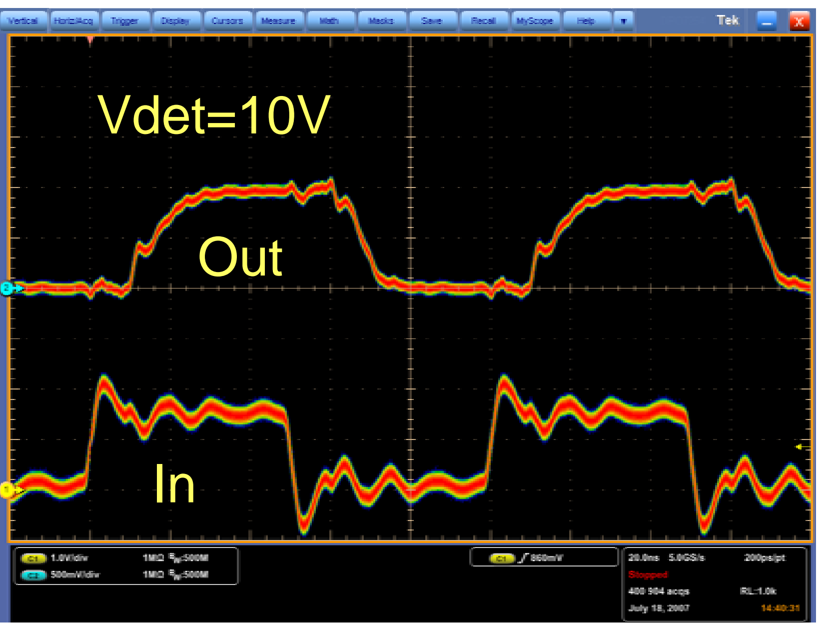


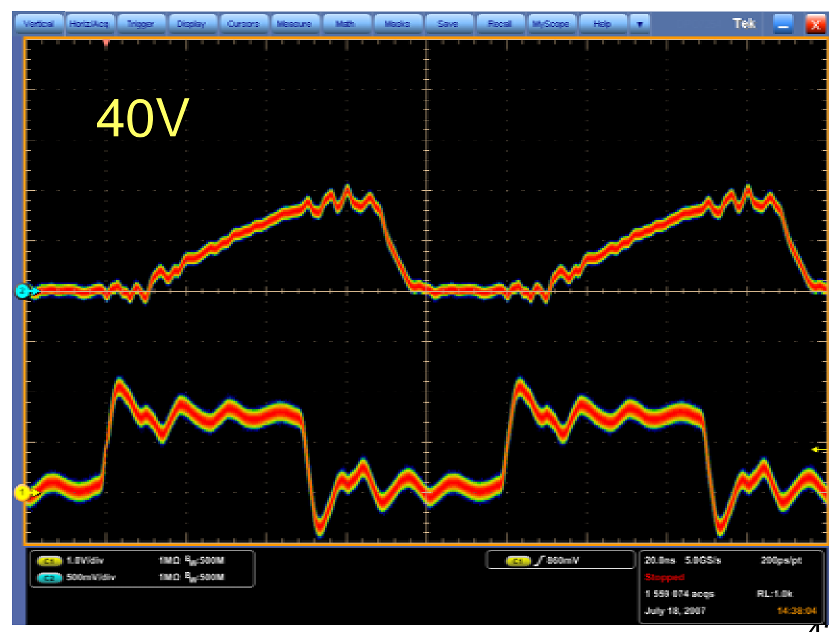
p+ ring = 0V

10MHz Clock

without p+ ring

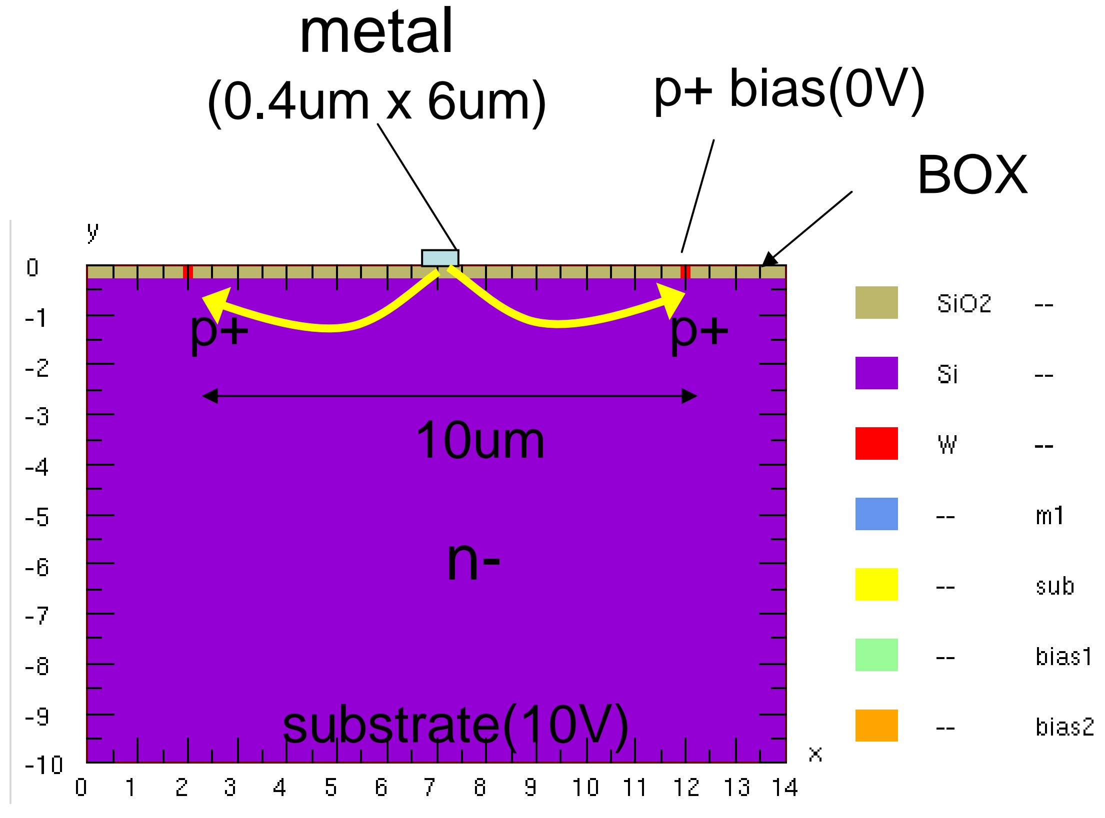




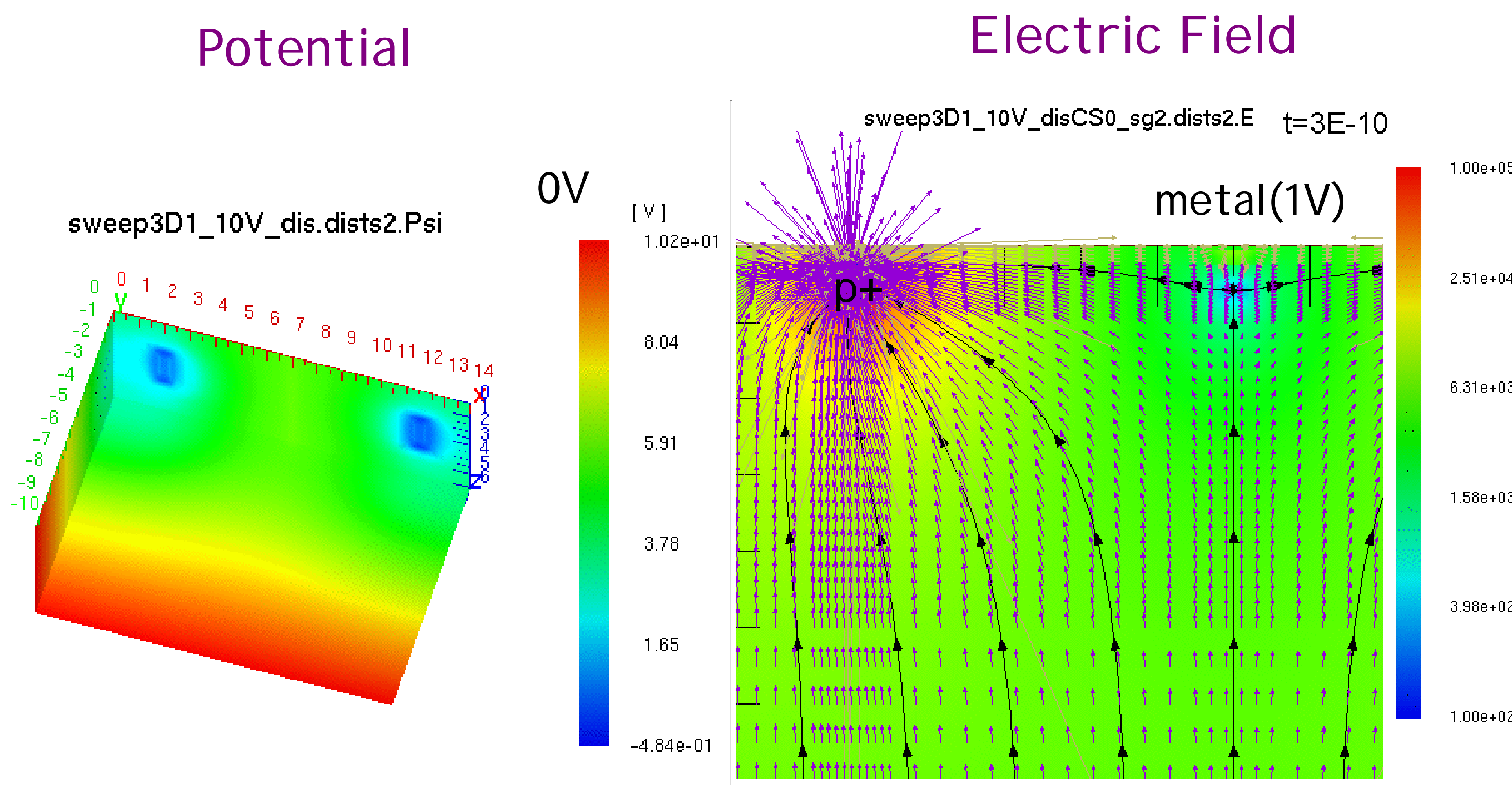


Signal Coupling Simulation

Circuit activity during measurement may affect sensor signal due to coupling through the BOX.

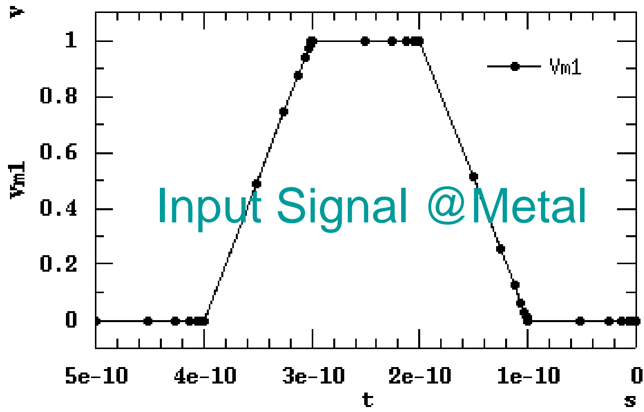


TCAD(Enexss) Simulation

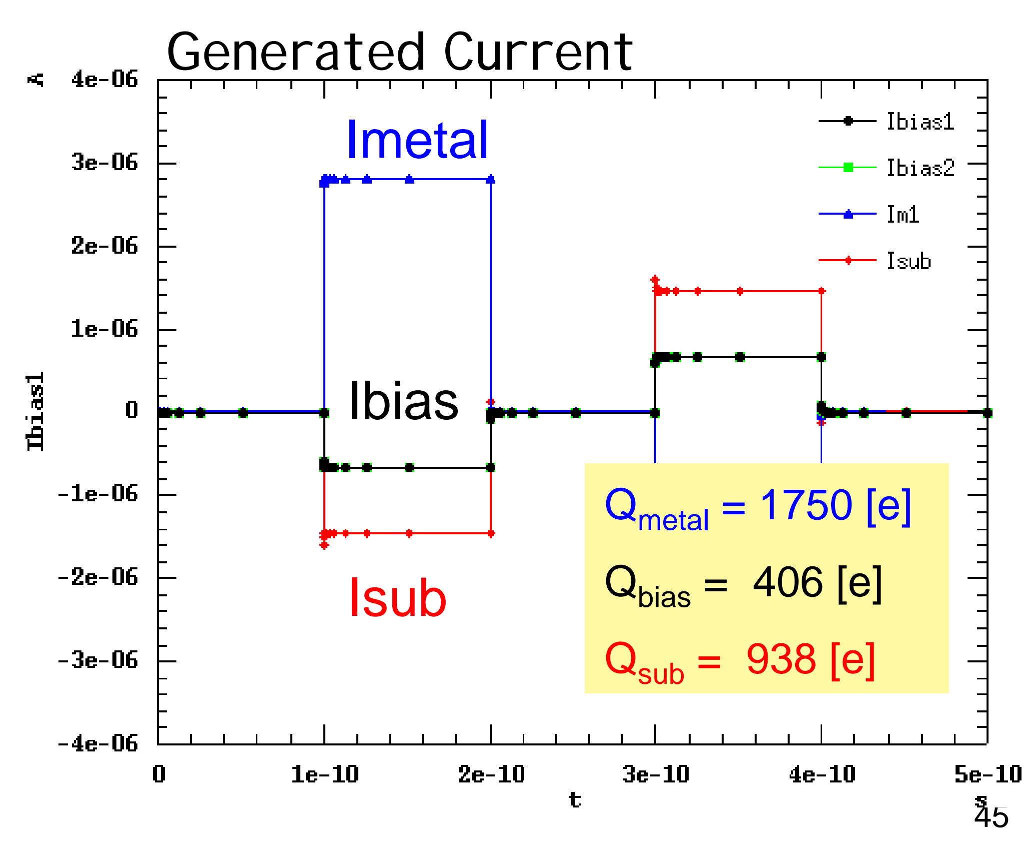


Signal Coupling (cont.)

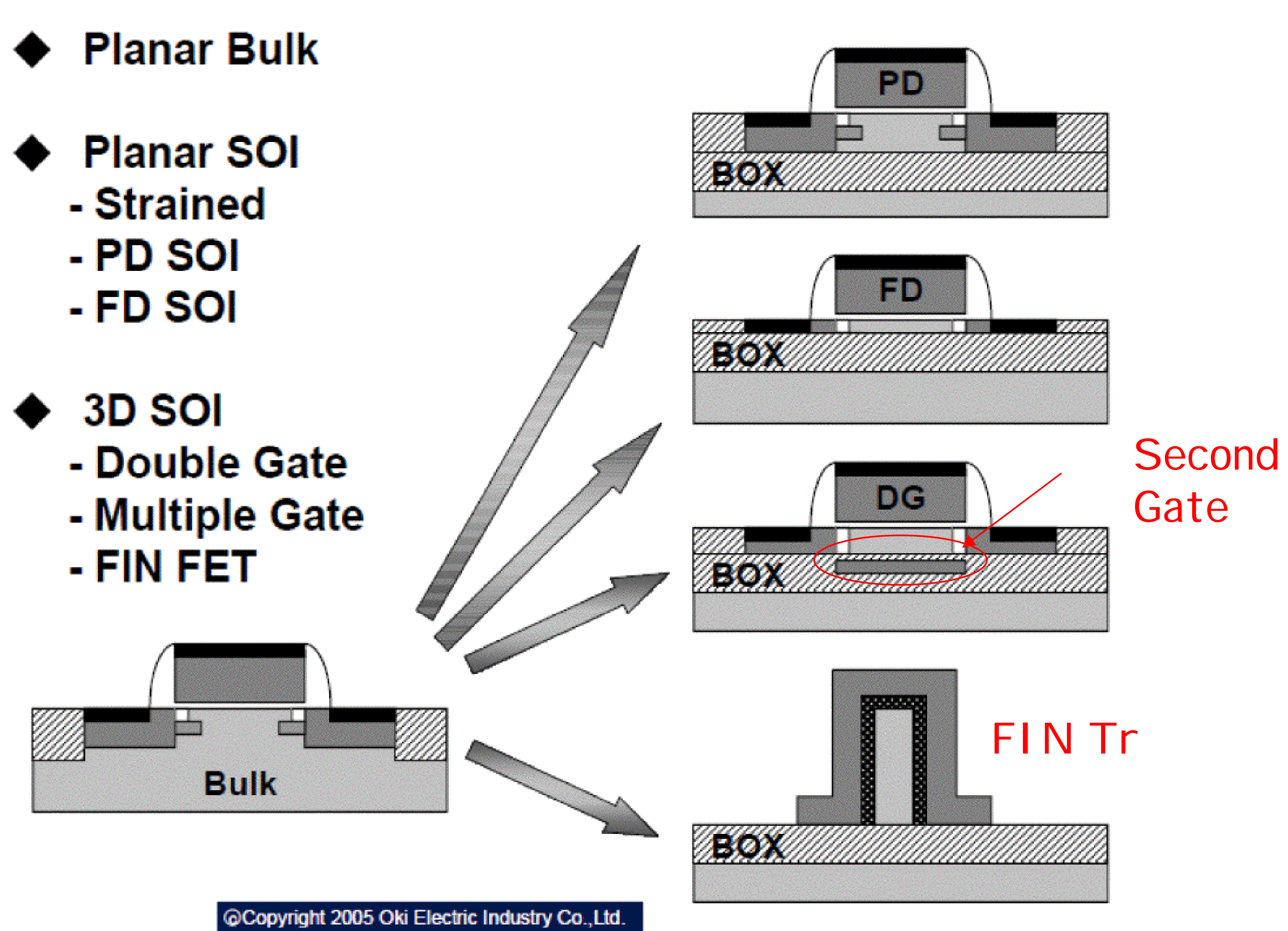
- Pulses in SOI circuit can generate non-negligible amount of charge to the sensor.
- Need further simulations in more realistic geometry.



- No effect in charge integration type sensor.
- Differential signal can reduce the effect.
- Use Double Gate/FIN SOI Tr?
- Use some guard structure?



SOI Device Structure Road Map



Summary of this section

- Processes for implanting p+/n+ to substrate and creating contacts are established with 0.15 μm technology.
- We could demonstrate the first SOI Pixel detects light and β-rays.
- SOI specific issues become apparent.
  - Back gate effect
  - Circuit to Sensor coupling
- TCAD simulation is powerful to study these effects.

OUTLINE

- SOI Device
  - History of SOI
  - Features of FD-SOI
- SOI Pixel Detector
  - Progress of SOI Pixel R&D
  - FY05 MPW Results
  - TCAD Simulations
- **FY06 MPW Run**
  - **Preliminary Results :**
  - **FNAL, LBL, U. of Hawaii, KEK**
- Summary

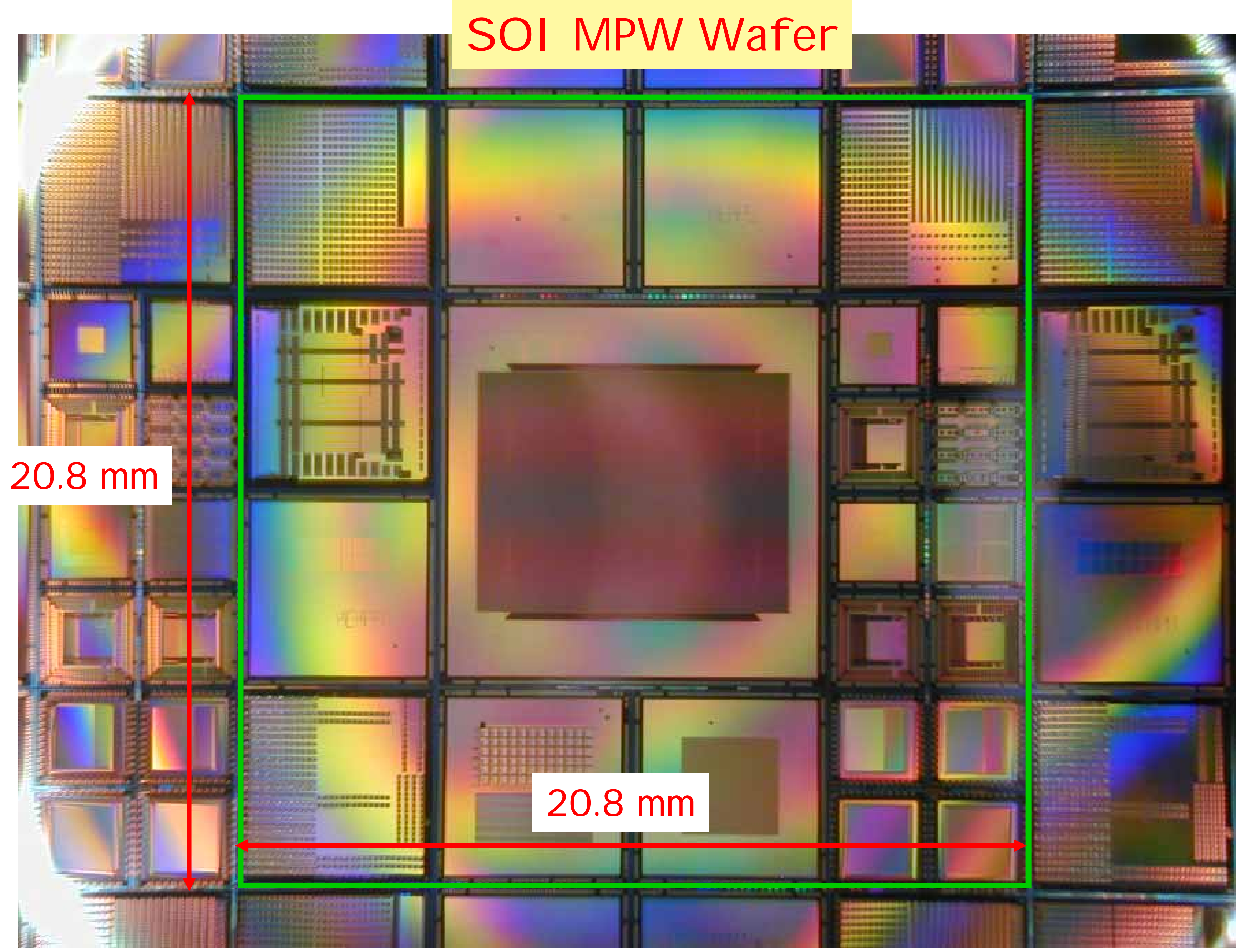
FY06 MPW Run

17 designs were submitted on Dec. 5, 2006

2.4 x 2.4 mm^2 --- 10 chips
5.0 x 5.0 mm^2 --- 6 chips
10.2 x 10.2mm^2 --- 1 chip

Some Preliminary Results are presented. (still under evaluation)

Top Cell Name	Chip size	Affiliation
VARPIXEL	2.4 mm	Osaka Univ.
TOPPIXN	2.4 mm	KEK
OKI0612	2.4 mm	Tokyo Univ.
Achip	2.4 mm	LBL
OKI_TOP	2.4 mm	FNAL(BNL)
ATEG	2.4 mm	JAXA/ISAS
BTEG	2.4 mm	JAXA/ISAS
CTEG	2.4 mm	JAXA/ISAS
isas_set0612	2.4 mm	JAXA/ISAS
RADFET1	2.4 mm	KEK
HawaiiNSUBSTRATE	5.0 mm	U. of Hawaii
detectorPOLY	5.0 mm	KEK
TOP_PIXELSTRIP	5.0 mm	KEK
TOP_8PREAMP	5.0 mm	KEK
TOPTEG2	5.0 mm	KEK
TOPINTPIX	5.0 mm	KEK
TOPCOUNT	10.2 mm	KEK


SOI MPW Wafer
20.8 mm
20.8 mm

FNAL: MAMBO - Monolithic Active pixel Matrix wit Binary cOunters

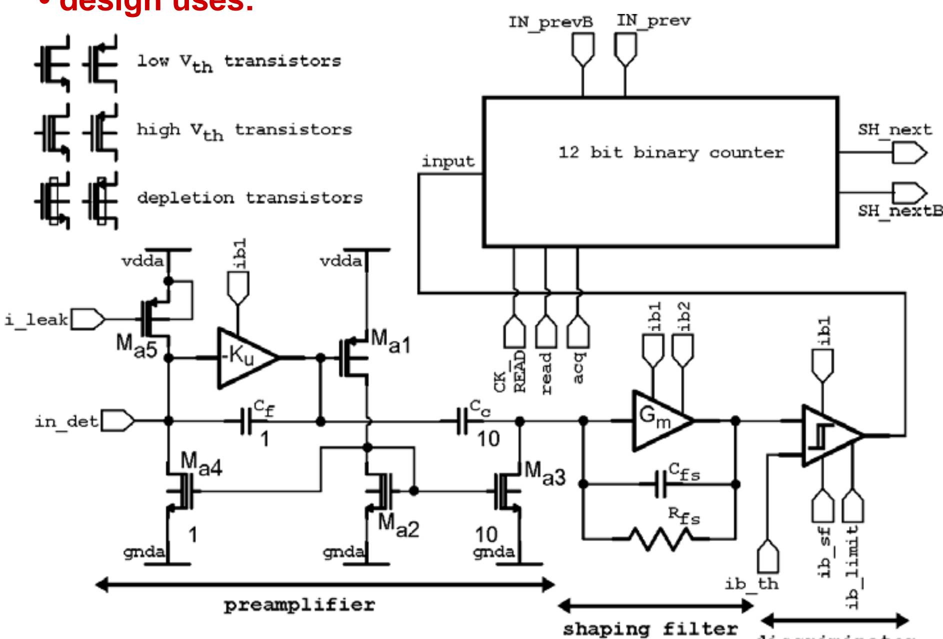
G. Deptuch

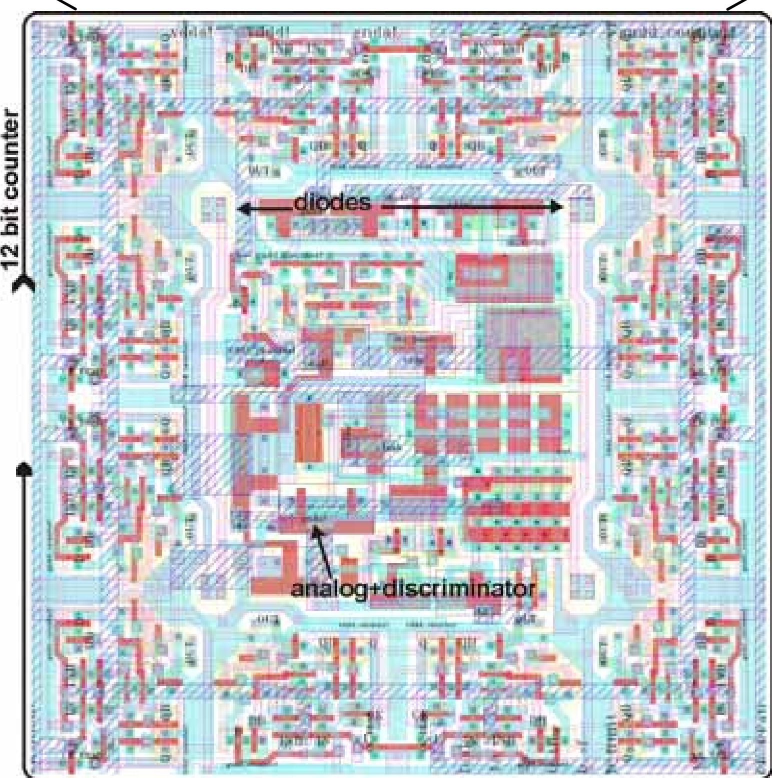
- applications
  - imaging detector for direct detection in electron microscopy (TEM), and soft X-rays,

design:

- test prototype 64x64 pixels, pitch 26μm, 4 parallel diodes /pixel (distance ~13μm),
- each pixel: CSA, CR-RC^2 shaper, discriminator + 12 bit binary counter,
- counter reconfigurable to shift register – readout serial (caterpillar) through all pixels.

- pixel:
  - design uses:





total: 280 transistors

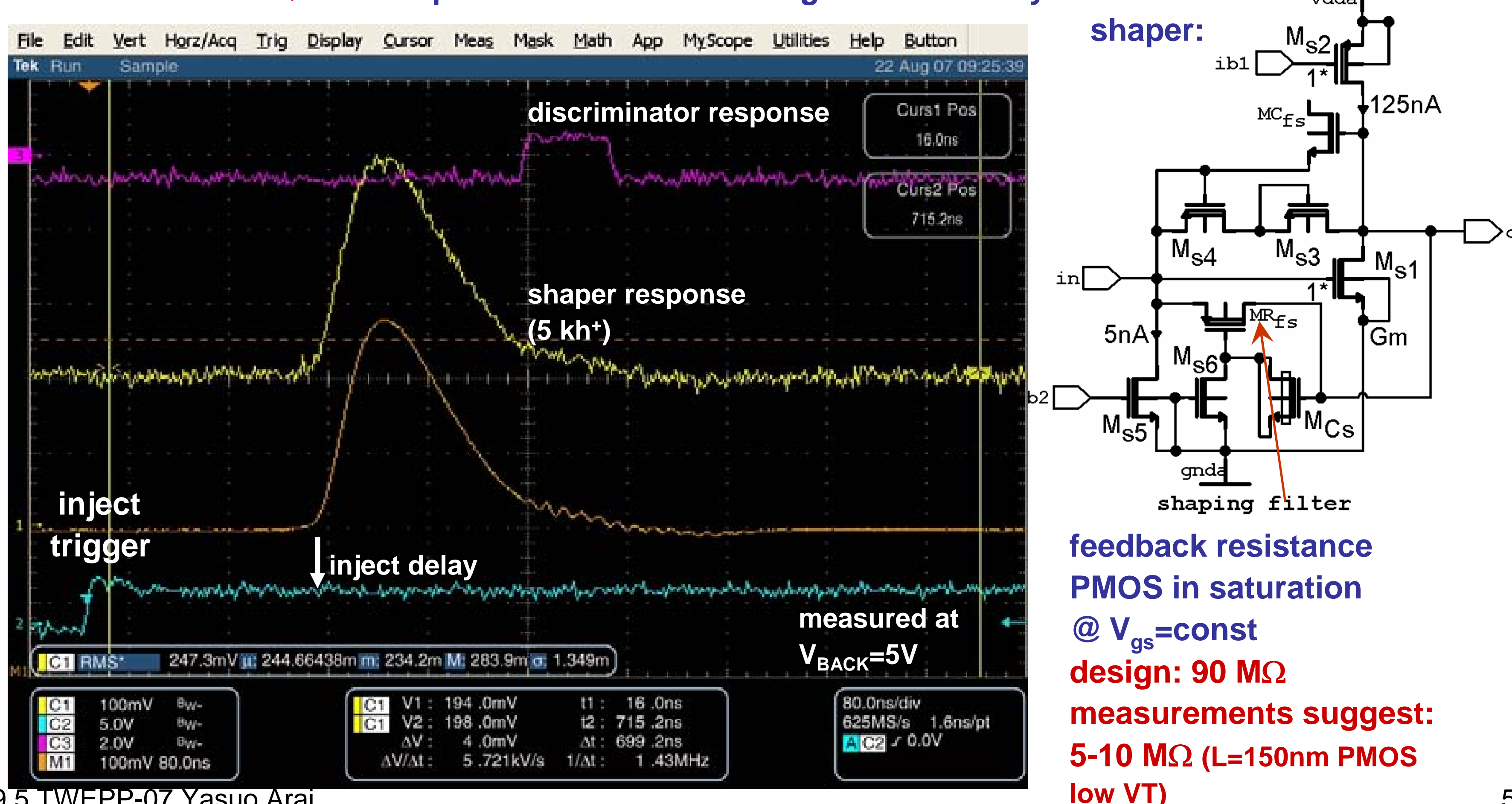
FNAL: MAMBO

G. Deptuch

tests: ⏩ **performed till now: measurements on test structures**

- **analog channel with charge injection by pulse generator OK,** → **Gain significantly lower and shaping much faster – seems to be understood;**
- **counter/shift register OK, (proper operation requires back-gate voltage above certain level ~5V due to conflicting leakage of NMOS and PMOS transistors in OFF state)**
- **discriminator OK,**

acquisition of full scale images is underway!



feedback resistance PMOS in saturation @ V_{gs}=const

design: 90 MΩ

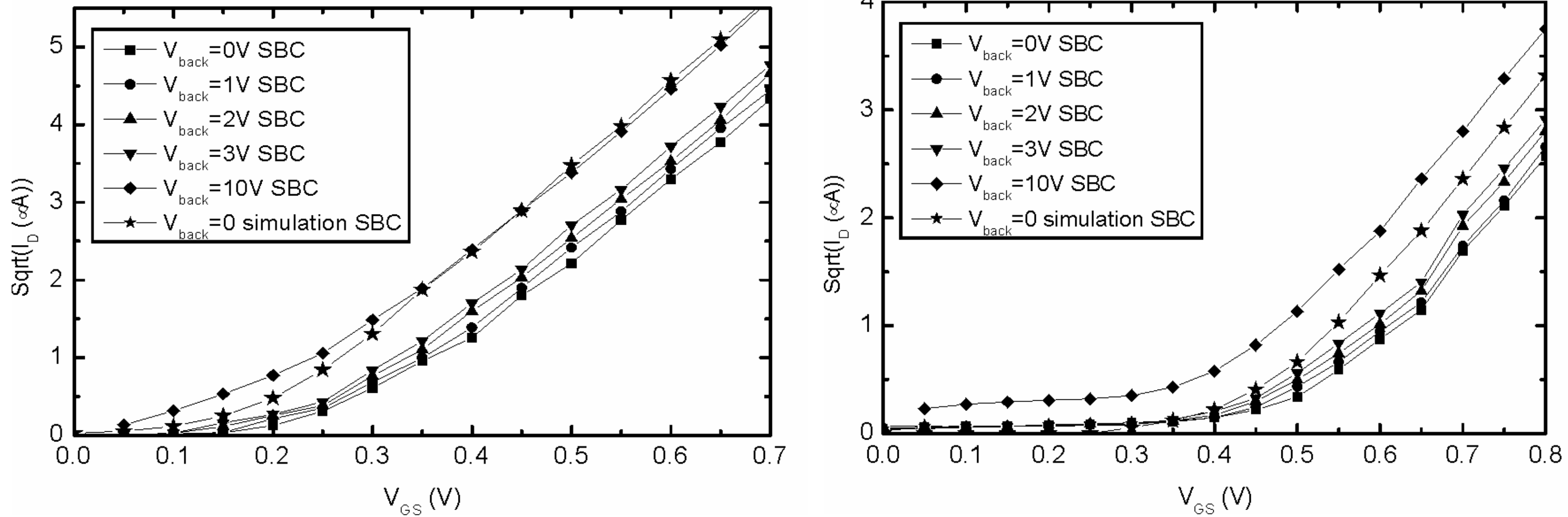
measurements suggest: 5-10 MΩ (L=150nm PMOS low VT)

FNAL: MAMBO

lesson learnt:

G. Deptuch

- **transistors in Silicon on Insulator technology are basically 5 terminal devices;**
  - **there is mutual interaction between transistors and the substrate (used as detector);**
  - **in fully depleted (FD) SOI, substrate plays role of a second gate with gate oxide thickness equal to the thickness of buried oxide (200nm);**
- **measurements of low V_T and high V_T NMOS transistors $I_D(V_{GS})$:**



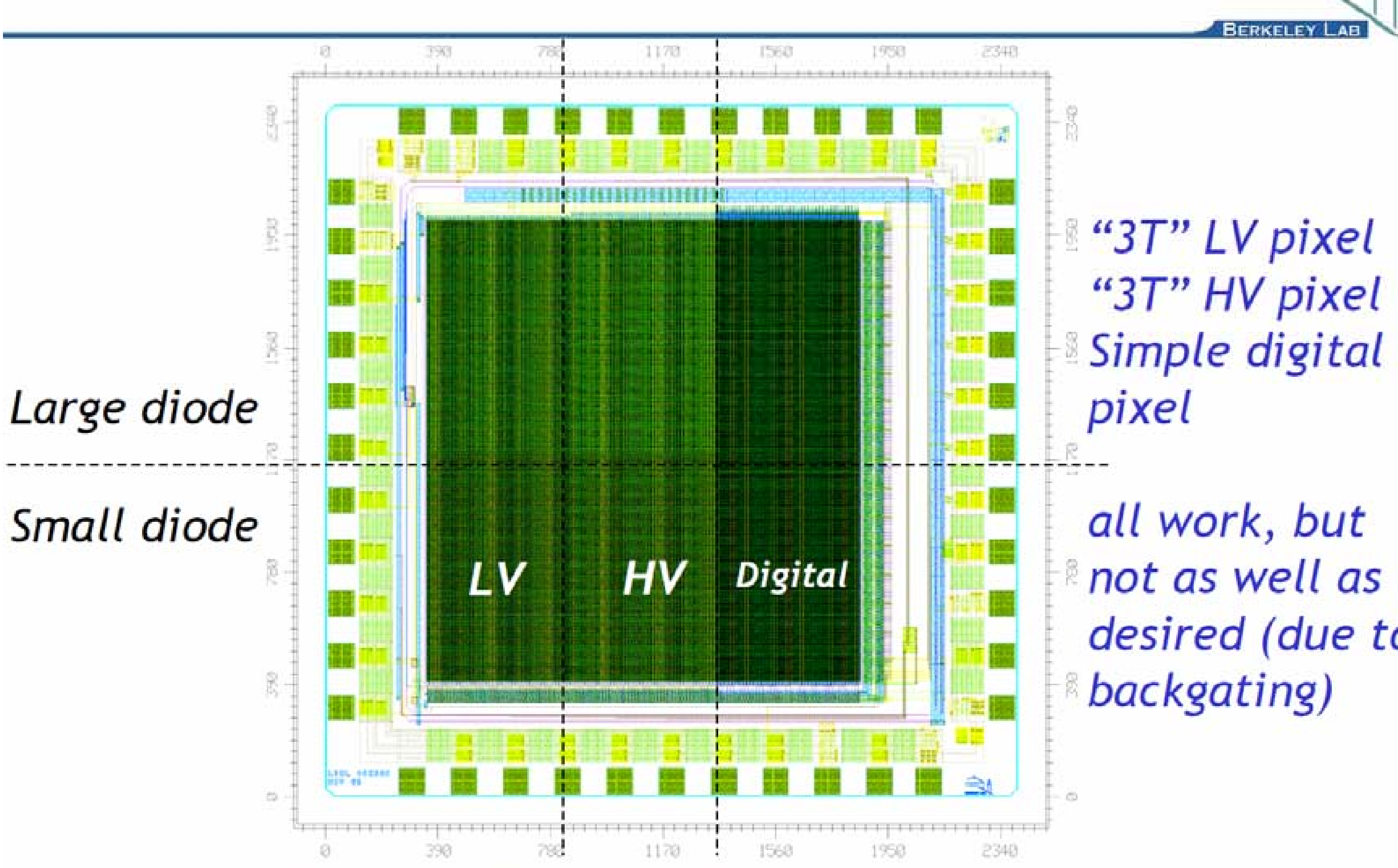
shift in threshold voltage !!! floating body and body tied to source transistors are affected in the same degree

- **hints:**
  - **important is to use dense matrix of p^+ implants to lower potential at the surface;**
  - **use rather low back-gate (generally it is enough V_{BACK}=10V to deplete 50 µm of Si)**
    - **good for electron microscopy, high energy physics, etc.**

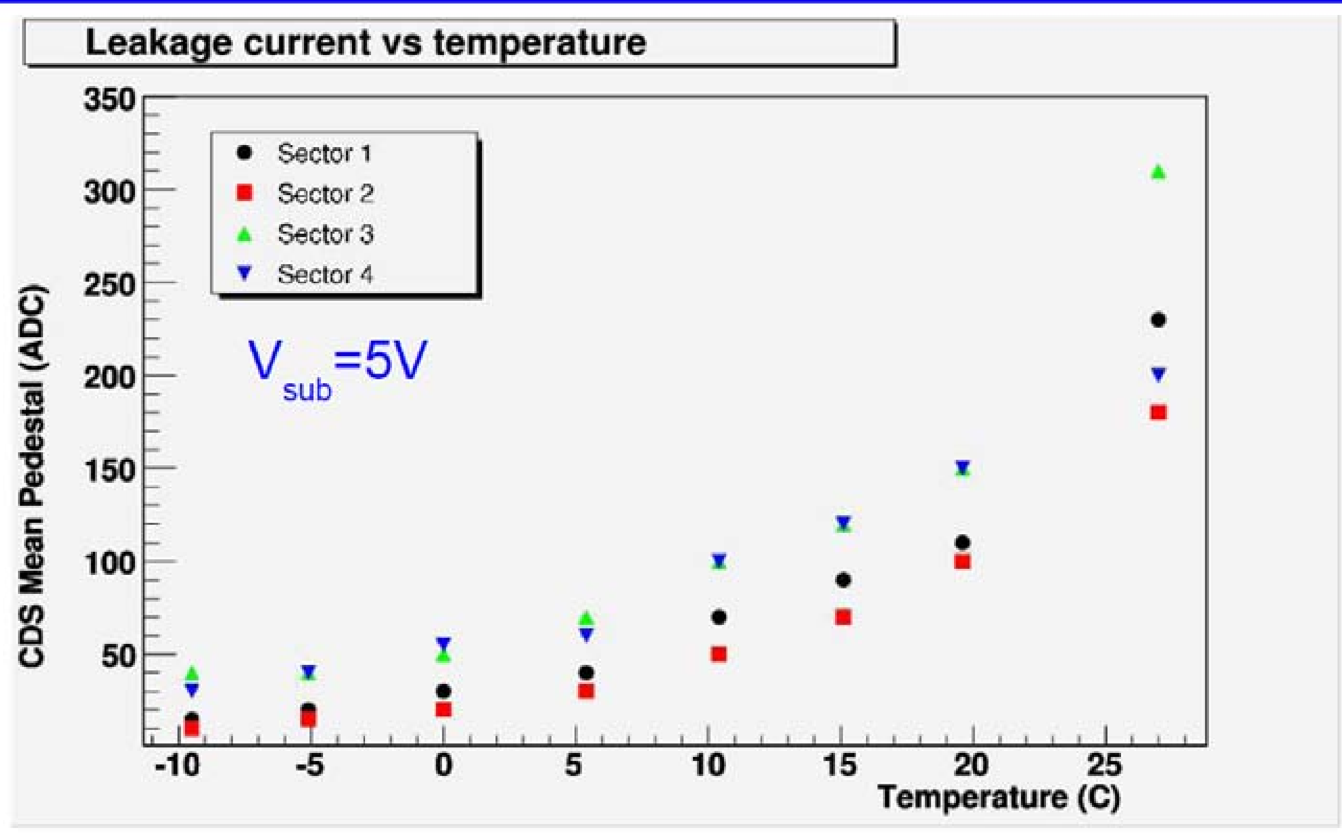
still more to learn

LBNL Pixel

Peter Denes



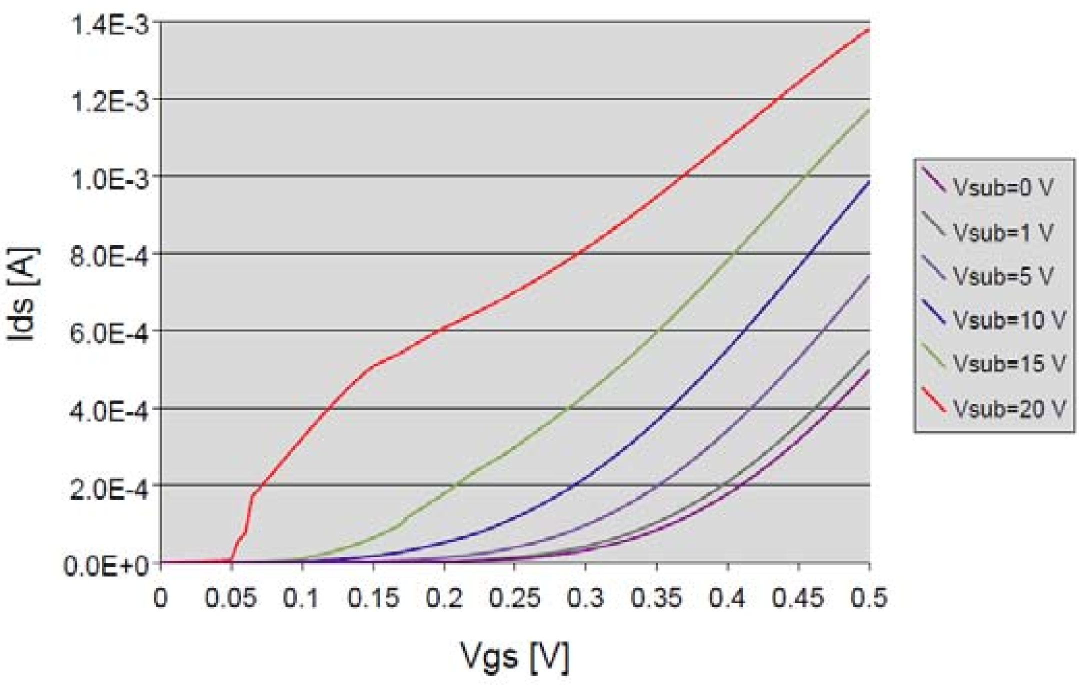
Cooling studies



- 4 analog sectors with 1.0 V and 1.8 V, 1 μm and 5 μm diodes
- Decrease of CDS pedestal level with cooling temperature consistent with leakage current behavior

M. Battaglia, D. Contarato, L. Glesener

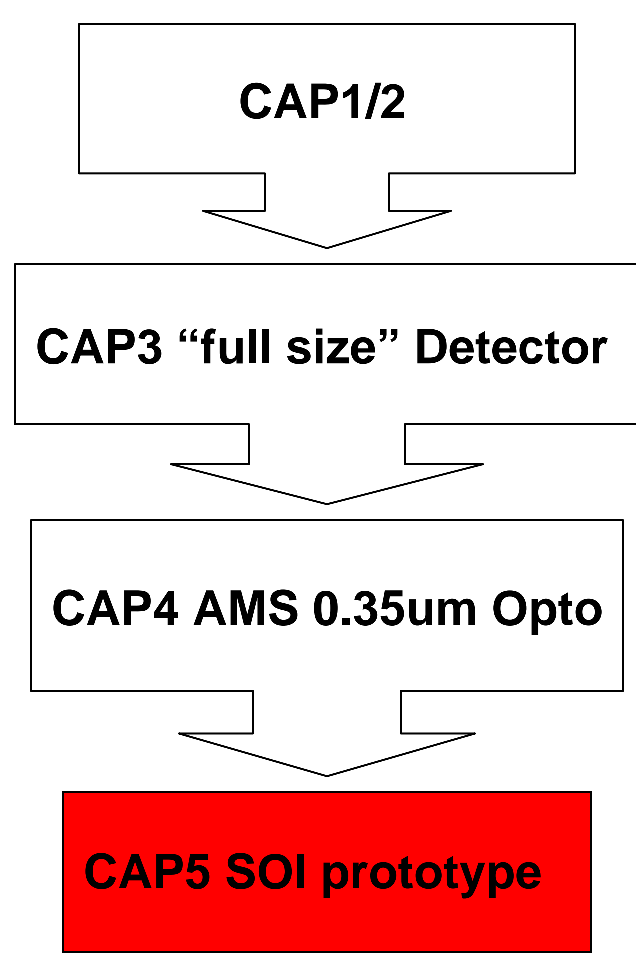
Transistor test: back-gating effect

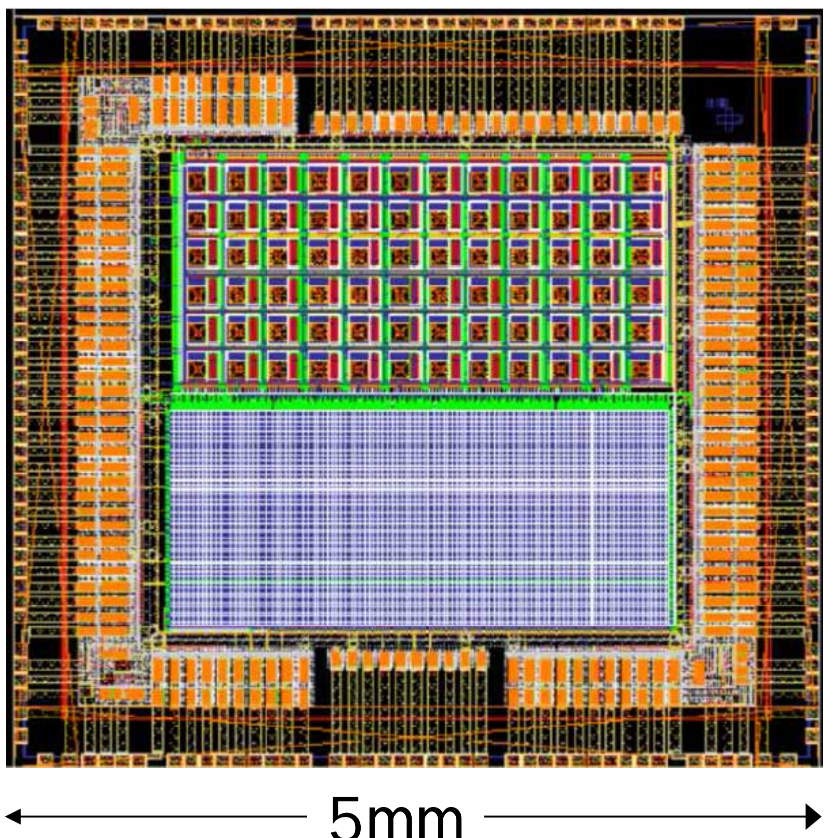


- Single test transistor characteristics measured for different substrate biases
- Threshold shift for increasing substrate bias due to back-gating
- Preliminary results from irradiation with 30 MeV protons up to 2.5e12 p/cm^2: thresholds unchanged w/o substrate bias, but increased effect of back-gating due to charge trapping in buried oxide: characteristics degraded already for V_{sub}=5 V

M. Battaglia, D. Contarato, L. Glesener

Univ. of Hawaii: Continuous Acquisition Pixel (**CAP**) Family





- The area corresponds to 3250 x 1500 μm^2.
- Pixel size occupies 28.7 x 32.5 μm^2.
- The number of columns is 108 and rows is 44.

E. Martin, G. Varner

KEK : I -V characterisitic of the detector

2.5 x 2.5 mm^2 chip

FY05

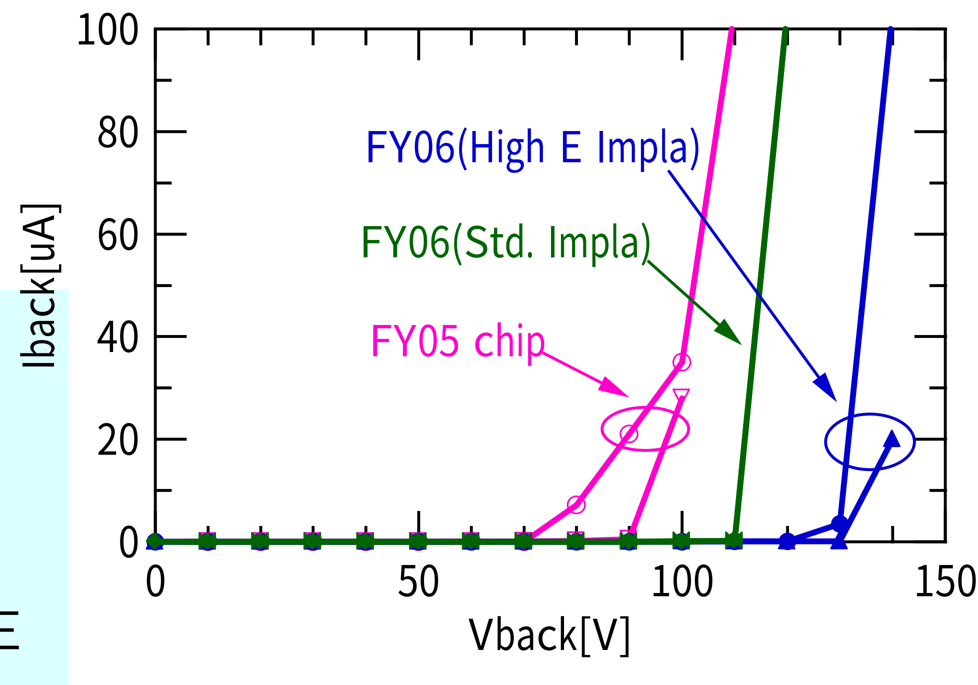
↓ Round the corner of bias ring.

FY06(Std.)

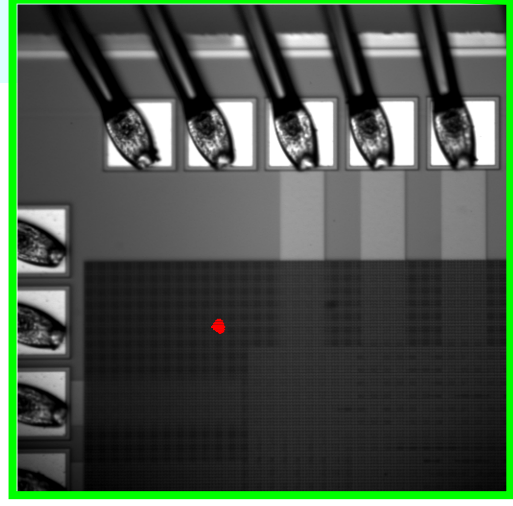
↓ p+/n+ implant with higher E (~x4.7 deep).

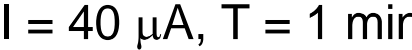
FY06(HE)

become better, and reached to ~130V.

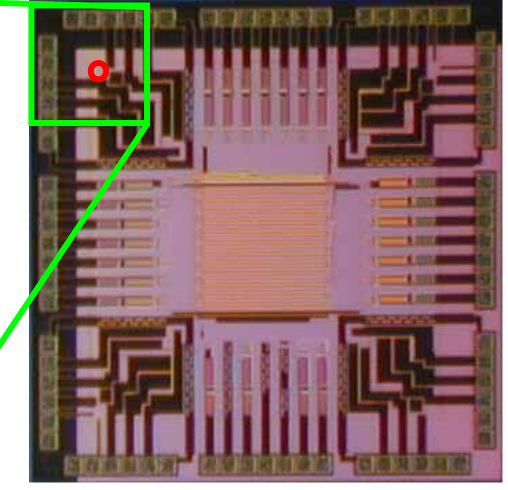


Micro Discharges are observed with infrared camera





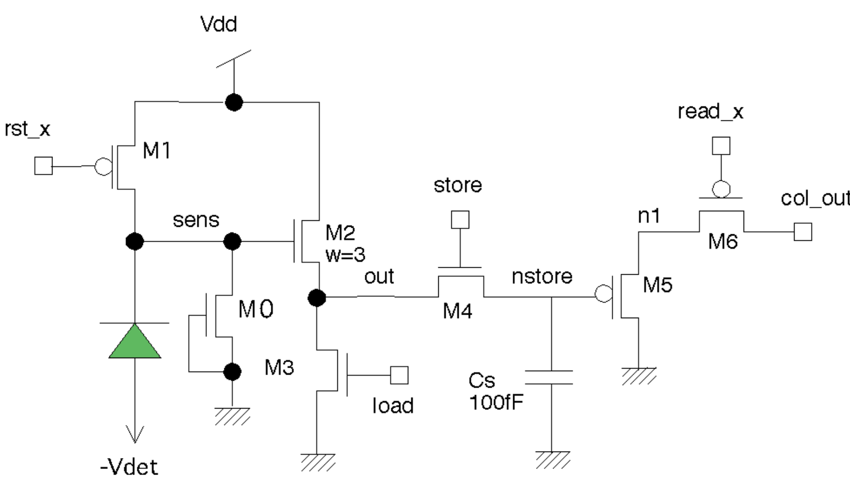
I = 40 μA, T = 1 min

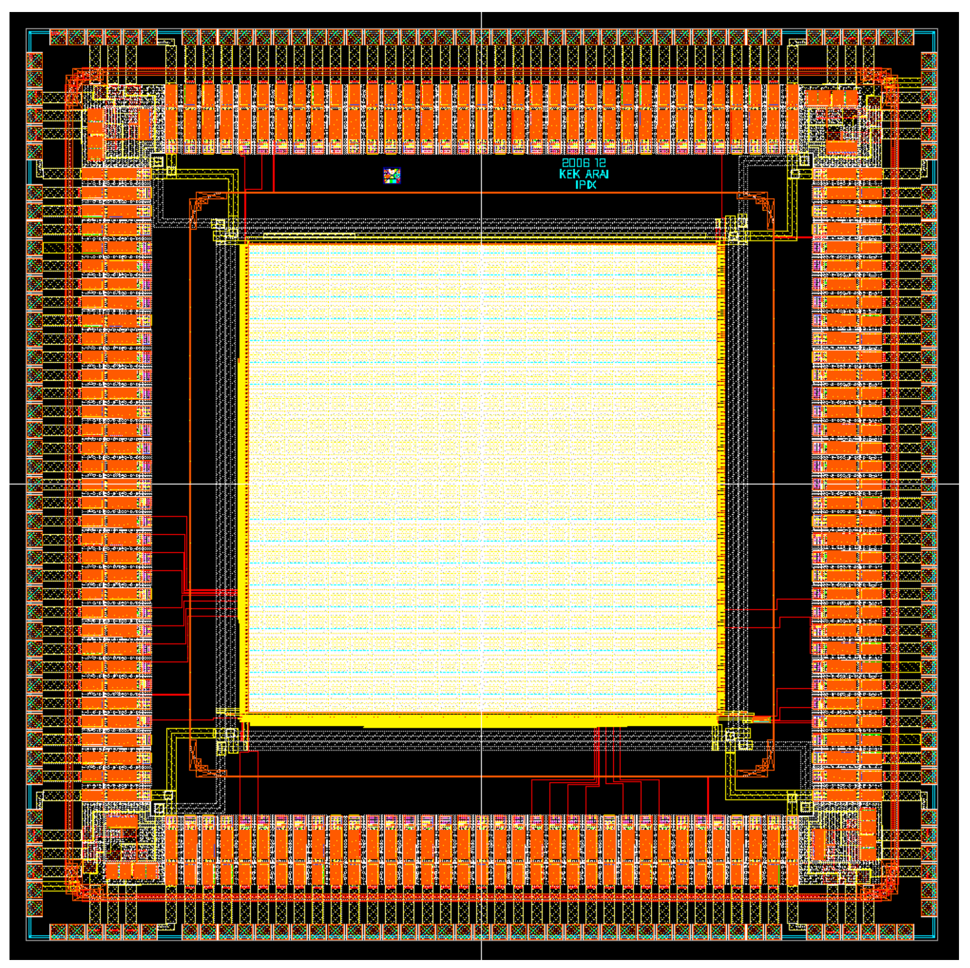


Corner of the bias ring

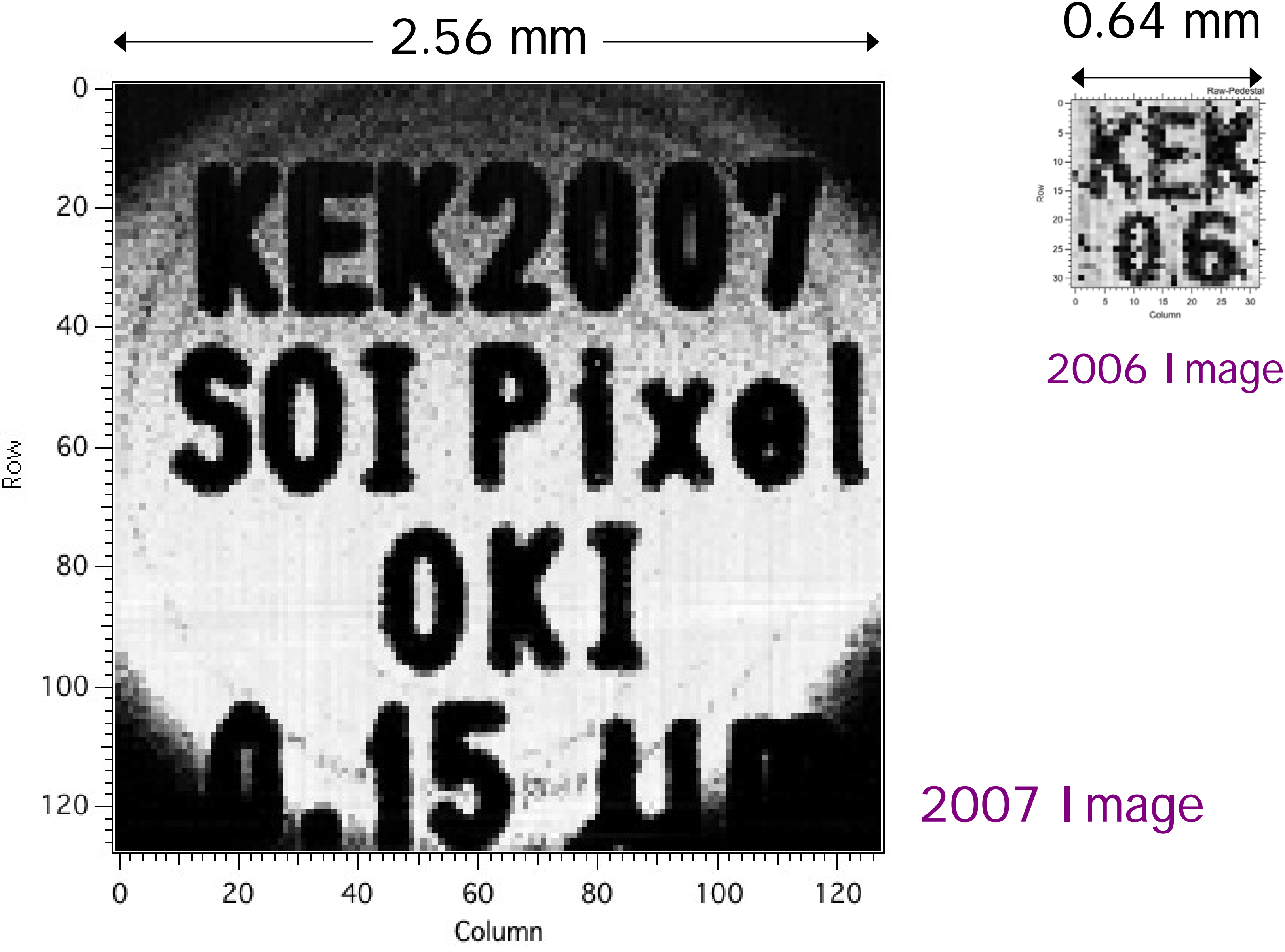
KEK : Integration Type Pixel (INTPIX)

- 20 μm x 20 μm pixel (same as FY05 design)
- 128 x 128 pixels
- 5x 5 mm^2 chip





INTPIX : First Image



2006 Image

2007 Image

FY07 Submission Plan

- Next submission at the end of November (~Dec.).
- Due to OKI process movement, we will use 0.2 μm process at the next run.

	0.15 μm	0.2 μm
Wafer Diameter	6 inches	8 inches
Core (I/O) Voltage	1.0V (1.8V)	1.8V (1.8/3.3V)
Gate Length	0.14 μm	0.2 μm
Gate Oxide Thickness	2.5/5 nm	4.5/7 nm
BOX Thickness	200 nm	200 nm
Ioff	<100pA/μm	<0.1pA/μm

Space is still available !

Summary

- SOI device has many interesting features to use in HEP and Space applications.
- We confirmed the basic operation of SOI pixel detector with OKI 0.15 μm FD-SOI technology.
- At the Second MPW run(FY06), we submited our own MPW run with 17 designs including US and Japan Univ./Labs.
- We are planning the Third MPW run in Nov.-Dec. with 0.2 μm technology
- We welcome more people to join to use this interesting technology.