Electronics and Sensor Study with the OKI SOI process

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Abstract

While the SOI (Silicon-On-Insulator) device concept is very old, commercialization of the technology is relatively new and growing rapidly in high-speed processor and low-power applications. Furthermore, features such as latch-up immunity, radiation hardness and high-temperature operation are very attractive in high energy and space applications.

Once high-quality bonded SOI wafers became available in the late 90s, it opened up the possibility to get two different kinds of Si on a single wafer. This makes it possible to realize an ideal pixel detector; pairing a fully-depleted radiation sensor with CMOS circuitry in an industrial technology.

In 2005 we started Si pixel R&D with OKI Electric Ind. Co., Ltd. which is the first market supplier of Fully-Depleted SOI products. We have developed processes for p+/n+ implants to the substrate and for making connections between the implants and circuits in the OKI 0.15μm FD-SOI CMOS process.

We have preformed two Multi Project Wafer (MPW) runs using this SOI process. We hosted the second MPW run and invited foreign universities and laboratories to join this MPW run in addition to Japanese universities and laboratories.

Features of these SOI devices and experiences with SOI pixel development are presented.

I. INTRODUCTION

A. History of SOI

Since planar processing technology was developed by R. Noyce in 1959 [2], most of ICs have been built on a bulk Si wafer. However, the first transistor, patented in 1928 [3] by J. E. Lilienfeld, was built on a thin semiconductor film (unfortunately, the technology was not mature at that time and there is no evidence that this device ever worked). This transistor has a structure very similar to that of a SOI device.

In a SOI chip, transistors are built on a very thin Si film surrounded by insulators, so it has an ideal structure for integrated circuits. However, mass production of SOI chips had to wait until 1998 when IBM announced that they would use SOI technology to make the Power PC MPU.

The first SOI wafer that could be used for integrated circuits was developed by K. Izumi [4] in 1978. This method is called SIMOX (Separation by Implanted Oxygen). In SIMOX, oxygen ions of 120-200 keV energy are implanted into a Si wafer with a fluence of 4-20x10^{17} cm^{-2}. The wafer is then annealed at ~1300 ºC for 3-6 hours to create a SiO_2 layer under a thin Si layer. Although SIMOX can provide high quality SOI wafers, the wafer cost is relatively high due to the necessity of large oxygen implantation doses.

Meanwhile, a clever method called Smart-Cut was developed by M. Bruel [5]. A SOI wafer fabricated using the Smart-Cut method is called a UNIBOND wafer [6], the process of which is shown in Figure 1. This process starts with two different wafers. The first wafer is implanted with H+ ions and bonded to the second wafer. The first wafer is then cleaved and a thin Si layer is transferred to the second wafer.

Normally SOI devices use only the thin upper Si layer (SOI layer) for circuit implementation, and the bottom wafer (handle wafer, substrate) works just as a mechanical structure. Since the UNIBOND wafer starts with two different Si wafers, it is easy to bond low-resistivity Si wafer to a high-resistivity Si wafer. Low-resistive Si is necessary for CMOS circuit implementation, while a high-resistivity Si substrate can be used as a radiation sensor.

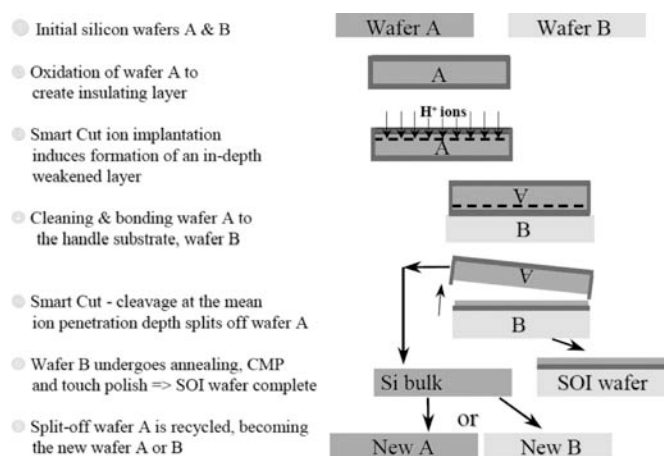

Figure 1: Flow diagram of the UNIBOND process [6].

B. Bulk CMOS vs. SOI CMOS

Figure 2 shows cross sections of bulk CMOS and SOI CMOS transistors. In a bulk CMOS device, each transistor is isolated by reverse-biased p-n junctions in a well structure. On the other hand, in a SOI CMOS device, each transistor is completely isolated by the Oxide insulator. Thus, parasitic effects in a SOI device are very small.

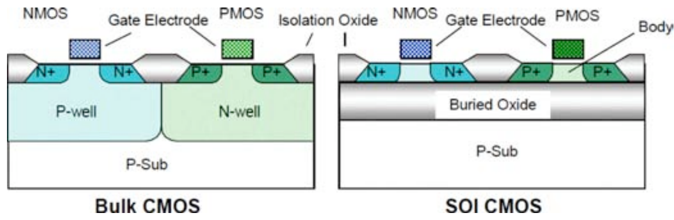

Figure 2: Cross sections of bulk CMOS and SOI CMOS transistors.

C. *PD-SOI and FD-SOI*

There are two kinds of SOI devices; Partially Depleted (PD)-SOI and Fully Depleted (FD)-SOI (Figure 3). The PD-SOI has a relatively thick SOI Si thickness (100-200 nm), while in the FD-SOI the SOI thickness is less than 50 nm.

In PD-SOI, there remains a neutral region in the body. This causes large floating body effects such as 'history' and 'kink' effects [7]. The 'history effect' makes it difficult to simulate circuits. The 'kink effect' increases the drivability of a transistor, so it is useful for high-speed digital circuits, but not good for analog circuits.

In FD-SOI, the whole body under the gate will deplete, thus floating body effects are reduced. In addition, the whole gate voltage is used efficiently to deplete the body region, so sub-threshold slopes are steep (Figure 4). This makes it possible to lower the threshold voltage and is good in low voltage (power) applications.

Today, many PD-SOI devices are available; IBM PowerPC, AMD Athelon, Sony Cell processor and so on. However, mass production of the FD-SOI is currently only performed by OKI, mainly for radio-controlled solar watches.

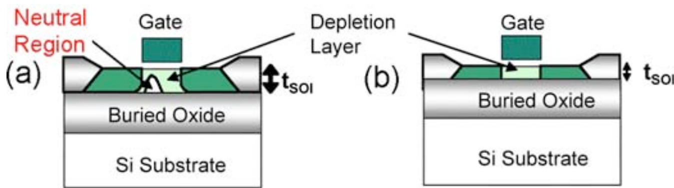

Figure 3 : Transistor structure of (a) PD-FOI and (b) FD-SOI.

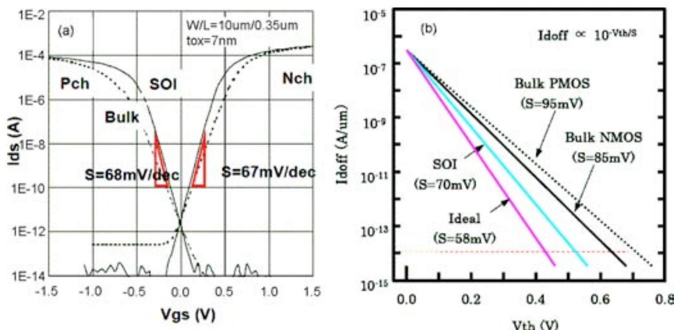

Figure 4: (a) Sub-threshold slope of FD-SOI transistors and bulk CMOS transistors. (b) Comparison of leak current (Idoff) vs. Vth [8] in different technologies.

II. FEATURES OF FD-SOI

There are many fascinating features of a FD-SOI device. In general, a SOI device has 20-30% better performance than a bulk device for the same photolithography, due to its smaller junction capacitance. Below are described some of the features relevant to high energy and space experiments [9].

A. *Latch-up free*

It is well known that there is a parasitic PNPN structure in bulk CMOS devices and this may cause latch-up of the device. As seen in Figure 5, there is no such parasitic structure in a SOI device.

Although there is a parasitic bipolar effect [10] in PD-SOI, which might reduce drain breakdown voltage, the effect is very small in FD-SOI.

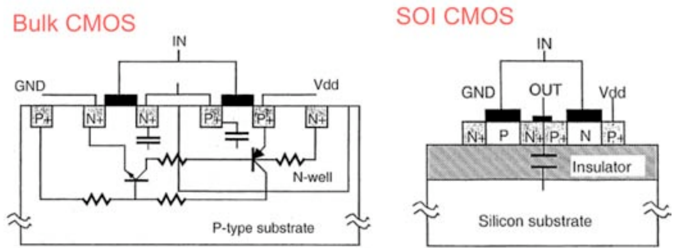

Figure 5: Parasitic PNPN structure in bulk CMOS and SOI CMOS structure [7].

B. *Area reduction*

Since there is no well isolation in a SOI device, as seen in Figure 5, a more compact layout is possible in a SOI IC. PMOS and NMOS can be located side-by-side if necessary. In a SRAM cell layout, for example, more than 30% reduction of area is reported when the same feature size technology is used.

C. *Circuit isolation*

In a SOI device, each transistor is isolated by Oxides (Field Oxide and BOX), thus higher isolation is observed in SOI compared with bulk technology (Figure 6). When a high-resistivity substrate is used, 10-40dB better isolation is reported, up to 10 GHz [11].

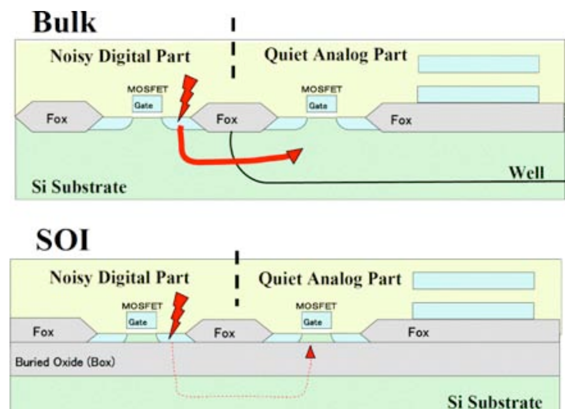

Figure 6: Noise travelling path in bulk and SOI devices.

D. High-Temperature operation

As stated before, a SOI device is immune to latch-up phenomena. The small junction area of FD-SOI devices reduces the high-temperature leakage currents by as much as 3 to 4 orders of magnitude compared to bulk CMOS devices. Threshold voltage variation with temperature is 2 to 3 times smaller than in bulk devices. These properties enable the fabrication of digital and analog SOI circuits operating up to and over 300°C with little performance degradation [12].

E. Single Event

Since the active Si thickness of the SOI transistor is very thin, the number of generated charges in the active area is very small, compared with bulk transistors (Figure 7). Thus higher immunity to single event effects (SEEs) is expected in a SOI device. Thus many SOI devices have been used in satellite instruments.

Although the SEE cross-section is already small in SOI devices, excellent SEE immunity is available by combining with the hardness-by-design (HBD) techniques [13].

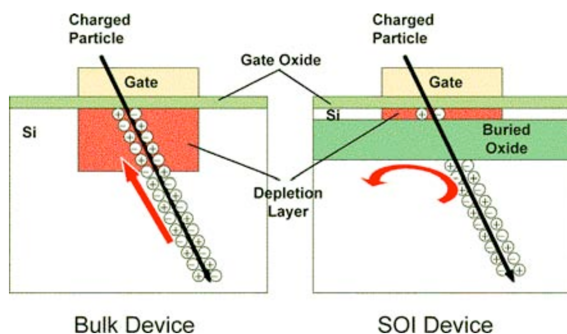

Figure 7: Charge distribution in bulk and SOI devices generated by the passage of a charged particle.

F. Total Ionizing Dose

Since the SOI transistor has many Si-SiO_2 interfaces (gate oxide, BOX, Field oxide), it is somewhat sensitive to Total Ionizing Dose (TID). Nevertheless, thanks to the fine device structure, transistors in the OKI 0.15 μm process show radiation tolerance up to a few hundred kRad (Si) [14]. This is usually enough for space applications. At much higher doses, holes are mainly trapped at the Si-BOX interface, and threshold voltage shift develops due to the back gate bias. The back gate effect is discussed in section IV. It can be partly compensated by biasing the substrate [15].

III. SOI PIXEL DETECTOR

Many attempts have been made to integrate pixel sensors and readout electronics into a monolithic device [16]. Highly-resistive Si must be used to make a thick depletion layer, which is necessary to get high-speed signal collection and to achieve high radiation detection efficiency. On the other hand, a LSI circuit needs low-resistivity Si to control appropriate transistor parameters.

The UNIBOND SOI wafer is a key component to realize such monolithic pixel detector. Pioneering work for a SOI pixel detector has been done by the SUCIMA collaboration [17]. Unfortunately the technology used there was rather obsolete (CMOS 3 μm technology), and suffered from many technical problems.

We have started SOI pixel detector R&D in collaboration with OKI Electric Industry Co. Ltd., in summer 2005 [18, 19, 20]. OKI is renown as the world's first supplier of FD-SOI products. The basis technology for fabricating the pixel detector is OKI's fully-depleted 0.15μm CMOS SOI process. Additional processing steps to create substrate implants and contact formation were developed by this collaboration.

Figure 8 illustrates a representative cross-section of the pixel detector. Several implant position arrangements are being tried. Two submissions to the OKI process were done and these processes were completed in spring 2006 (FY05 run) and 2007 (FY06 run). Especially in the FY06 run, we called for chip designs outside of our collaboration. Figure 9 shows a photograph of the FY06 MPW wafer. Mask size of the process is 20.8 mm and we shared the mask among 17 user designs.

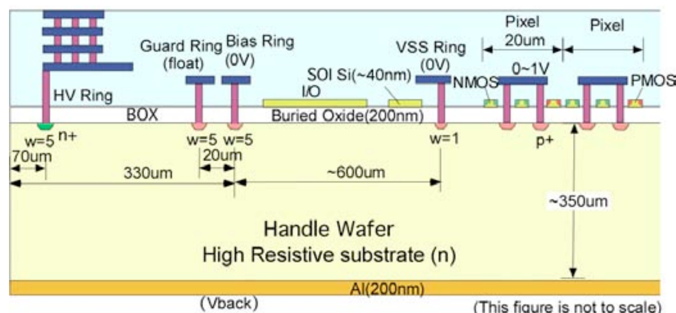

Figure 8: Representative cross-sectional view of the SOI pixel detector.

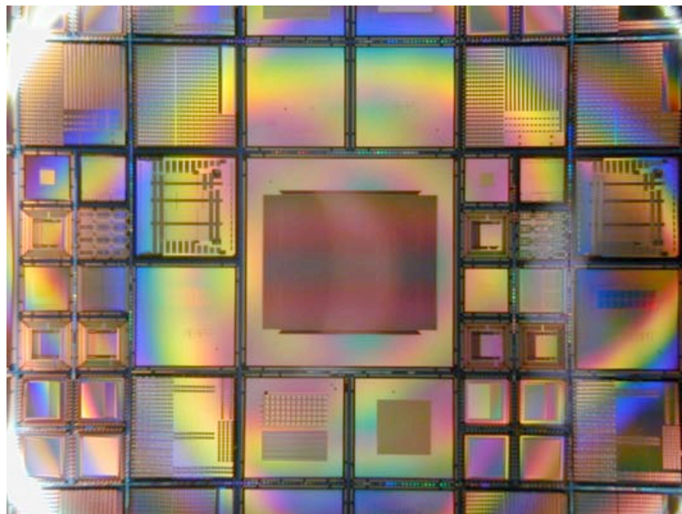

Figure 9: Photograph of the FY06 run MPW wafer. Wafer size is 6 inch in diameter, and the mask size is 20.8mm x 20.8 mm. The wafer includes submissions from Osaka Univ., Tokyo Univ., U. of Hawaii, JAXA/ISAS, Fermilab, LBNL, and KEK.

Table 1: Features of the OKI SOI CMOS process

Process	0.15μm Fully-Depleted SOI CMOS process, 1 Poly, 5 Metal layers.
SOI wafer	Diameter: 150 mm φ (SOITEC) Top Si : Cz, ~18 Ω-cm, p-type, ~40 nm thick Buried Oxide: 200 nm thick Handle wafer: Cz、 700 Ω-cm, 650 μm thick
Backside	Thinned to 350 μm and plated with Al (200 nm).
Supply Voltage	Core 1V, I/O 1~1.8V
Transistors	High Voltage Tr (I/O), High Threshold Tr, Low Threshold Tr. Floating body and body tight

A. *SOI Process*

Characteristics of our SOI process are summarized in Table 1. We used a SOI wafer of low resistivity p-type Si on top, and a high resistivity (700 Ω•cm) n-type substrate on the bottom.

The process flow of the SOI pixel is depicted in Figure 10. Implantation of p+/n+ to the substrate is performed after cutting the SOI and BOX layer. In the FY05 run, the implant was done under the same conditions as the transistor drain/source region, so the depth of the implant was only ~0.1 μm. In FY06 run we tried deeper implants by changing the implant energy and using lighter implant particles, targeting a ~4.7 deeper implant profile. After forming contacts between the p+/n+ implants and the 1st metal layer, normal SOI CMOS processing is performed.

After wafer processing, the wafer backside is ground mechanically from 650 μm to ~350 μm, then plated with 200nm of aluminium. Detector voltage can be applied both from bottom and top pads, which are connected to a high voltage (HV) n+ implant ring.

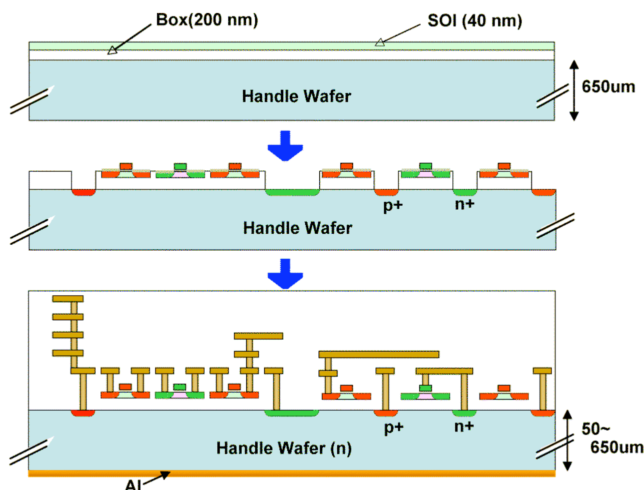

Figure 10: Simplified SOI pixel process flow.

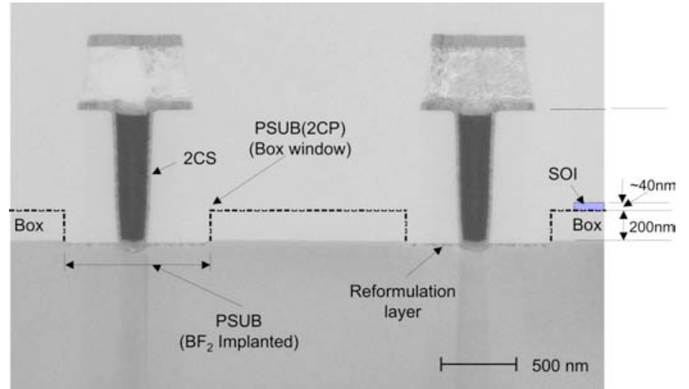

Figure 11: TEM photograph of the p+ implant and contact cross section.

Figure 11 shows a TEM photograph of the cross section of the p+ implant to the substrate and contact to the 1st metal layer. Sheet resistance of the p+ (n+) implant is measured to be 136 (33) Ω/square, and the resistance of the 0.16 x 0.16 μm^2 contact to the p+ (n+) implant is 218 (87) Ω. These values agreed with expectation.

B. *Pixel TEG*

We have developed simple pixel detectors with a pixel size of 20 μm by 20 μm. The pixel circuit is a standard active pixel type with a storage capacitor, illustrated in Figure 12. At the periphery of the chip there exist row and column selects, control logic, and reference voltage generator circuits.

Layout of a single pixel cell is shown in Figure 13. The centre of each pixel (5.4 μm x 5.4 μm) is open (no metal) to allow light illumination testing. Four p+ junctions are created in each pixel, with each junction of octagonal shape and a width of 4.4 μm.

I-V characteristics of the detector are shown in Figure 14. Voltage is applied from the backside Al pad. Almost the same characteristics are obtained using the HV ring pad. We could apply more than 90V without breakdown for FY05 chip. In the FY06 chip we have used a smoother corner for the bias and guard rings, increasing the breakdown voltage to 110 V. As stated before, we also fabricated a deeper implant chip, and it could extend breakdown voltage to 130V.

Due to the back gate effect, which will be discussed in the next section, detector voltage operation is limited to a much lower value to permit operation of the electronic circuits.

We took images of a plastic mask placed in front of the pixel detector and illuminated with red laser light (670 nm wavelength). An image taken with 128 x 128 pixels is shown in Figure 15. The detector bias voltage is 1V and the integration time is 24 μs. The pedestal voltage during a reset period is subtracted for each pixel. The signal collected in the white (saturated) part of the detector is estimated to be about 20,000 photons based on laser intensity and pixel geometry. Pixel capacitance is estimated roughly as 8 fF, so the induced voltage of the sensor node is about 400 mV. This is consistent with the observed signal amplitude.

We also confirmed the sensitivity to β-rays by using a ^{90}Sr β-ray source. We observed a signal voltage jump of 70mV in the sensor. This is consistent with a depletion depth of 44 μm and a generated charge of 3500 e- (0.6 fC).

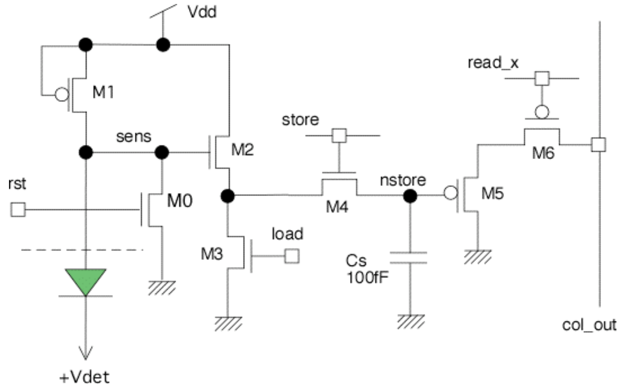

Figure 12: Schematics of a single pixel circuit.

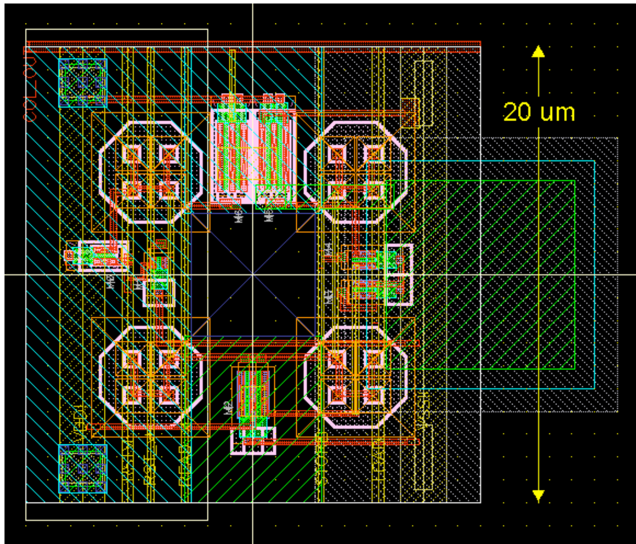

Figure 13: Layout of a pixel cell. Each pixel has 4 p+ implants of octagonal shape. At the right of the cell is the storage capacitor. The pixel centre is left free of metal to allow light illumination testing.

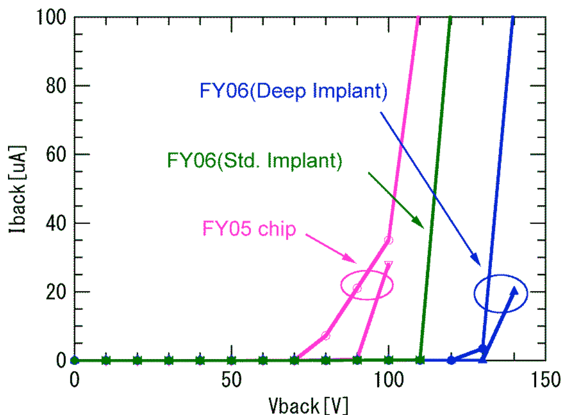

Figure 14: Measured Iback -Vback curves for various OKI SOI pixel detectors.

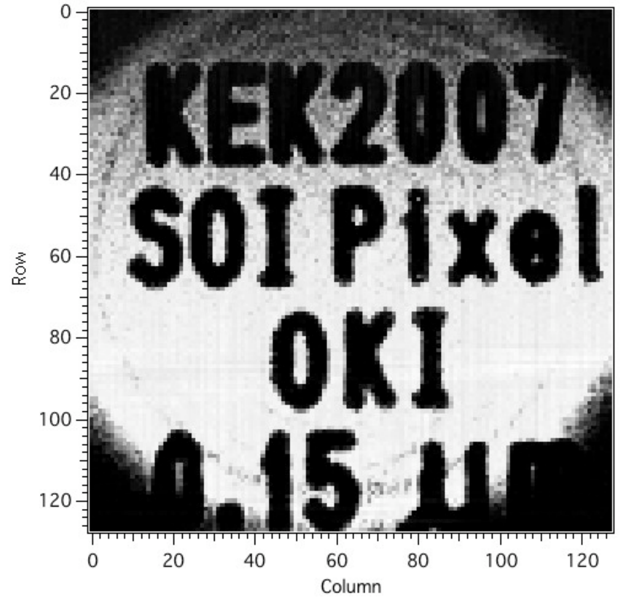

Figure 15: An image taken by the pixel sensor with a 'KEK2007' mask. Exposure time is about 24 μs, and detector bias voltage is 1V. Characters are written on a plastic mask for printed circuit lithography and the diameter of the laser light is about 3mm ϕ

IV. TCAD STUDIES

To understand the behaviour of the SOI pixel detector, Technology CAD (TCAD) which simulates process and device operation is very useful. We used a 3D-TCAD simulator called ENEXSS [21], which is developed by a Japanese consortium called SELETE.

Some of the preliminary results are shown below, though these results are extracted from a very small scale simulation and do not yet cover a full size detector.

A. Back Gate Effect

The potential under the BOX acts as a back gate of the transistors in the top Si. As the back gate voltage is increased, the NMOS transistor threshold voltage is decreased and that of the PMOS is increased. Finally the circuit stops working for excessive back gate voltage.

This is confirmed in test chips by observing an input-output signal of the I/O buffers where no p+ implant exists, so the detector voltage is almost directly applied to the back of the I/O buffers. In this case the output signal becomes very small when the back voltage exceeds 15V.

This back gate voltage can be reduced by placing a p+ implant near transistors and connecting it to ground voltage. This is confirmed with ENEXSS simulation as shown in Figure 16. By placing the p+ implants within 10 μm of the transistors, the threshold voltage shift can be reduced to less than 100 mV at a back voltage of 40V.

Since there was no time to redesign new I/O buffer cells, we just surrounded the I/O buffers with a p+ ring as close as possible. We observed the back gate effect is greatly reduced

and the I/O signal does not disappeared even in 40V back voltage.

B. Circuit to Sensor cross talk

In a SOI pixel detector, the electronics circuit and the sensor are separated by the BOX layer. The thickness of BOX in the present process is 200 nm. Although good isolation between circuit elements is expected in SOI, as stated in the previous section, cross talk studies between circuitry and sensor is still important.

Figure 17 shows simulated electric field strength and lines of electric force. There is a p+ implant in the upper left and a metal signal line at the upper right. Voltage change in the metal line disturbs the electric field, so some amount of charge is induced through capacitive coupling. In some applications, this may not be negligible. In that case, we should use differential signals and/or make guard structures to sensors. Proposed transistor structures for the next generation, such as double gate and FIN transistors (Figure 18), might reduce the cross talk.

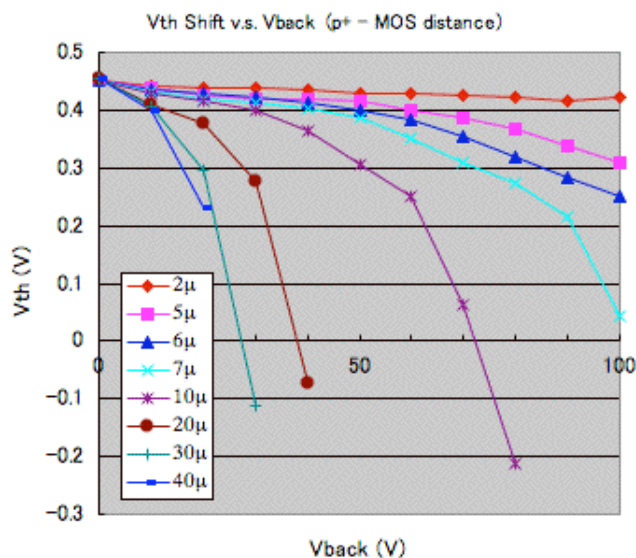

Figure 16: Simulation for NMOS threshold voltage vs. back voltage (Vback). Each curve corresponds to the distance between the NMOS and the p+ implant. By placing p+ implant near the NMOS, the shift of the threshold voltage is reduced.

Table 2: Process differences between OKI 0.15 μm and 0.2 μm SOI CMOS processes.

Process	0.15 μm	0.2 μm
Wafer Diameter	6 inches	8 inches
Core (I/O) Voltage	1.0V (1.8V)	1.8V (1.8/3.3V)
Gate Length	0.14 μm	0.2 μm
Gate Oxide Thickness	2.5 / 5 nm	4.5 / 7 nm
BOX Thickness	200 nm	200 nm
Off state Tr. Leak Current (Ioff)	< 100 pA/mm	< 0.1 pA/mm

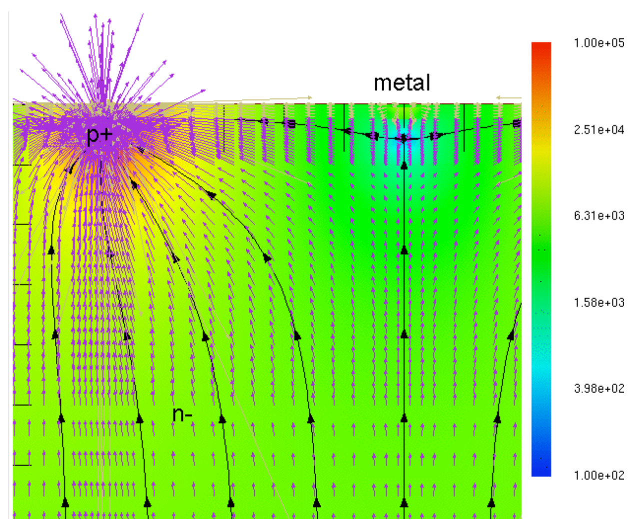

Figure 17: Electric field map and lines of electric force around a p+ sensor node simulated using ENEXSS.

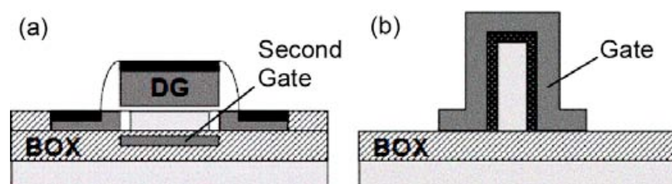

Figure 18: Structures of future SOI transistors; (a) double gate transistor, (b) FIN transistor.

V. SUMMARY AND FUTURE PLAN

SOI technology is envisaged as a mainstream technology in future LSI processes. In addition, it has many fascinating features useful for high-energy and space applications.

We have started a development of a monolithic SOI pixel detector. The detector consists of a wafer-bonded sensor of high-resistivity Si mated to a CMOS circuit in low-resistivity Si. We use a commercial (OKI 0.15 μm SOI) process with commercial wafers (SOITEC).

Two submissions in this process were done and showed good initial performance for light and β-ray detection. Several issues specific to the SOI structure are being studied with ENEXSS simulations.

We are planning the next submission for December 2007 (FY07 run). Due to a process line change at OKI, we will use a 0.2 μm SOI CMOS process in the next MPW run. Major differences between these processes are listed in Table 2. Although the feature size is somewhat increased, higher operating voltage and reduced transistor leakage current can be obtained in the 0.2 μm process. We welcome more participants to join the MPW run.

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