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Electronics and Sensor Study with the OKI SOI process

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We are evaluating SOI (Silicon-On-Insulator) technology for radiation-hard electronics and monolithic radiation sensor applications. The process we used is a 0.15um CMOS, fully-depleted SOI technology developed by OKI Electronics Industry Co. Ltd.
This SOI device has two Si layers; one is a thick substrate (handle wafer) which is Czochralski high-resistivity silicon, and another is SOI layer which is 40nm thick, low-resistivity silicon. Those Si layers are separated by a 200nm thick buried oxide (BOX) layer.
The SOI layer is used to implement standard CMOS circuits. Although the handle wafer is normally just a physical structure in the SOI device, we developed a process to create p-n junctions in the handle wafer and connect them to transistors in SOI layer. Thus the handle wafer can be used as a radiation sensor.
Since there is no mechanical bonding between the sensor and electronics, the capacitance of the sensor node is very low and it has excellent sensitivity to irradiation. By thinning the handle wafer, we can make low-material pixel detectors.
We submitted first test designs at the end of 2005, and had successful results of test chips consisting of a 32x32 pixel detector, strip detectors and front-end electronics chips. At the end of 2006, we then performed our own MPW (Multi Project Wafer) run by collecting 17 different designs from US and Japanese universities/laboratories.
The OKI SOI process and the results from this MPW run are presented.

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