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3D System Integration for high density interconnects

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3D-Integration is a promising technology towards higher interconnect densities and shorter wiring lengths between multiple chip stacks, thus achieving a very high performance level combined with low power consumption. This technology also offers the possibility to build up systems with high complexity by combining devices of different technologies. Ultra thin silicon is the base of this integration technology. The fundamental processing steps will be described, as well as appropriate handling concepts.
Three main concepts for 3D integration have been developed at IZM. The approach with the greatest flexibility, called Inter Chip Via - Solid Liquid Interdiffusion (ICV-SLID), is introduced. This is a chip-to-wafer stacking technology which combines the advantages of the Inter Chip Via (ICV) process and the solid-liquid-interdiffusion technique (SLID) of copper and tin. The fully modular ICV-SLID concept allows the formation of multiple device stacks. A test chip was designed and the total process sequence of the ICV-SLID technology for the realization of a three-layer chip-to-wafer stack was demonstrated. The proposed wafer-level 3D integration concept has the potential to build multi-layer high-performance chip stacks and is well suited as a replacement for embedded technologies based on monolithic integration. To address yield issues, a wafer-level chip-scale handling is presented as well, to select known-good dies and work on them with wafer-level process sequences before joining them to integrated stacks.

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