Fault-Tolerant and Radiation Hardened SPARC Processors

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Outline

- Historical Background
- LEON2FT & AT697
- LEON3 and GRLIB
- LEON3FT Projects
- Software tools overview
- Conclusion
Why SPARC architecture?

- In 1991, a 32-bit replacement for 1750 was needed by projects like HERMES and COLUMBUS
- ESA performed two architectural studies, evaluating processors such as MIPS, THOR, MC68020, I386, NS32
- ESA also invited industry for round-table discussions
- Finally, SPARC was selected due to:
  - Open architecture without patents or license fees
  - Well designed and documented
  - Easy to implement
  - Established software standard
  - Available design (CY601)
ERC32 Development

- 32-bit SPARC V7 architecture based on Cypress 601
- 0.8 um CMOS/EPI, 50 Krad, SEU LET: 15 MeV
- 3-chip solution (IU, FPU, MEC)
- 14 MHz, 10 MIPS, 2 MFLOPS
- Error-detection through parity on all registers and buses
- Proof-of-concept 1991 (SS2 parts + GALs)
- First prototypes in 1996
- First flight parts in 1998
3-chip ERC32 flight projects

- The 3-chip ERC32 has been used in four space projects
  - Control computer for Space Station (DMS-R)
  - Control computer for Automatic Transfer Vehicle (ATV)
  - PROBA-1 Control Computer
  - Standard Payload Computer (SPLC)
- 3-chip ERC32 was discontinued in 2002
Space Station Control Computer
Space Station Control Computer

- Installed in Russian Module 'Zvezda'
- 2 x FT Voting computers + 2 control post computers
- Guidance, Navigation and Control of entire Space Station
- Operating system: VxWorks + Voting FT layer
- Application software developed by RCS Energia (Russia)
- Launched July 2001
- Working nominally since launch
Automated Transfer Vehicle

- ATV re-fuels and boosts Space Station
- ERC32 FT Computers Based on DMS-R
- Launch 2008
Standard Payload Computer

- VME-based system for payload control in Space Station
- 14 Mhz ERC32, 6 Mbyte RAM, 80 Mbyte mass-memory
- Ethernet, 1553, Analog + Digital I/O, Video
PROBA-1

- Project for On-Board Autonomy
- 10 MHz ERC32
- VxWorks O/S
- 50,000 lines of C-code
- Launched October 2001
- Still operational
**ERC32 Single-chip TSC695**

- Developed to reduce cost and improve performance
- 0.5 um rad-hard CMOS, 300 Krad, SEU LET: 50 MeV
- 20 MHz, 14 MIPS, 4 MFLOPS, 0.5 W
- First samples in 1999
- Parity error-detection of on-chip registers and buses
- Current baseline processor for all ESA missions
- Used also outside Europe: US, Israel, India, China
- Used in many projects: Cryosat, GOCE, Herchel/Planck, SMART-1, SPACEBUS-4000, Ariane-5, Galileosat, Aelous, Deep-Impact, various military
Experienced problems with ERC32

- Proprietary design, difficult to port
- Limited to 20 MHz due to external memory timing
- Non-standard complex I/O interface
- Low-performance DMA
- Not possible to use for SOC design
- No high-level simulation model
- No support
- Bugs...
LEON project

- To create a European-designed SPARC processor
- 100 MIPS, 20 MFLOPS performance
- Rad-hard and SEU free
- Standard interfaces
- Modular
- Portable
- Written in VHDL
- Project budget until first prototype: $250K
First LEON design: LEON1FT

- SPARC V7 5-stage pipeline
- Separate, direct mapped instruction/data caches
- Meiko FPU (ERC32)
- Custom on-chip bus
- 32-bit PROM/SRAM memory controller with EDAC
- Portable VHDL model
- Synthesizable for ASIC and FPGA
- Extensive fault-tolerance to cope with SEU on soft process
- Released in open-source to improve test coverage
LEON1FT layout
LEON1FT Details

- LEON1FT implemented on Atmel 0.35 um CMOS process
- Purpose: to demonstrate fault-tolerance SEU protection
- 2 x 4 Kbyte cache
- Full TMR on all registers
- (39,7) BCH EDAC on register file
- (34,2) parity on cache memories
- Master/checker capability
- 30 mm², 100 Kgates
- 50 MHz, 10 MFLOPS, 0.5 W, 3.3 V
- Prototypes available 2001, fully functional
- SEU tested using heavy-ion injection (Cyclotron Louvain)
LEON1FT SEU test board
LEON1FT SEU results

- ~10,000 errors were injected in two test campaigns
- Full detection and correction of all errors
- No software impact
- No master/checker errors
- FT concept considered successful
LEON1FT Cyclotron setup
Improved performance: LEON2FT

- SPARC V8 5-stage pipeline with hardware MUL/DIV
- Multi-set caches with LRU
- On-chip AMBA bus for modularity
- 32-bit PC133 SDRAM controller with EDAC
- 32-bit full PCI interface with DMA
- On-chip debug support unit (DSU)
- Maintained LEON1 FT logic
- Targeted for 100 MHz on 0.18 um processes
- 120% performance improvement over LEON1
LEON2 Block Diagram

- DSU
- LEON2 SPARC
- Icache
- Dcache
- AHB I/F
- FPU
- UARTS
- TIMERS
- IOPORT
- AHB/APB
- PCI
- PROM
- SRAM/SDRAM
- RS232
- I/O

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LEON2FT UMC Demonstrator

- Purpose: evaluate FT concept on 0.18 um process
- Synthesized for UMC 0.18 um CMOS, commercial lib.
- Full FT with EDAC, parity and TMR with skewed clocks
- 2 x 2 x 8 Kbyte caches (32 Kbyte total), InSilicon PCI bridge
- New SDRAM controller with EDAC + HW MUL/DIV + DSU
- 100 MHz, 250 mW, 5 mm2
- Manufactured end-2002, device fully functional
- SEU tested through heavy-ion injection (Cf-252)
- FT logic successful, removed all 1,000 errors
- SEL due to commercial libraries – not useful for space
LEON2FT UMC layout
LEON2FT prototype board
AT697E/F: LEON2FT Flight parts

- LEON2FT on Atmel Rad-Hard 0.18 um process
- Full FT with EDAC, parity and TMR with skewed clocks
- 48 Kbyte cache, InSilicon PCI bridge
- SDRAM controller with EDAC + HW MUL/DIV + DSU
- 100 MHz, 3.3V I/O, 349-pin CGA package
- Samples Q2 2005, flight parts Q4 2008 (TBC)
- Export license required
- Exclusive rights licensed to Atmel (F)
- Designed by Gaisler Research under ESA contract
AT697 Validation board
LEON2FT/GRLIB SOC projects

- Astrium AGGA-3 GPS/Galileo receiver (GRFPU)
- Saab COLE Controller (GRFPU, MMU-FT)
- LABEN Spacecraft controller (GRFPU)
- Saab/Gaisler RTC Instrument controller (ESA)
- Alcatel Alenia PMRM Spacecraft controller
- All devices produced by Atmel due to exclusive license of the LEON2FT design
The next step: GRLIB and LEON3

- Increased use in SOC designs requires a more efficient design methodology and IP library
- Identified requirements:
  - Common interfaces
  - Unified synthesis and simulation scripts
  - Built-in portability
  - CAD tool independent coding style
  - Unrestricted licensing
  - SEU tolerance for space applications
GRLIB IP Cores

- 32-bit LEON3 SPARC processor
- High-performance IEEE-754 floating-point unit
- 32-bit PCI bridge with FIFO and DMA
- 10/100/1000 Mbit Ethernet MAC
- PROM/SRAM/SDRAM controller with BCH or Reed-Sol.
- AHB round-robin arbiter, APB bridge
- Utility cores: UART, timer, interrupt control, GPIO, ...
- Memory and pad wrappers for FPGAs and ASIC
- CAN-2.0, MIL-STD-1553, Spacewire
- USB-2.0, DDR1, DDR2, SPI, I2C
LEON3 SPARC V8 Processor

- 7-stage pipeline, multi-processor support
- Separate multi-set caches with LRU/LRR/RND
- On-chip debug support unit with trace buffer
- 250/400 MHz on 0.18/0.13 um, 250/400 MIPS, 25 Kgates
- 125 MHz on Virtex2pro FPGA, 3500 LUT
- 25 MHz on RTAX2000, 8000 cells (25%)
- SEU tolerance by design for space applications
  - Pipelined FT to avoid timing impact
  - Corrects up to 4 errors in each register/cache word
  - Auto-flush of faulty cache lines avoids error build-up
LEON3-FT Template Design

DSU → LEON3 SPARC

LEON3 SPARC → FPU

FPU → UARTS

UARTS → TIMERS

TIMERS → IOPORT

IOPORT → AHB/APB

AHB/APB → AHB

AHB → DSU

DSU → MEM CTRL

MEM CTRL → PCI

PCI → SPW

SPW → CAN/ETH

CAN/ETH → RS232

RS232 → I/O

I/O → ENABLE

ENABLE → BREAK

BREAK → ACTIVE

ACTIVE → DSU LINK

DSU LINK → PROM

PROM → SRAM/SDRAM

SRAM/SDRAM → PCI

PCI → LVDS

LVDS → PHY

PHY → CAN/ETH

CAN/ETH → RS232

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LEON3 Projects

- **LEON3FT Actel RTAX2000**: MicroSat, TubiTac, DLR (2x), Assurtech, Uni.Bergen, Syderal, SSC, General Dynamics, Ball Aerospace, Acer, NSPO
  - Flight parts (RTAX2000S-1) delivered to MicroSat, launch on TacSat-3 October 2007
  - Flight in 2008: ARGO, PRISMA

- **LEON3FT ASIC designs**: SCOC (Astrium), Aeroflex UT699, LEON3FT-DARE (ESA), Ramon GR702/712, LEON3FT-IHP, LEON3FT-GINA (ESA)

- **Commercial LEON3 systems**: AiSeek, ACARD, ARC, Alpha, BridgeCo, Comsis, Eonic, Fresco, Gigle, Javad, Orbita, Orbital Research, Radionor, Satrec, Siemens, Silverbrook (2x)
RTAX LEON3/GRLIB configurations

- Pre-programmed fixed LEON3FT systems on RTAX2000
- Delivered as programmed components from Actel
- Four baseline configurations:

<table>
<thead>
<tr>
<th>Core</th>
<th>Instrument</th>
<th>U.S. Config</th>
<th>EUR config</th>
<th>Mixed config</th>
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<tbody>
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<td>Memctrl + EDAC</td>
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<tr>
<td>Std peripherals</td>
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</table>

Other configuration possible on custom order
SOC Design Kit also available
LEON3FT (RT)AX development board

- (RT)AX2000 device in CGA624 or FBGA896 socket
- 4 Mbyte SRAM + 256 Mbyte SDRAM with ECC
- 10/100 Mbit/s Ethernet, Spacewire, 1553, 33 MHz PCI
- CPCI Form factor
LEON3-FT-RTAX SEU Test Setup

- 168 hour SEU test injection (Cf-252) completed
- FT fully successfull, report available on-line
LEON3-FT-RTAX SEU Test Setup

- Vacuum chamber with Cf-252 source
LEON3-FT RAMON Project

- Objective: to implement a LEON3FT system using Ramon Chips 0.18 um rad-hard library (Tower)
- GR702 prototype produce end-2006
  - Extensive characterisation and radiation testing
  - Device fully functional and radiation hard
- GR712 high-performance version
  - 2-CPU MP system, 32 Kbyte cache, GRFPU
  - 6x Spacewire, 2x CAN, 2x Ethernet
  - ~ 150 MHz operation, < 1W
  - Sold as component, support by Gaisler
Figure 1: Block diagram of GR712RC
LEON3FT 0.25 um ASIC demonstrator

- IHP 0.25 um CMOS process, 100 MHz, 3.3 V
- First samples manufactured in August 2005
- Manufactured on Rad-Hard library Q4-2007 (Dolphine)
LEON3FT MP Project (GINA)

- ESA research project, started September 2005
- 4-processor SMP system for high-end space application
- Goal: 1 GIPS / 1GFLOPS @ 266 MHz (GAIA requirements)
- 4 x Spw, PCI, 2 x CAN, Ethernet, 4 x serial
- Prototyped on XC2V6000 / XC4LX200 boards
- Ecos, RTEMS MP software adaptation
- VxWorks bsp
- ASIC prototype 2008
LEON3FT MP Architecture (GINA)
LEON3FT MP Prototype board
XC2V6000 & XC4VLX200
## LEON2/3FT Device Overview

<table>
<thead>
<tr>
<th>Device</th>
<th>Peripherals</th>
<th>Radiation</th>
<th>MIPS</th>
<th>Availability</th>
<th>Process</th>
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<tbody>
<tr>
<td>TSC695E</td>
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<td>20</td>
<td>Now</td>
<td>Atmel 0.5</td>
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<td>Now</td>
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<td>UMC 0.15</td>
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<td>Now</td>
<td>Tower 0.18</td>
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<td>Tower 0.18</td>
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<tr>
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<tr>
<td>UT699</td>
<td>Eth, CAN, SpW</td>
<td>100 Krad</td>
<td>65</td>
<td>2008</td>
<td>UMC 0.25</td>
</tr>
</tbody>
</table>

COLE, SCOC and PMRM are proprietary designs
GINA, IHP and DARE are only research prototypes
LEON3 Software Tool-chains

- ECOS open-source kernel
  - Supports SMP synchronisation of up to 8 CPUs
- RTEMS
- uClinux & Linux-2.6 (SMP & MMU)
- VxWorks 5.4 and 6.3, MMU support
- Aonix Ada
- ThreadX
- Bare-C & Pthreads
- Mentor Nucleous end-2007
LEON3 Software Support tools

- GRMON plug&play debug monitor
  - Debug 'drivers' for each specific IP core
  - Modules allow IP vendors to provide own drivers
- TSIM high-performance LEON3 simulator
- GRSIM modular simulator
  - Modular, re-entrant simulator based on TSIM
  - Can simulate any number of buses, cores or cpu's
  - Vendor independent models
- GDB/DDD
- Eclipse C/C++ IDE
Summary

- LEON2 and LEON3 are well received by the international space community, and will be the baseline processor cores for both US and European devices and systems.
- The portability of the LEON3 model allows fast and simple implementation on new technologies (or FPGAs).
- A rich software environment is available, based on both commercial and open-source software tools.
- The dual-use and open-source approach of the LEON3 model guarantees long term availability and support.