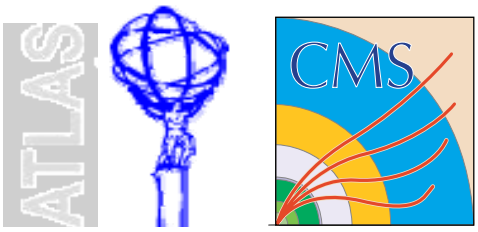
Joint ATLAS/CMS NOTE 2007/002



Joint ATLAS-CMS working group on optoelectronics for SLHC

Report from sub-group C Optical Link Evaluation Criteria and Test Procedures

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Abstract

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1 Introduction

This document proposes the evaluation criteria and test procedures for optical data links that are developed to read out the detector front-end electronics in ATLAS and CMS for the LHC upgrade (SLHC). These optical links need to be radiation resistant to the requirement of the detectors' operational lifetime in the SLHC. The goal of this document to develop standardized test procedures and evaluation criteria for future designs and tests to follow, and to make our testing work for optical link R&D projects simpler and more effective. In doing so, we also document and maintain our expertise on multi-gigabit per second radiation resistant optical link systems for particle physics experiments.

The tests have two levels: the optical link system level and the component level. The tests also have two parts: the laboratory (in-lab) functional measurements and the irradiation resistance evaluations. We will concentrate on the laboratory functional tests. The radiation resistance tests are discussed in detail in this joint working group's subgroup B (ref. subgroup B document).

2 The laboratory tests

A block diagram of a typical optical link (the physical layer) is shown in the following figure.

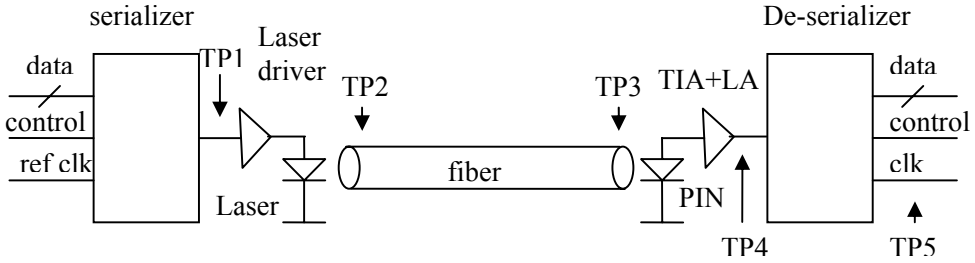

Fig.1. An Optical data link block diagram. The laser driver plus the laser are usually inside one subassembly that is called the OTx (optical transmitter). The PIN diode with the trans-impedance amplifier (TIA) and the limiting amplifier (LA) are usually inside one subassembly that is called the ORx (optical receiver).

Test points TP1 to TP5 are defined as the following: TP1 is at the electrical output of the serial bit stream from the serializer. TP2 is at the output of the laser, usually tested with a short section of a fiber. TP3 is at the input to the PIN diode, usually tested at the end of the fiber with the full length in the application. Both TP2 and TP3 are optical signals of the serial bit stream. TP4 is the electrical signal at the input of the deserializer. TP5 is at the parallel data and clock output from the deserializer.

At the link system level, the following properties need to be characterized:

1. The input and output (parallel) data timing diagram with respect to the reference (input case) or recovered (output case) clock.
2. The range of data transmission rate and associated reference clock frequency.
3. System latency (excluding fiber propagation delay).
4. Eye diagrams at TP1, TP2, TP3 and TP4 and the eye mask tests at TP2, TP3 and TP4. Electrical signals at TP1 and TP4 (usually LVDS) need to be checked against their design specifications. From the eye diagram the following information needs to be extracted: the rise and fall times (20%-80%) of the signal waveform, the jitter in the serial bit stream triggered with the reference (frame) clock, the optical power levels (high, low and average) at TP2 and TP3.
5. The BER as a function input optical power to ORx.
6. The maximum transmission range (the length of the fiber) at the specified bit error rate (BER) or mask margin over a certain type of fiber at the specified data rate.
7. The reference clock jitter tolerance as a function of the bit error rate (BER); the output (recovered) clock jitter.

8. Other general system parameters: power supply voltages and consumption of each component, optical power margins and a powering up/reset scheme.
9. The measurement of the system should cover a range of operational conditions such as temperature, humidity, vibration, magnetic field, if applicable.

At component or subassembly level, a subset of the above properties will be characterized, for instance:

1. The serializer reference clock jitter transfer function.
2. The latency introduced at each component (serializer, OTx, etc) level.
3. The serial bit stream jitter measurements at TP1, TP2, TP3 and TP4, hence to learn the jitter contribution from the OTx and the ORx and the signal dispersion introduced by the fiber.
4. The optical power output of the OTx.
5. The optical power attenuation of the fiber.
6. The sensitivity of the ORx (for example at BER of 10^{-12}), hence the optical power budget is measured.

The measurements are conducted at room temperature (about 25 degree C) and normal humidity condition. For applications in extreme conditions (below 0 degree C or above 40 degree C, or in high humidity environment, high magnetic environment), additional tests in operational condition are recommended.

Reliability tests and accelerated aging tests at component or subassembly level are recommended. Reliability tests at system level are suggested to study the weakest point in the system.

3 Definitions and procedures

The definitions presented below will evolve with time and experience. Please look for the latest issues of this document.

3.1 BER

A BER measurement is usually carried out with a parallel pseudorandom data pattern as input to the link, or a pseudorandom bit stream (PRBS) at component level (ex. the test only on OTx). The BER requirement of 10^{-12} in many cases is based on Gigabit Ethernet standards. Commercial components for this data rate range are usually specified to have a BER better than 10^{-14}. A BER measurement that reaches 10^{-12} takes at least 14 minutes at 1.25 Gbps, or 7 minutes at 2.5 Gbps, depending on desired confidence level. For optical links that operate slower than 1 Gbps, the BER requirement may need to be scaled down to a proper value so that the measurements can be carried out in a reasonable time period.

3.2 Jitter

Jitter in a clock or bit stream in the time domain is also classified as random jitter and deterministic jitter. A useful discussion about the jitter measurements are posted at http://www.physics.smu.edu/~scalise/SMUpreprints/SMU-HEP-04-10.pdf. One may also use a commercially available jitter analyzing package such TDS7BUPJA3 package for TDS7000B, Tektronix, to extract the information on different jitter components.

Jitter of a clock or a bit stream has two components: the amplitude and the frequency. A function generator with controlled jitter injection is needed to carry out the jitter tolerance measurement. A typical system reference clock jitter tolerance plot is shown here:

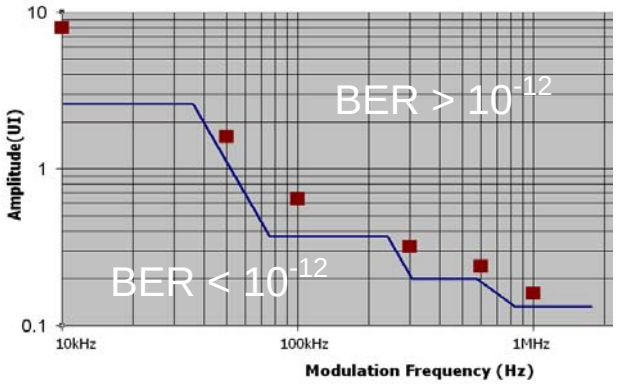

Fig. 2. The GOL-TLK link system reference clock jitter tolerance measurement. The red squares are the measurement results. The blue line is the set requirement on the reference clock jitter.

3.3 Eye mask

Eye mask tests at TP1, TP2, TP3 and TP4 at industrial standard transmission rates are defined by IEEE, ITU and other documents (example: 1000BASE-SX in IEEE 802.3z standards for gigabit Ethernet transmission over fiber optic operating in multi-mode and 850 nm wavelength). In applications where custom data rates are used, a proposed definition of the eye mask is shown in the following figure. The mask is defined 20% above the low level (usually logical 0) and 20% below the high level (usually logical 1) in the vertical axis (usually the voltage or optical power); 20% within the crossing points in the horizontal axis (the time). Most sampling oscilloscopes provide the possibility for users to define a user eye mask. A clean clock, usually the reference clock to the optical serializer is used as the trigger to the oscilloscope for the eye diagram measurement. If any dots are found within this eye mask, they may cause bit errors and the eye mask test fails.

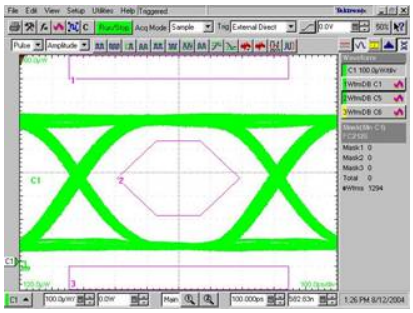

Fig. 3. A typical eye diagram with an eye mask defined 20% within the eye as shown as the red hexagon. Limits on waveform over and under shoots are also marked with the red rectangles above and below the green eye diagram.

Limits on waveform over and under shoots are usually also checked through the eye mask test. Signals with over and/or under shoots will not cause bit errors, but indicate maladapted circuits in the design.

3.4 Optical power budget

The optical power budget is the margin between the lowest signal received from the transmitter by the photodiode and the receiver sensitivity. It is usually designed in such a way that the transmitted optical power respects the laser safety requirements (European and the US standards) and in the meantime maximizes the received optical power. Typically a 10 dB optical power budget, but at least 3dB is recommended. This is mostly an issue of the ORx sensitivity at component level and in the system implementation level. Whenever possible, eye-safe laser output power levels should be used.

3.5 Other tests

Reliability and life tests are usually performed at an elevated temperature (but still within the maximum operational limit), with all the other parameters (power voltage, humidity, etc) set at recommended values. A reference on life test performed on one optical transmitter is posted here: http://cdsweb.cern.ch/record/955111.

4 The irradiation tests

The irradiation test procedures and evaluation criteria are discussed and documented by the ATLAS CMS opto-electronics joint working group, subgroup B. A full scale of the functional tests both at the link system level and at the component level are recommended to be repeated, either during irradiation, or before and after the irradiation and during annealing periods. Reliability is recommended to be re-evaluated after the irradiation tests. For all these tests the standardized setup described in this document could be used, as documented in section 5.

5 The reference optical link and a standardized test setup

Both in-lab and irradiation tests, and both at component and system levels need special equipment and setups. These test setups are usually a complete link system even for tests at component level. In order to standardize the test procedures and to make the preparation of these tests more effective, the idea of a **reference optical link** is proposed. This reference link does not replace the radiation resistant link that is under development. Instead, the reference link functions as a bench mark for the link (or component inside a link) to be tested against. The building blocks of the reference link (see block diagram below) may also function as building blocks for users to quickly reconfigure into a **standard test setup** with the components under development to be tested in. When a complete user link needs to be tested, one may use the building blocks of the reference link as data generator and error checking (like a parallel BERT) to the link. One possible prototype of this reference link is to be designed and built using FPGA based serializer and de-serializer channels. Both Altera and Xilinx have such FPGA chips. For example the ALTERA Stratix II GX as serializer and deserializer that has a data transmission rate ranging from 622 Mbps to 6.375 Gbps, covering the industrial standards of 1.25 (1.6), 2.5 and 3.125 Gbps data rate. In the following diagram we use this FPGA as example to illustrate the idea. In the implementation stage, one FPGA chip should be chosen to simplify the development and make it economical. The reference link will be constructed with three modular boards: the serializer/deserializer (SerDes) board, the OTx board (laser driver + laser) and ORx board (PIN + TIA and limiting amplifier). The connection between the serializer board and the OTx board, the ORx board and the deserializer board are 50 ohm cable with SMA connectors; the connection between the OTx board and the ORx board will be optical fiber which may also be radiation resistant. The laser and PIN diode are to be soldered to their boards. They may be replaced with other lasers or PIN diodes to test these lasers or diodes. But due to the fact that this procedure may damage the soldering pads, it is suggested to use a new OTx or ORx board with the laser or PIN diode under testing. As for the laser side, bias and modulation currents should be adjustable in such a way that one can use a VCSEL or an Edge Emitting Laser.

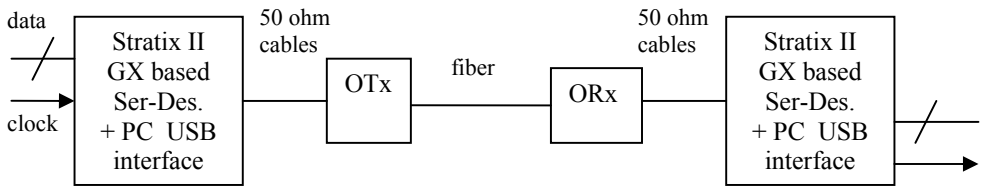

Fig. 4. Block diagram of the reference link. The input and output data bus is optional. Data can be generated and errors can be checked in the same FPGA chip on the same board (an implementation with a Stratix chip is shown here as example). A USB based PC interface is provided for data logging.

In this design philosophy, one can easily replace one of the three modular boards to construct a "custom" link to evaluate a component or a subassembly under development and test that in a complete link system. This construction also allows for irradiation tests of a component, especially in an online SEE measurement that requires a complete link system to be functional during the tests.

A standardized test setup with the above proposed SerDes board based on the Stratix II GX chip can be designed and constructed. Function blocks can be programmed in this FPGA. Proposed function blocks inside the Stratix II GX look like the follows:

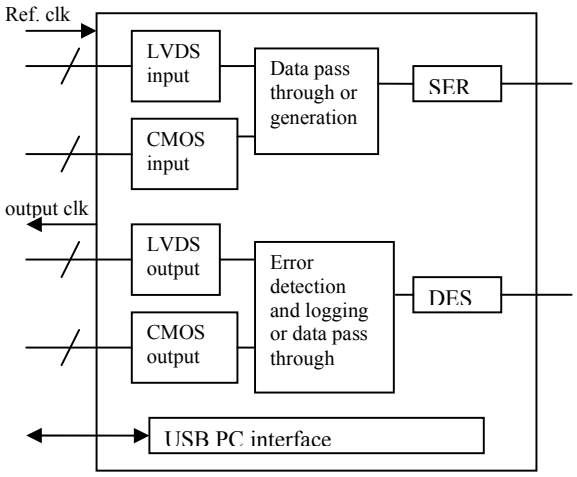

Fig. 5. Basic function blocks in the Stratix II GX FPGA chip. The USB PC interface provides control and DAQ over a distance of 40 meters, suitable for most tests.

One may construct a reference link using one or two of this Stratix II GX carrier boards plus one OTx and one ORx boards. One may replace the VCSEL on the OTx board or the PIN diode on the ORx board to carry out tests on these OE components. In the case of testing a serializer, for example the LOC chip, one may construct the test system shown below that may be used to test the LOC chip both in the laboratory and during irradiation.

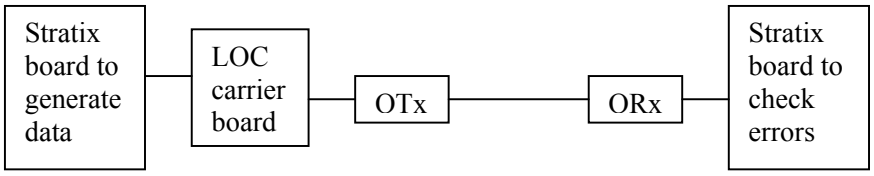

Fig. 6. Example of a LOC test link system. Here again the two Stratix blocks can be one or two boards. The LOC is an ASIC that integrates the serializer and the laser driver, maybe even the laser into one packaged chip. This ASIC is being developed based on a 0.25 μm silicon on sapphire CMOS technology for ATLAS LAr readout upgrade.

Another example would be to allow us to "quickly" construct a system to test the GBT and/or the Versatile Link (VL) with the building blocks from the reference link:

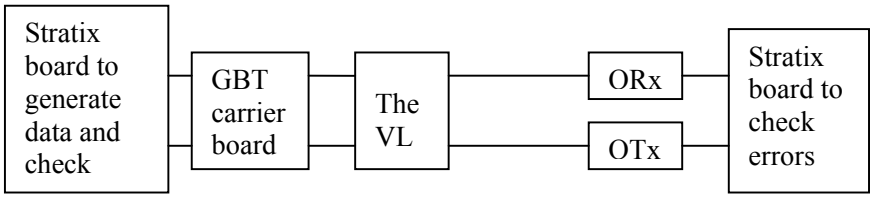

Fig. 7. Example of a GBT and Versatile Link test system. The GBT and VL are developments at CERN for the next generation optical readout.

Both the GBT and the VL can be placed in radiation for TID and SEE tests.

Standardized hardware requires and facilitates standardized firmware (FPGA code) and software (GUI). Because the Stratix II GX carrier board is the same in all link systems that are constructed, this makes it possible to have one package of firmware and software and to be developed (or adapted) by all the users and maintained at a few locations for a long period of time throughout the R&D phase.

One example of this standardized firmware is a proposed bit error testing scheme. In this scheme parallel PRBS are used for the data word to be transmitted. Automatic alignment at the receiver end is used to account for different transmission time due to different fiber length, different serializer delays. The error checker records three types of errors: type one, single bit flip. This is defined as when comparing the received word with the (re-)generated, there is one bit that is different. In this case, the bit location in the word and the flip type (from 1 to 0 or 0 to 1) are recorded together with a relative time stamp as precise as the reference clock (the parallel data clock); Type two: multi-bits flip in one parallel word. In this case the link keeps frame locked, that is, the following word is received correctly. In this error type, the number of bits that are incorrect is recorded with the time stamp; Type three: multi-bits flip in two or more consecutive words. We assume that this is because of the link frame loss. In this type of errors, only the duration of the frame loss is recorded with the time stamp at the beginning of the frame loss. All three types of errors are recorded in the receiver FPGA and stored in a FIFO to be transmitted to the PC. This way, together with the time stamp of each error, we will have complete information during a SEE test for off-line data analysis.

6 A list of suggested instruments

With the reference link, the following instruments are needed to carry out the tests discussed in section 2:

1. A clock and pattern generator with jitter injection.
2. A multi-GHz real-time oscilloscope with matching (differential) probes and an optical to electrical signal converter (O/E module), or a sampling oscilloscope with electrical and optical input modules. Jitter analysis software with these oscilloscopes is recommended to have.
3. An optical power meter.
4. An optical power attenuator.

7 Summary

Test procedures and evaluation criteria for radiation resistant optical links for the SLHC upgrade are discussed. The in-lab functional tests are described in this document, while the irradiation evaluation and tests are discussed in the subgroup B report. A specially designed reference optical link is proposed to benchmark the developed links, to standardize their testing, and to simplify the test preparations. Based on this reference link, standardized test systems can be constructed for component and subassembly tests.