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A complete set of firmware for the TileCal Read-Out Driver.

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TileCal is the hadronic tile calorimeter of the ATLAS experiment at LHC/CERN. The Read-Out Driver (ROD) is the main component of the TileCal back-end electronics. The ROD is a VME 64x 9u board with multiple programmable devices which requires a complete set of firmware. This paper describes the firmware and functionalities of all these programmable devices, especially the DSP Processing Units daughterboards where the data processing takes place. Finally, some results obtained during the TileCal commissioning phase are presented.

Summary

TileCal is the hadronic tile calorimeter of the ATLAS experiment at LHC/CERN. The central element of the back-end system of the TileCal detector is the Read-Out Driver (ROD). The TileCal ROD motherboard based on a common design for ATLAS calorimeters and it includes multiple programmable devices and two Processing Units daughterboards. These devices are programmed with a complete set of firmware code which is, in some cases, also common for both ATLAS calorimeters RODs. Both, the common and the TileCal specific firmware are described in this paper emphasizing on the Processing Units reconstruction algorithms.

The input data coming from front-end is received in the ROD through 8 Optical Receivers and transmitted to 4 Field Programmable Gate Arrays (FPGAs) (called StagingFPGAs). The StagingFPGA is the ROD input data distributor and transmits the received data to the Processing Units daughterboards. Two InputFPGAs receive, check and transmit the data in the PU towards two Digital Signal Processors (DSPs).The DSPs are the main component of the ROD since they are responsible for data reconstruction in real time at the ATLAS first level trigger rate. Besides, the DSP code also includes Timing, Trigger and Control (TTC) synchronization, Muon Tagging and Missing Et algorithms, histogramming, and real time behaviour information. In addition, the Output FPGA implements the interface between the PU and the VME bus and TTC system. The DSPs process and send the data to the ROD motherboard Output Controller FPGA (OC_FPGA). Finally, the OC_FPGA is the output data distributor and is responsible of data transmission to the Read-Out System (ROS) through the Transition Module (TM).

Two more FPGAs provide the interface with the VME bus (VME_FPGA) and with the TTC system (TTC_FPGA). Besides, some extra functionalities and recent firmware upgrades are also presented in this paper. Finally, some results obtained during the TileCal commissioning phase are also presented. During this phase the basic firmware and the recent upgrades are being tested as well as the DSP reconstruction algorithms.

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