Electronic Developments for the Hades RPC Wall: Overview and Progress

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Abstract

This contribution presents the current status and progress of the electronics developed for the Resistive Plate Chamber detector of HADES. This new detector for the time-of-flight detection system will contain more than 1000 RPC modules, covering a total active area of around 7 m^2. The Front-End electronics consist of custom-made boards that exploit the benefit of the use of commercial components to achieve time resolutions below 100 ps. The Readout electronics, also custom-made, is a multipurpose board providing a 128-channel Time to Digital Converter (TDC) based on the HPTDC chip.

I. INTRODUCTION

Recent advances on RPCs (Resistive Plate Chambers) have allowed since a few years ago to build RPCs with inexpensive materials and to use them for precise time-of-flight measurements at normal conditions of pressure and temperature. These detectors are becoming widely used because their excellent TOF capabilities and reduced cost, facing in some applications to the well assessed technology of plastic scintillators. The RPC detectors that will be installed in the low angle region of HADES (High Acceptance DiElectron Spectrometer) are used for both particle identification and triggering. 1024 double-sided readout detectors will be placed in an active area of about 7 m^2, distributed in 6 sectors, covering a polar angle between 12º and 45º with 2π azimuthal acceptance [1].

The electronic systems involved in the RPC wall are the Front-End that digitizes the signals from the RPC cells, the Readout that labels and packs the digital signals from the Front-End and the power supply board. All of them are based on custom-made boards.

HADES is currently installed at GSI Darmstadt (Germany), and has as main goal the detection of electron pairs produced in relativistic pion-nucleus and nucleus-nucleus collisions, with high invariant-mass resolution and high acceptance, to obtain information about the modification of the properties of vector mesons in nuclear matter, both normal and hot and compressed. HADES consists of several sub-detectors providing triggering, and particle identification and discrimination capabilities. Among these sub-detectors the RPC detectors cover the TOF system at low angles, where the particle rate is low enough, whereas plastic scintillator rods read by photo-multiplier tubes are set up for large angles. The new RPC detector will increase the granularity and time resolution to levels that will allow extending the range of possible collisions in HADES from C-C to Au-Au.

II. OVERVIEW OF THE CURRENT SYSTEM

The block diagram of the current electronics is shown in figure 1. Two different parts can be distinguished: on the right, the Front-End electronics and, on the left, the Readout system. Both systems are custom-made and have been built specifically to satisfy the requirements of the HADES RPC wall.

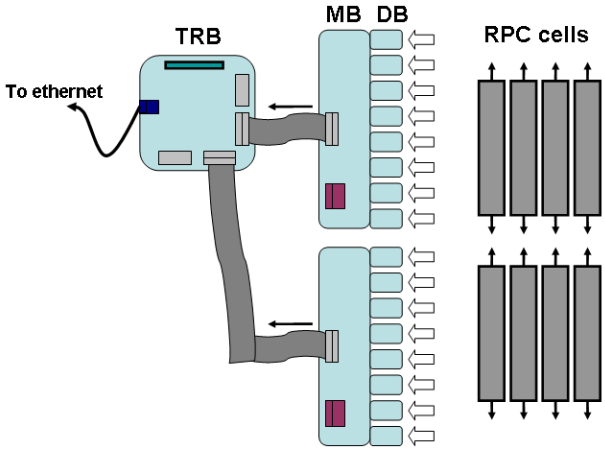

Figure 1: Block diagram of the current electronics and RPC cells.

The Front-End is built using only commercially available devices. The use of a dedicated Front-End analog ASIC for the read out of the detector signals would have been an excellent option for saving space and power, but the number of electronic channels (2048) is not big enough to consider this possibility. For this reason, the Front-End is based in a simple design to fit existing space constraints existing due to the geometry in the detector. A simple design also has de advantage of low power consumption, which is needed to minimize problems with heating. In any case, it is already foreseen the availability of air flow for the cooling of the electonics. Geometrical considerations were a key aspect to adopt the solution of implementing the Front-End in two separate cards, which are connected forming a 90º angle. Such

a way of connection, which is very unusual, made difficult the task of finding connectors with good features at high frequency. The solution adopted eventually was the use of small pitch card edge connectors from the SAMTEC HSEC8 series, specified at high frequency, to preserve the integrity of the transmitted signal.

The Front-End electronics deals with the short analog pulses provided by the RPC cells and digitizes them by means of wide-band analog electronics, while the Readout system is a digital system that provides convenient processing to separate valid events and discard non-relevant events.

The two cards of Front-End electronics are the Daughterboard (DB) and the Motherboard (MB). The DB takes analog signals from the RPC detector cells, and after the amplification, a fast single edge discriminator (leading edge method) generates digital pulses which leading edge gives the arrival time of the RPC signal. This arrival time is used to measure the time-of-flight of particles respect to a START signal (produced by a diamond detector located next to the target of HADES), and is used for particle identification. For the requirements of HADES a time resolution lower than 100 ps should be provided by the RPC electronics (including the detector response).

The leading edge method is very simple, but has as a counterpart the introduction of walk error in the time resolution (see figure 2). The walk error, which can be reduced by decreasing the threshold voltage of the discriminator, is limited by the fluctuations and noise in the base line of the signal. In the case of RPC signals this walk error is very small, due to the small rise time (typically 500 ps) of the RPC signals.

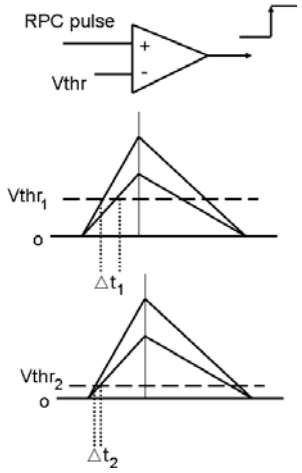

Figure 2: Leading edge and error dependent on the amplitude of the input signal.

To reduce the error and to improve the time resolution as much as possible, a measurement of the charge is performed. The usual method for charge measurement is the use of a shaper followed by an ADC to obtain a digital word that is send to the Readout system. However, a high particle rate requires parallel transmission via a data bus. To simplify this, the Time over Threshold method was adopted, which allows sending the information about the charge of the particle together with the timing pulse by just modulating the width of the pulse with the charge. Detailed information about the DB can be found in [2].

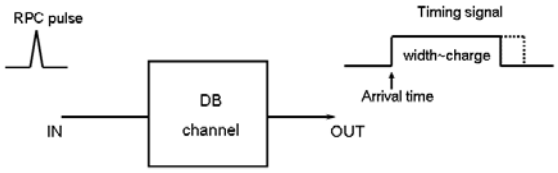

Figure 3: Timing output signal from a DB channel after the detection of an RPC pulse.

The digitized timing signals are converted into LVDS and transmitted via the MB to the Readout system. The MB not only delivers the timing-signals from 8 DB to the Readout board, but also has other important tasks: the MB supplies the stable voltages required by the DB (+5V,-5V,+3.3V), combines the 32 multiplicity signals coming from the DB to provides a low level trigger signal, allocates DAC for the threshold voltages of the comparators on the DB, provides test signals distribution and interface for DAC.

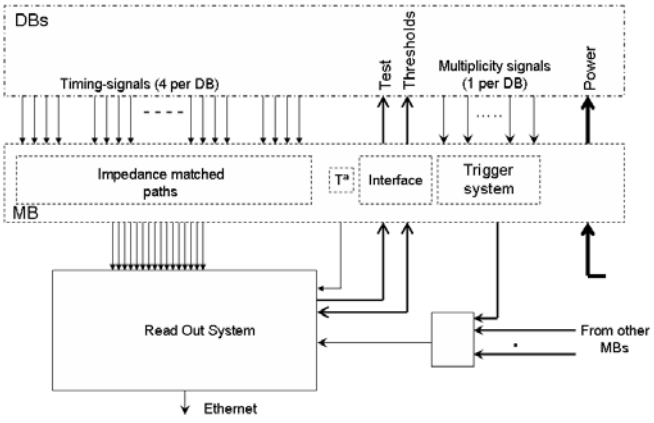

Figure 4: Block diagram of the Front-End and Readout interface.

To improve the performance of the MB, several updates were made respect to the first version [3]. Main changes are commented in the following lines.

A new feature was implemented on the MB to verify the correct programming of the DAC (implemented by the LTC2620 DAC set up in daisy chain). The normal procedure is the use ADCs for reading every channel output and to check if the voltage value is the correct one. Instead of this, and in order to simplify the electronics, the checking was limited to reading the content of the shift register of the DAC after every DAC programming operation. This is easily done by clocking out the data stored in the shift register and comparing this data with the programming data sent for setting the thresholds.

The test signals distribution on the MB was redesigned to eliminate the temporary manual switch present in the previous version. The idea is to deliver separate test signals to even and odd channels. These signals are generated from the Readout system and sent to the MB as LVDS signals via ribbon cable. Because of layout considerations, four LVDS repeaters placed on the MB distribute each test signals to odd and even channels of the DB. This set up facilitates the distribution of the signals along both sides of the MB due to the central position of the MB-TRB connector and the length of the MB (40 cm). The LVDS repeater used is the SN65LVDS100, featuring very stable propagation delay vs. temperature, and the receiver is the MAX913, that converts the LVDS signals to TTL to generate a narrow signal similar to the RPC pulses to be used as test signal and calibration purposes.

The ripple/noise filtering scheme on the MB was fully redesigned to increase the ripple/noise rejection on the MB and to guarantee stable supply voltage for the proper operation of the Front-End electronics. This issue is especially important, considering that the power supply system will be based on switching power supplies. The new design includes the addition on the MB of Low Drop-Out regulators (LDO), which have a very good power supply rejection ratio up to frequencies of 100 kHz in case of the positive regulators selected (ADP3338) and 10 kHz for the negative ones (LT1175). The LDO selected can be operated with extremely low ESR capacitors (ESR ≈ 0), which is an advantage for noise rejection and ensures the stability of the regulators.

Switching power supplies output contain ripple at the switching regulator frequency (typically some hundreds of kilohertz), and noise from the transition times of the power switches at very high frequency that can be identified as spikes superposed on the ripple. Nevertheless, as commented previously, the ripple/noise rejection of the regulators is good only until some frequency. As a result, the regulators are not efficient in rejecting noise, and it is necessary to add external filters to reduce it. Relatively high capacitance ceramic capacitors are used as input-filter capacitors to smooth the ripple and spikes before they reach the regulator. Filter capacitors smooth, but do not eliminate the spikes.

To minimize noise, the method explained in [4] was implemented. The idea is shown in figure 6 and it is based on the addition of ferrites combined with filter capacitors. In this way, the high impedance of the ferrites at high frequencies is combined with the low impedance of the capacitors to create a resistor divider with a very high reduction factor at high frequencies.

A ferrite BLM41PG102SN1 from Murata is included at the input of the regulator, providing an impedance of 1kΩ@100MHz. An extra ferrite BLM18PG121SN1 with less impedance but lower DC impedance (only 0.05 Ω) is located at the output of the regulator. Filter capacitors selected at the output of the regulator are multilayer ceramic (MLCC), which offer very low ESR to achieve effective filtering.

The trigger system provides information about the number of channels fired for a given event. The MB collects the trigger information from the 32 channels and generates a trigger output signal for low level purposes. This is implemented in two stages. Four summing-difference amplifiers and a summing amplifier work in cascade so that every fired channel produces a contribution of -100 mV at the trigger output. As the number of channels contributing to the trigger signal is 32, the output voltage with all channels firing simultaneously is -3.2 V, that corresponds to the dynamic range of the Readout system. If no channel is fired, the trigger output vanishes. In this new version, a trimmer placed at the positive input of the second stage is used for calibration, allowing correcting any possible offset of the output. Also the slew rate of the operational amplifiers used (OPA690) was reduced to minimize the overshoot on the trigger output signal, which may give an erroneous number of fired channels. This has been easily implemented by adding a small feedback capacitor in every operational amplifier.

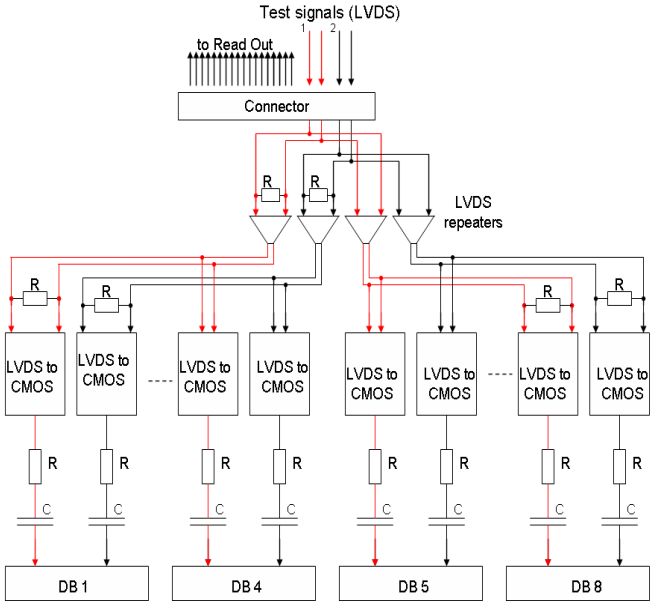

Figure 5: Test signals distribution. Test signals to even channels are represented in red and the ones for odd channels in black.

The inclusion of a temperature sensor on the MB allows the detection temperature variations, which could be a sign of warning, preventing failures on the system. At first a SPI temperature sensor was considered, in order to take advantage of the SPI protocol already implemented. However, the impossibility of including the temperature sensor into the DAC chain forced us to explore new options. Eventually it was decided the use of the temperature sensor DS18B20. The DS18B20 is a digital thermometer featuring ±0.5°C accuracy over a -10°C to +85°C range. Data is read out over a 1-Wire serial bus with 9 to 12 bits of resolution (user-programmable). Thus, it only requires one extra pin on the MB-TRB connector, and is completely independent of the SPI system. For simplicity this signal is not converted into LVDS for transmission because it is not a specially sensitive or critical signal.

The Readout system that reads the timing signals coming from the MB is a custom board consisting in a multi-purpose 128-channel Time to Digital Converter (TDC) electronics based on the HPTDC chip with functionality DAQ on-board [5].

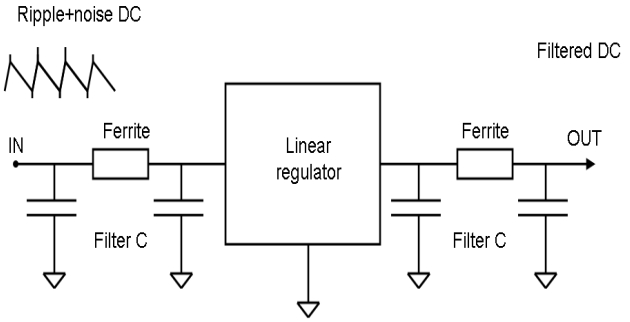

Figure 6: Ripple/noise filtering scheme.

III. RESULTS OBTAINED WITH THE CURRENT SYSTEM

A prototype setup of 24 RPC cells was mounted into the HADES frame and tested at GSI with particles coming from reactions of 1.5 AGeV 12C beam, of different intensities on a Pb target [6]. The cells were staggered in two layers: 13 cells in the front layer (upstream) and 11 cells in the back layer (downstream). One of the most important aims of this test was the time measurement of the whole detector-FEE-TRB chain. The existing overlap between cells in two layers made it possible. Due to the small distance between layers the variations in the time-of-flight of different particles travelling across the space between them is negligible compared to the time jitter of the full electronic chain. Then, subtracting the time-of-flight values of a particle going through two overlapped cells it is possible to get an estimation of the time resolution. The results of the time resolution measurements are shown in figure 7.

Since the charge was also measured, this information was used to perform a procedure called "slewing correction" to the time resolution measurement to reduce the walk error. The results, shown in figure 8, reveal a light improvement of the time resolution.

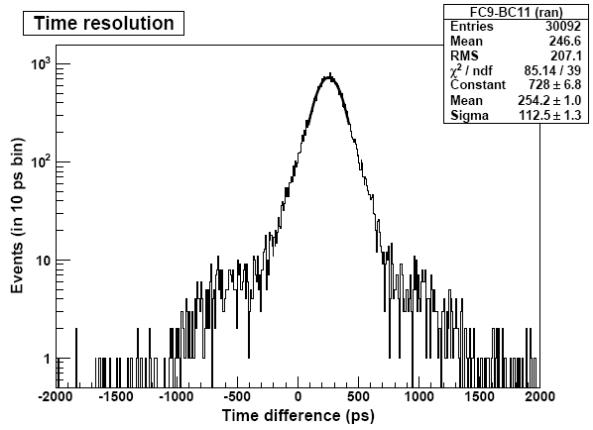

Figure 7: Time resolution measured of the electronics (80 ps).

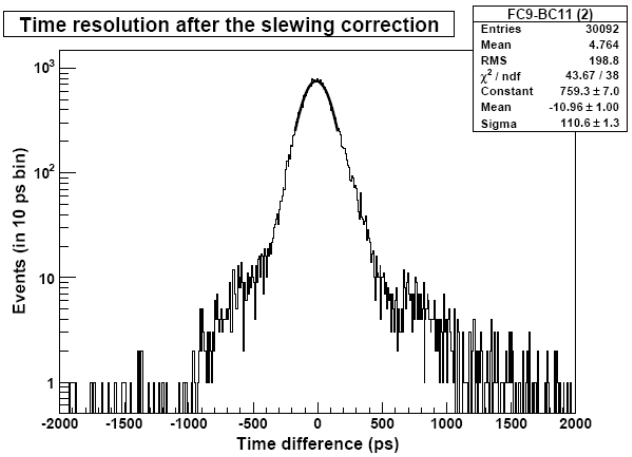

Figure 8: Time resolution measured of the electronics after slewing correction (77 ps).

IV. PROGRESS AND OUTLOOK

The results obtained with the current version of the Front-End electronics show a very good performance and fit the requirements of the HADES RPC wall. However, some improvements were implemented with the aim of improving the response and stability of the charge measurement and also to reduce power consumption on the DB, and to increase noise rejection and provide better grounding on the MB.

On the DB, the charge measurement was modified by means of 1) replacing the amplifier by a new one of 30 dB gain 2) by including a second integration to improve linearity.

The new amplifier used is the BGM1013, a monolithic device from Philips that features 31 dB gain at 2.2 GHz. The wide band of the amplifier guarantees the RPC signal integrity in the amplification, while the high gain provides better charge resolution for RPC signals of low charge.

On the other hand, the second integration, implemented with a simple passive RC network, provides an opposite response to the first integration (which was inverted by means of an operational amplifier). This allows to linearize the exponential response of the first integration by adjusting the timing constant of the passive integrator.

This improvement was implemented in such a way that the output of the second integrator is connected directly to the latch enable of the leading edge discriminator, which provides as a benefit the implementation of the charge measurement without the need of a second comparator, achieving a reduction of the power consumption on the DB of 30% respect to the previous version.

The MB was also modified in two ways: first, by adding common mode filters and second, by including a cooper ground plane at the bottom side of the board.

The common mode filters used are the BNX-022 from Murata, and are located at the input power connector of every voltage supply. The reason for this update was the aim of increasing the noise rejection on the MB, that despite of having regulators and EMI filters, did not have any protection for common mode noise. The common mode noise [7] is propagated to the load not only through the power line path but also through the ground path, and for this reason

differential filters (RC, LC) and regulators are not effective against this kind of noise.

The copper plane included at the bottom side of the MB is a way to improve the grounding of the Front-End electronics to the detector. This function could also be accomplished by increasing the number of screws attached to the detector, but this was not possible due to the presence of copper traces on the PCB that could not be avoided. Thus, the copper area was attached to the detector metallic box with the help of a gasket, reducing the impedance of the ground of the Front-End respect to the ground of the detector. Any existing impedance between these two grounds could behave as common impedance, representing a possible source of noise.

Regarding the other two main systems that take part of the electronics for the HADES RPC wall, an update of the Readout system is in progress, and the power supply system is being developed.

A general-purpose trigger and readout board with on-board DAQ functionality is being developed for the Readout system. It contains the 128-channel TDC based on the HPTDC (achieving 40 ps resolution) to read out the HADES RPC detector, as in the previous version, but the new version [8] has been designed to be detector independent and thus may serve for any high speed data acquisition by using a flexible add-on board concept.

Custom power supply boards will provide the required voltages to the Front-End electronics: +5V, -5V and +3.3V. This power supply boards are based on commercial switching DC/DC modules that are conveniently filtered (common and differential modes) to obtain clean power supply voltages. This supply boards will also contain sensing capabilities to implement the low voltage monitoring system. This monitoring system is based on a single computer on-chip that sends the relevant event data to the mass storage system via Ethernet.

V. REFERENCES

[1] D. González-Díaz. PhD thesis, Universidad de Santiago de Compostela (Spain), 2006.

[2] D. Belver et al., Nucl. Phys. B158 (Proc. Suppl.), 47 (2006.;

[3] A. Gil et Al., Proceedings 12th Workshop on Electronics for LHC and Future Experiments, Valencia, 2006.

[4] J. Williams. EDN. Linear technology corp. December 05, 2005.

[5] M. Traxler et al., 128 channel high resolution TDC with integrated DAQ-system, GSI Scientific Report, 2005.

[6] P. Cabanelas, Master Thesis, Universidad de Santiago de Compostela, 2006

[7] “Understanding common mode noise”. Report G019.A (4/99). Pulse, TECHNITROL Co.

[8] "A General Purpose Trigger and Readout Board for HADES and FAIR-Experiments" accepted for publication by IEEE Transactions on Nuclear Science, 2007.