Proposal, development and test of an analog front-end electronic board for the Nemo telescope.

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Development, realization and test of an electronic data acquisition-board for the NEMO (NEutrino Mediterranean Observatory) collaboration are described in this work. The collaboration is involved in R&D for the construction of a deep underwater kmˆ3 scale Cherenkov neutrino telescope in the Mediterranean sea. Thousands of optical modules are equipped with a photo multiplier tube and an electronic circuit for data acquisition and transmission. This work shows a possible solution for the front-end board compatible with an analog sampling chip; this data acquisition system has been developed to be fully compliant with the data transmission system of the Nemo Phase-1 apparatus.

Summary

The data acquisition board described in this work is a prototypal front-end for the Cerenkov neutrino telescope Nemo. The detector involves thousands of Optical Modules (hereafter OM) spread over a volume of 1 Kmˆ3 and supported by a three-dimensional structure. Each OM is equipped by a photo multiplier tube (PMT) for Cerenkov light detection and an electronic circuit for data acquisition and transmission (DAQ-Board). The proposed structure of the detector is made up of a 9x9 towers grid; a tower is a mechanical support made of 18 superimposed floors hosting 4 OMs each. The spacing between the towers and the width of the floors will grant the coverage of the entire one Kmˆ3 volume. The Italian proposed site for the telescope is the southern Ionian Sea near the coast of Capo Passero, Sicily.

Nowadays a test apparatus called Nemo Phase-1 is running. This structure involves a single tower made up of 4 floors only and it has been deployed few kilometers away from the coast of Catania.

The data acquisition board proposed works with a full custom ASIC called LIRA (acronym from the Italian for "Analog Delay Line"), used for the PMT waveform analog sampling. The aim of this project is to develop a front-end board integrating the analog sampling technology over the present data transmission system; even the layout of the board meets the mechanical constraints imposed by the Phase-1 OM specifications. The main components of the proposed solution are: the chip for the analog sampling, a pipelined ADC for samples conversion at 20 MHz, and a programmable logic device for the acquisition process control and data transmission to a floor data-concentrator (Floor Control Module).

The low power analog sampler supports rates up to 200MS/s and embeds an over-threshold trigger and signal classifier. This chip, in normal operating condition, consumes 150 mW for a 50 KHz event rate. The sampler stores each photo-electron signal into two parallel FIFOs, one acquiring the PMT anode and the other acquiring the last dynode signal to grant a higher dynamic extension. Once the sampler FIFO is full, data can be read and converted at 20MHz by the pipelined ADC. The real time classification of the signal permits to choose properly the analog channel that should be digitized: a high dynamic pulse will be read from the low-gain dynode channel; on the opposite, a low signal will be read from the anodic FIFO sampler. Digital samples are then temporarily stored inside an FPGA: a programmable digital logic device responsible for controlling the sampling process, transferring data and executing remote commands.

The board has then been tested simulating a PMT signal with an arbitrary function generator and acquiring the sampled digital waveform on a PC using a logic state analyzer. The firmware for the interface towards the FCM has been simulated on a PC

while the hardware line transceivers have been tested on board to inspect signal integrity. Nowadays we are setting up a more exhaustive test bench on the actual data acquisition system.

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