



System Design of the ATLAS Absolute Luminosity Monitor

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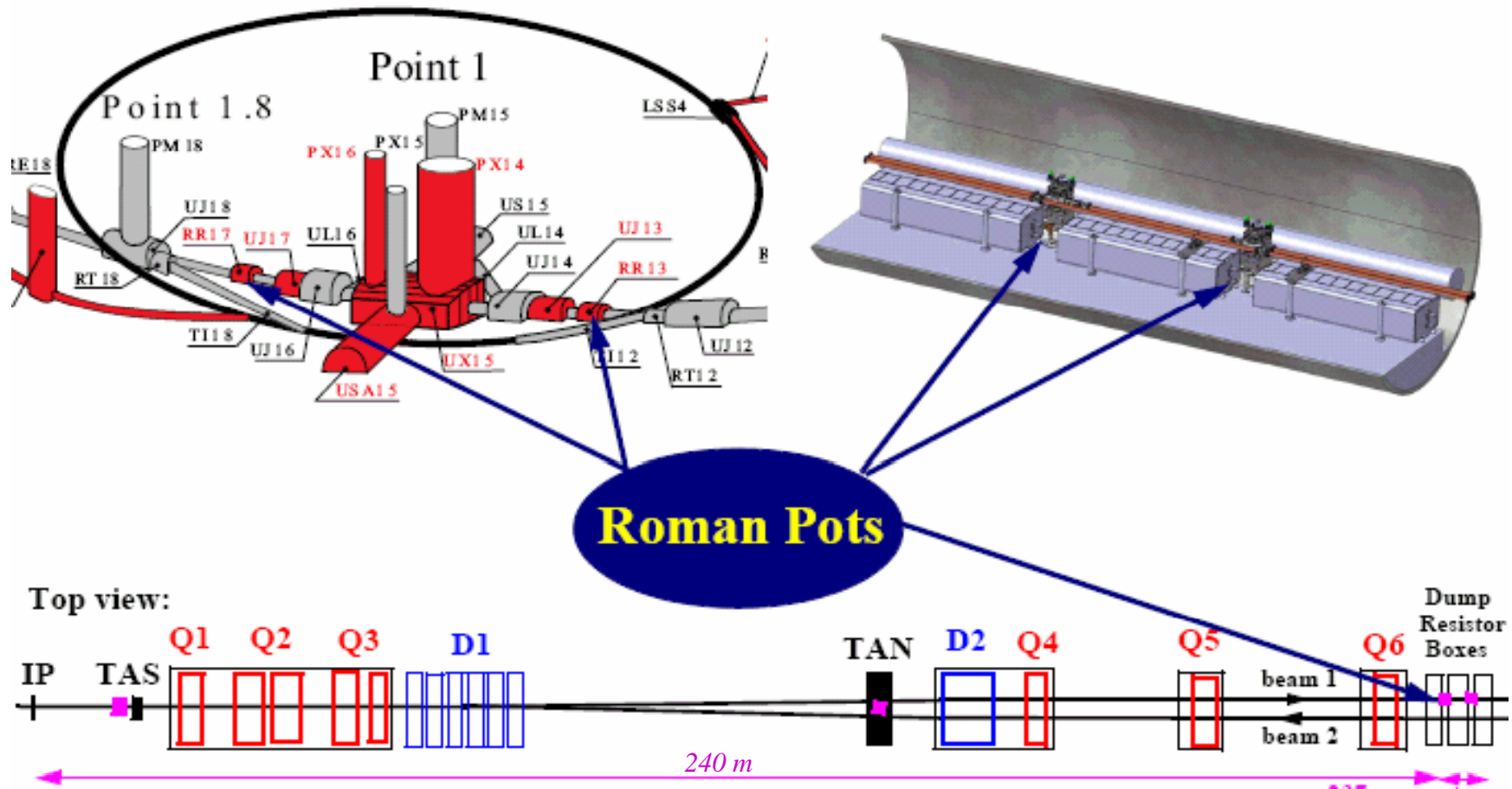
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Roman Pot locations



ALFA: Absolute Luminosity For ATLAS



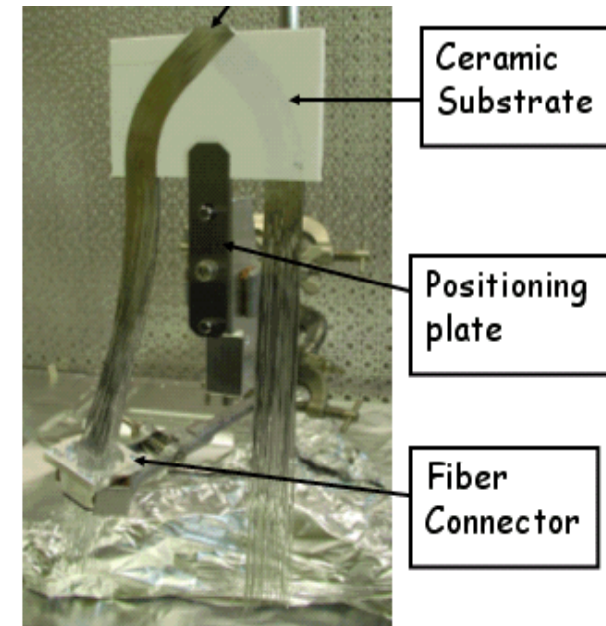
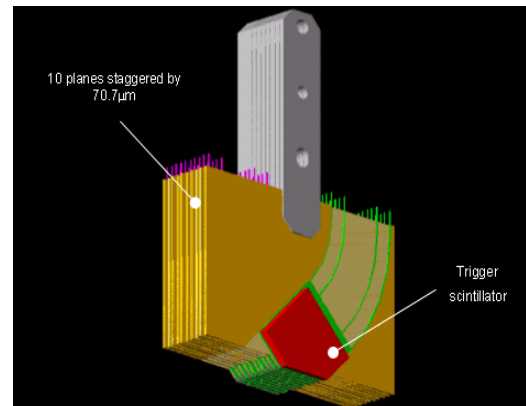
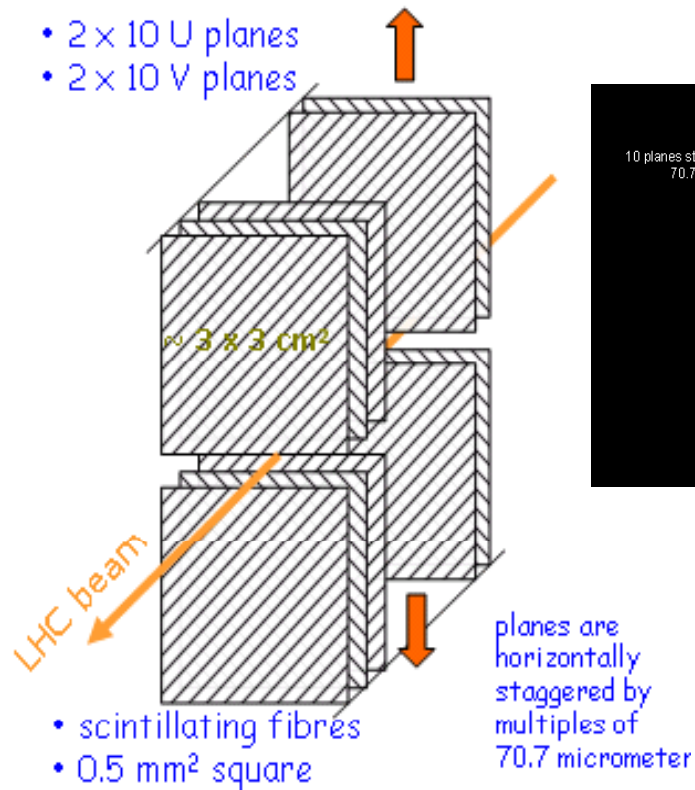


The ALFA Scintillating Fiber Tracker



Concept

- 2×10 U planes
- 2×10 V planes



The 20x64 fibres are read out by MA-PMT (R7600-M64 from Hamamatsu)



The Roman Pot Assembly



The Roman Pot Unit

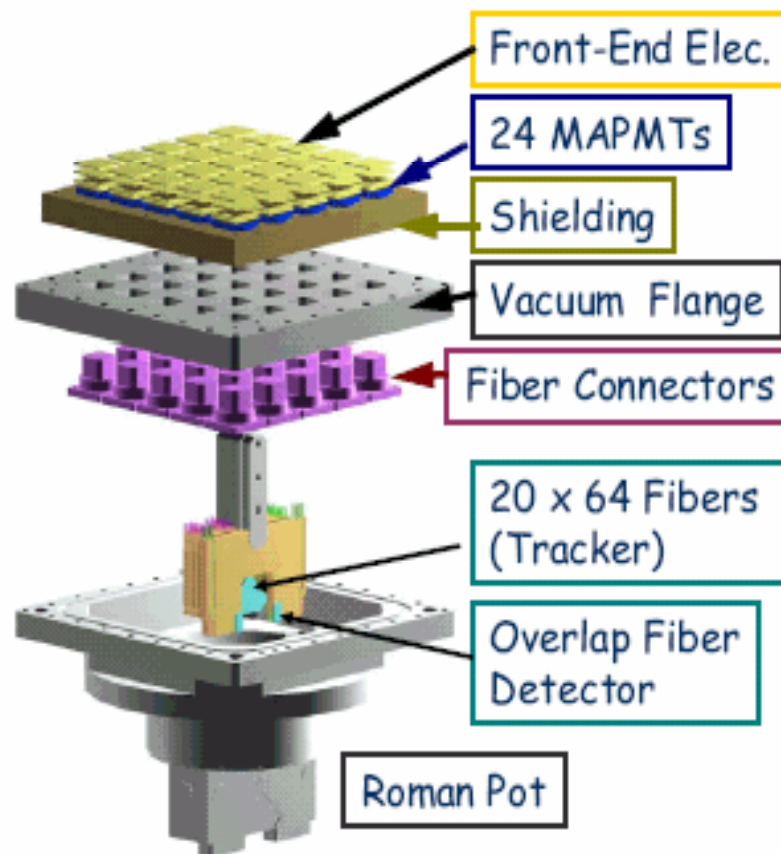
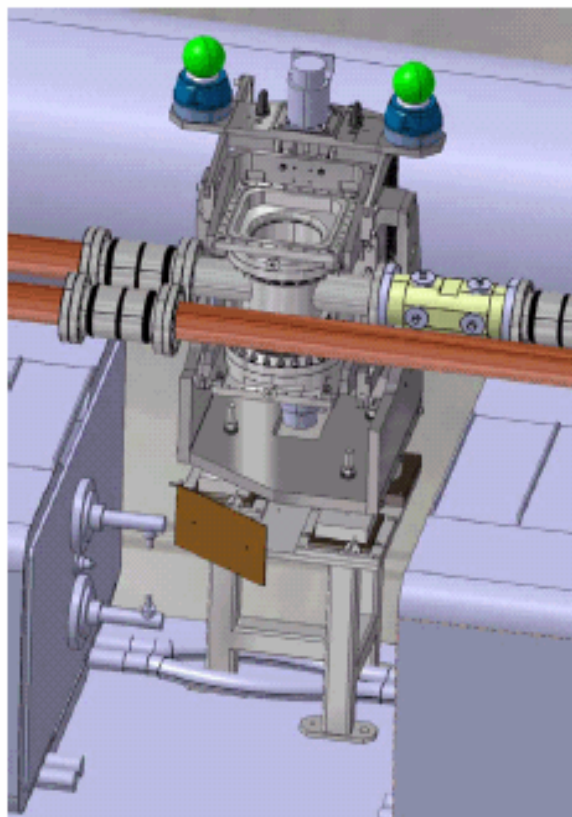
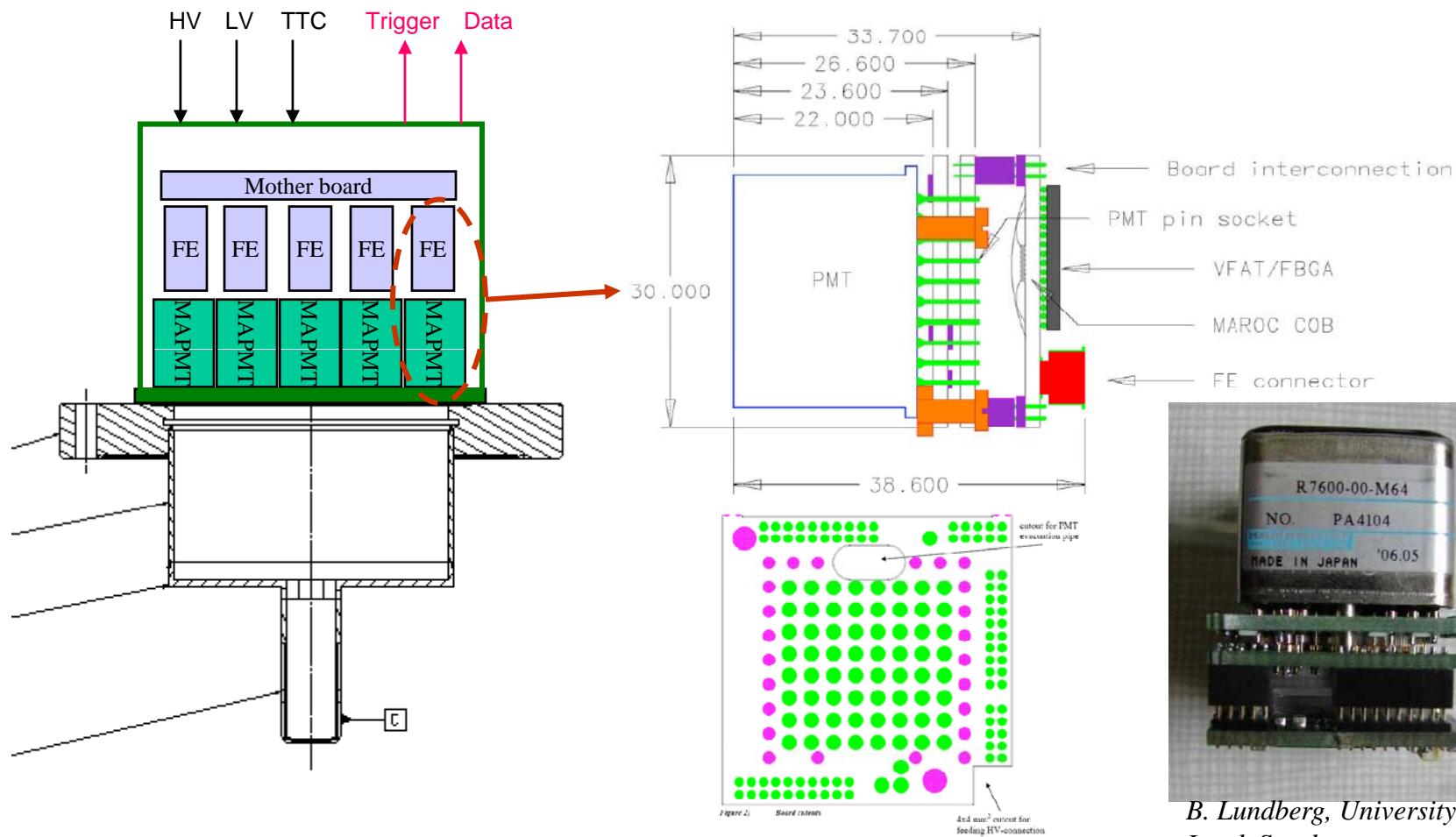




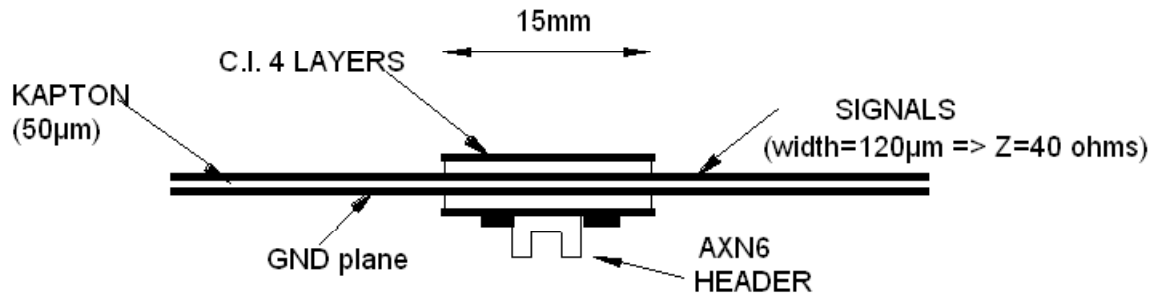
Photo Multiplier Front-End (PMF)



B. Lundberg, University of Lund, Sweden.



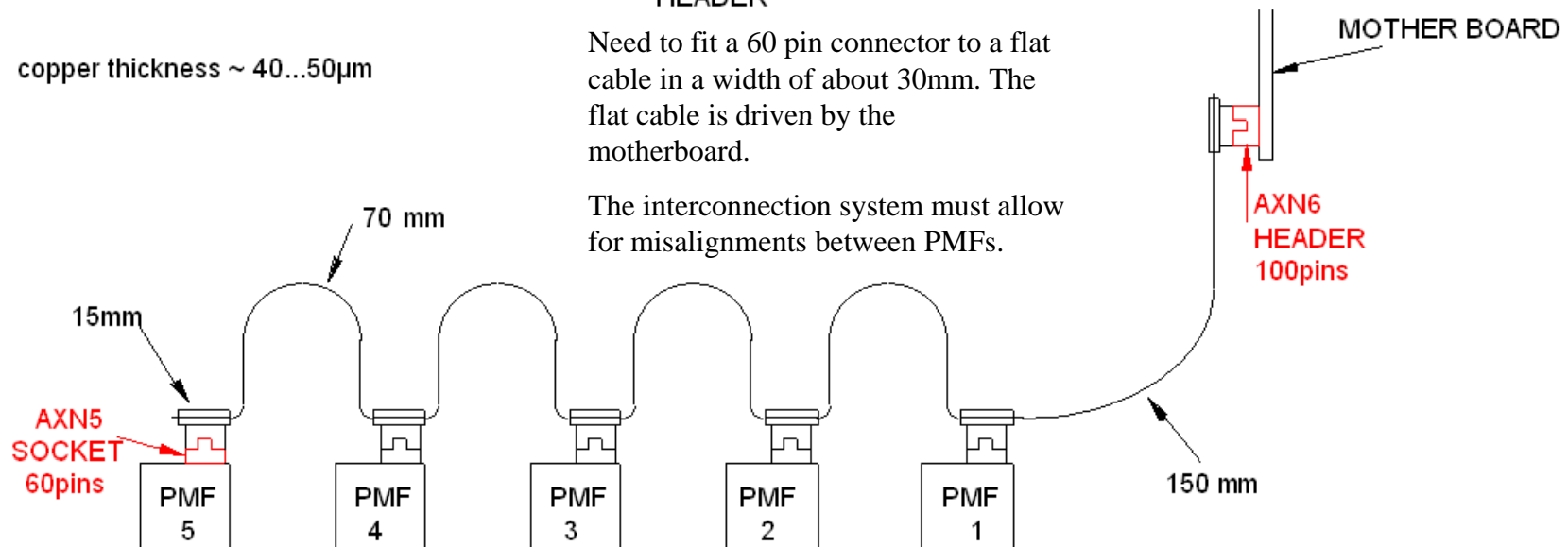
PMF Kapton Interconnections



First version based on flat cable tested in 2006. Kapton interconnects is designed and under construction at LAL-Orsay.

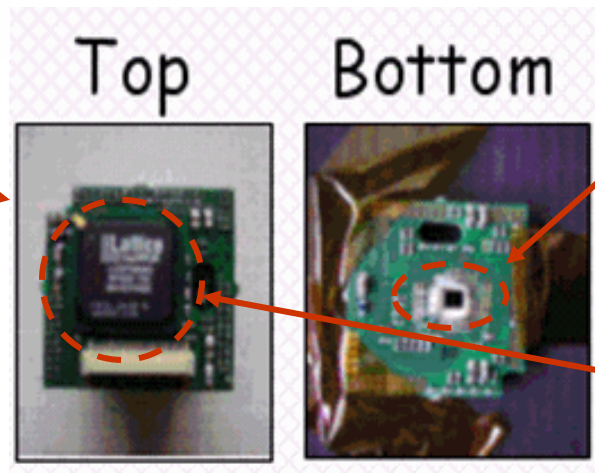
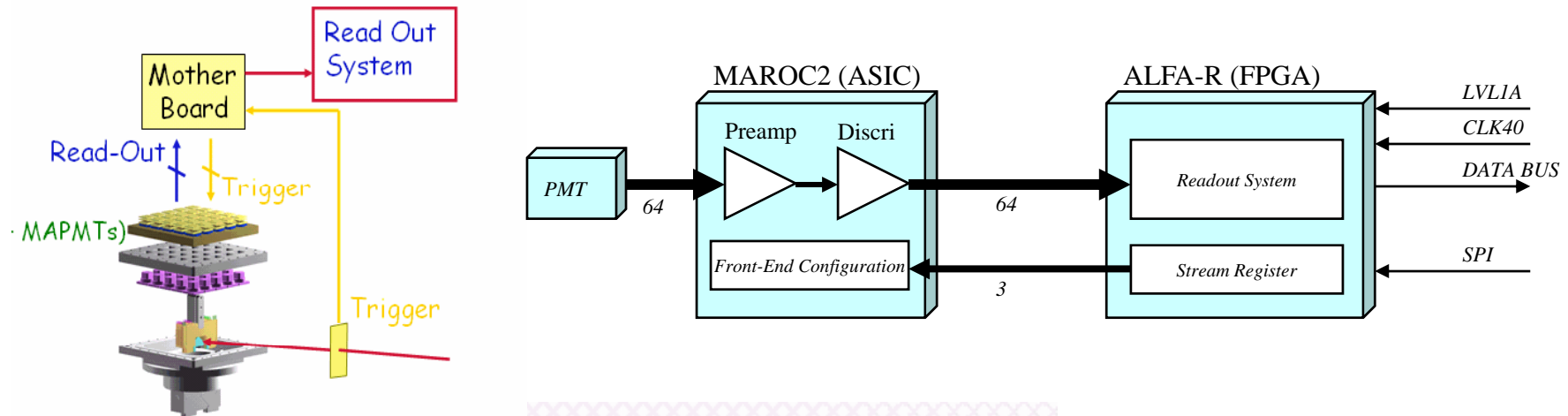
Need to fit a 60 pin connector to a flat cable in a width of about 30mm. The flat cable is driven by the motherboard.

The interconnection system must allow for misalignments between PMFs.





The ALFA Front-End Electronics (PMFE)

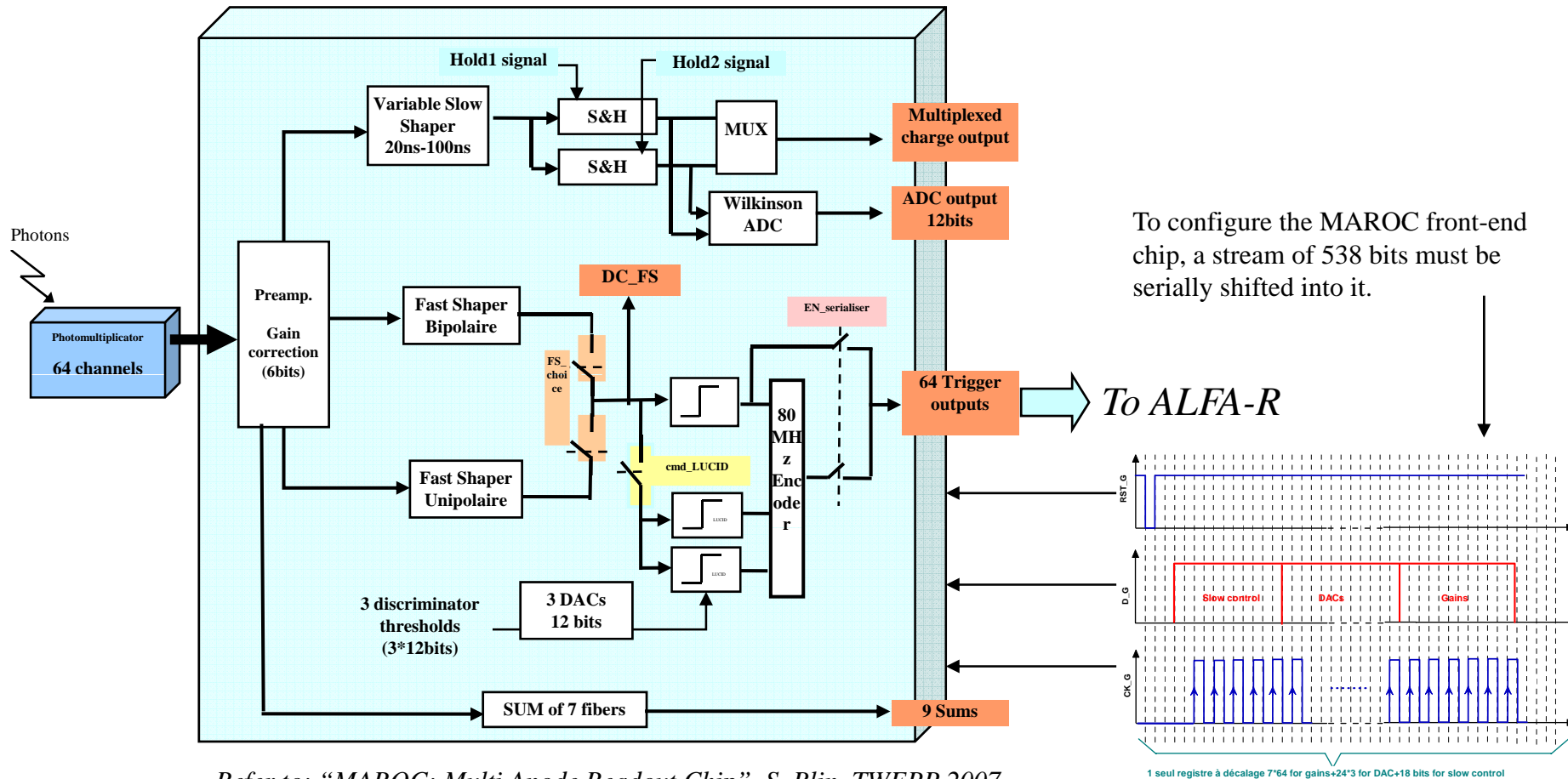


MAROC Chip bonded to PMFE

ALFA-R FPGA (BGA) on the back of the PMFE



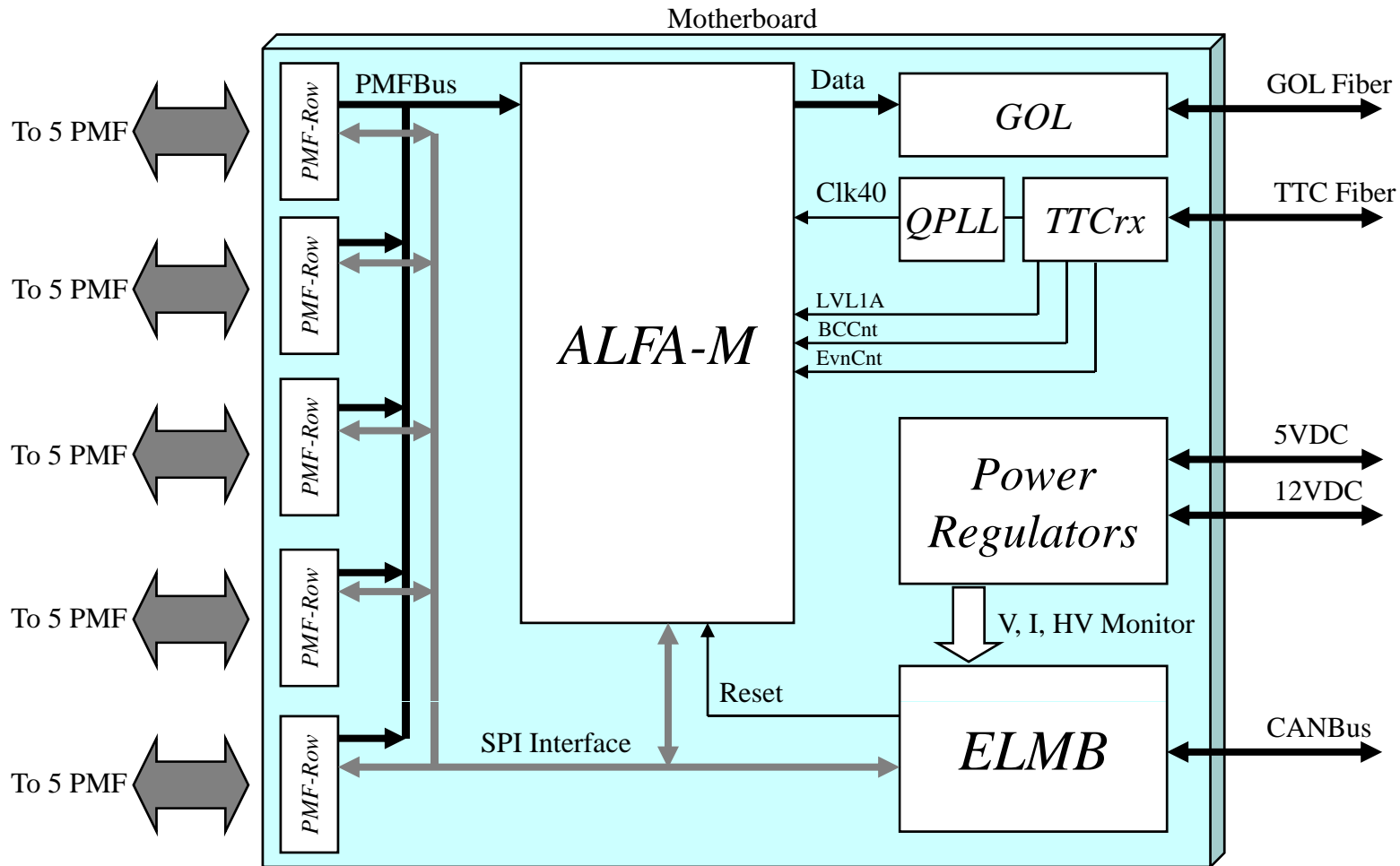
MAROC2 Front-End



Refer to: "MAROC: Multi Anode Readout Chip", S. Blin, TWEPP 2007.



ALFA Motherboard

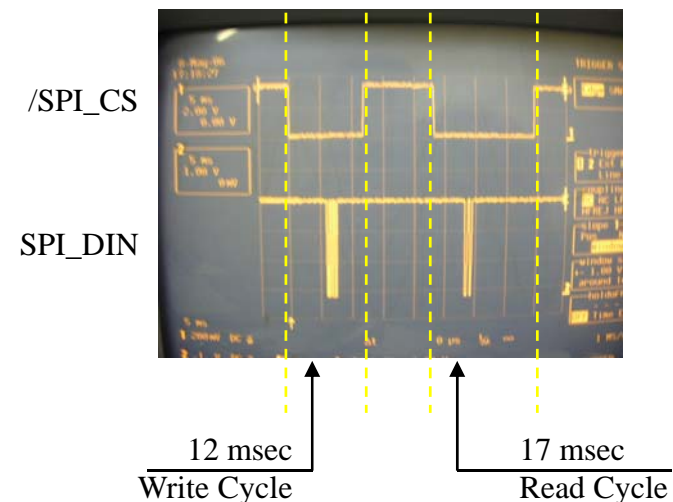
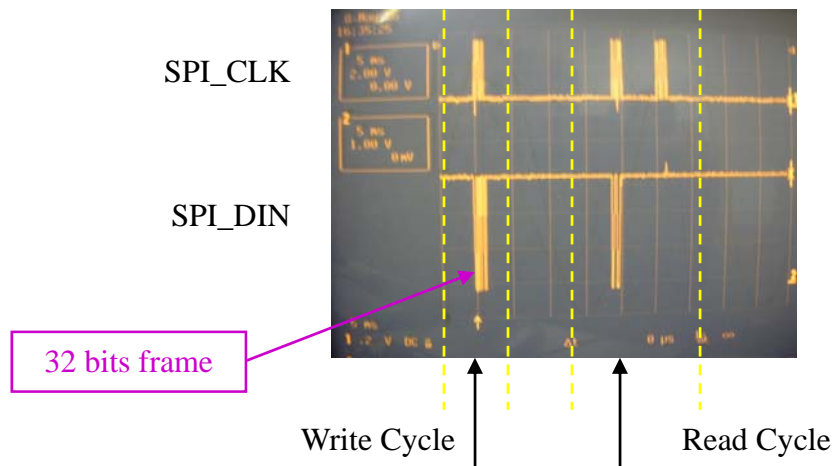




SPI Communication with an ELMB



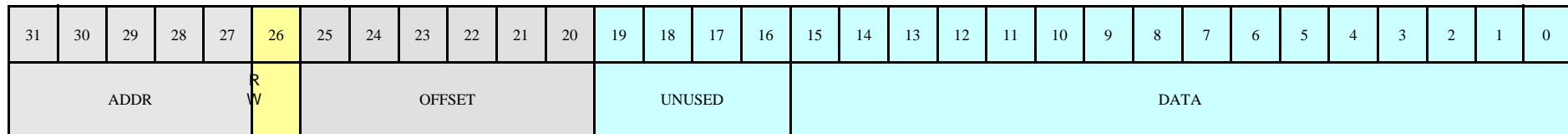
- Each PMF needs 538 bits of configuration, 25 PMFs -> 13 450 bits.
- An ELMB is provided to configure the RP front-end independently of the TTC status.
 - IO ports were discarded because of the limited bit rate (<100 bps, > 2 min. uploading).
 - SPI port was tested for a rate of 12 msec/ 32 bits frame, allowing to upload the configuration much faster (few seconds).
 - SPI port was easily implemented in ALFA-R and ALFA-M allowing to set some registers of the FPGAs and to monitor a Status register.



With the support of S. Franz from ATLAS DCS.



SPI Frame Format

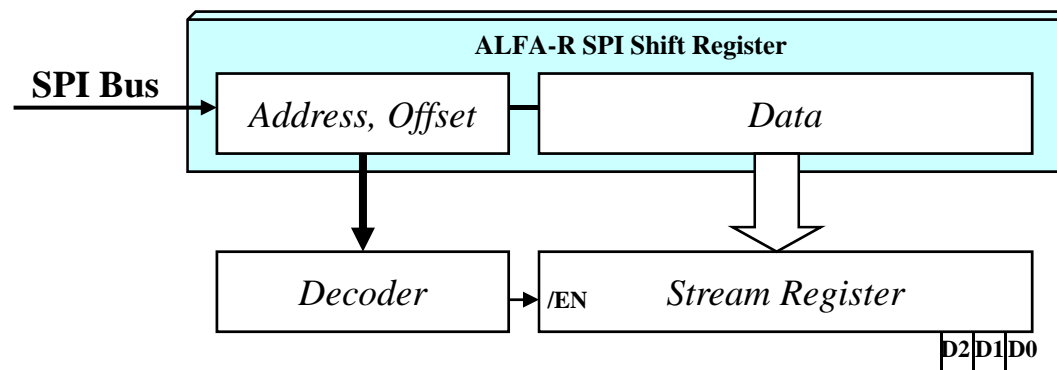


<u>ADDR</u>	<u>Addressed Structure</u> 0: Motherboard 1 to 25: PMF 31: Broadcast to all PMFs
<u>R/W</u>	<u>Read/WriteFlag</u> 0: Request register data 1: Set register data
<u>OFFSET</u>	<u>Register Offset</u> Pointer to a given register of the addressed structure
<u>DATA</u>	<u>Data Field</u> Data as specified for addressed register.

- Motherboard registers:
 - Control, Status.
- PMF registers:
 - Control, Status.
 - Masks.
 - Configuration Stream.



Stream Configuration of PMFs

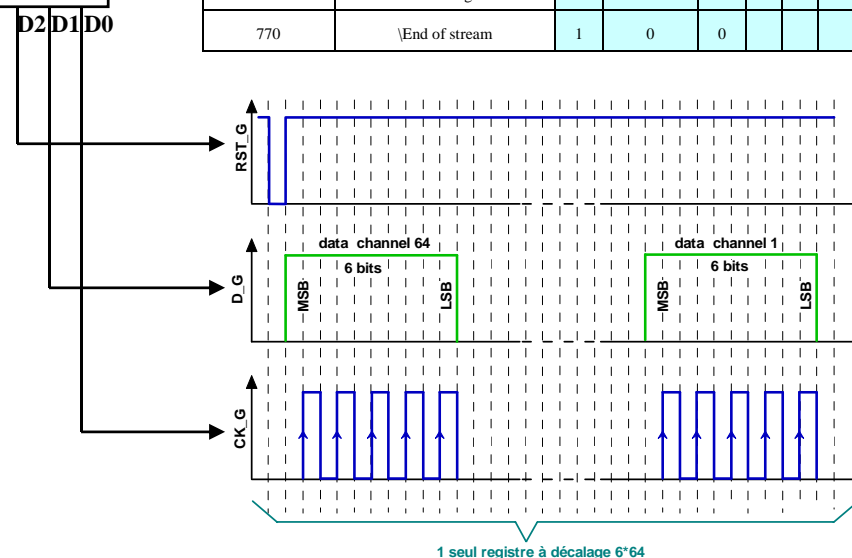


Word count	Cycle	5	4	3	2	1	0
1	Reset Low	0	0	0			
2	Reset High + MSB64	1	CH64.5	0			
3	Clock high to validate MSB64	1	CH64.5	1			
4	Clock low and next bit	1	CH64.4	0			
5	Clock high	1	CH64.4	1			
...							
768	Clock low and last bit	1	CH1.0	0			
769	Clock high	1	CH1.0	1			
770	\End of stream	1	0	0			

The MAROC front-end chip is configured through a serial interface: a reset pulse initiates the configuration, then all the configuration bits are shifted and validated by a clock.

The configuration is sent on SPI from the ELMB, a stream of 3 bits configuration vectors are passed.

The entire configuration is passed within few seconds.



Refer to: "FPGA based Readout Logic of the Front-end Electronics of the Absolute Luminosity Monitor", W. Iwanski, TWEPP 2007.



PMFs Configuration from DCS



The main interface is divided into several sections:

- PMF parameters:** A table with columns for Gain, Mirror, and Thermo, indexed 1 to 4. Below the table are buttons for 'Set gains', 'Set mirrors', 'Set Thermos', 'Reinit to default values', and 'Set as default values'. A 'Create config file' button is followed by a text input field.
- Flags:** Contains buttons for 'TTC Reset', 'Hard reset', 'Soft reset', and 'GOL reset'. A callout box points to these buttons with the text 'Reset commands for FPGA'.
- Configuration:** Includes 'Selected PMF' and 'All PMFs' buttons. Below are checkboxes for 'Gain' and 'DAC (Mirror and Thermo)'. A callout box points to these buttons with the text 'Launch configuration of PMF(s)'.
- Copy config from selected PMF:** Features a 'to:' dropdown menu and a 'Set' button. A callout box points to this section with the text 'Tool to copy configuration from one PMF to another one'.
- Manual commands:** Contains a 'Launch interface' button. A callout box points to this button with the text 'Write/read commands'.
- Status:** Shows indicators for 'OPC server' and 'ELMB'.

Callout boxes on the left side of the interface:

- 'Tools to prepare the setup of the PMFs' points to the PMF parameters table.
- 'Tool to store configuration in text file' points to the 'Create config file' button.
- 'Status of software / hardware' points to the 'Status' section.

A secondary window titled 'QuickTest: FPGA register set up' is shown on the right, with an arrow pointing from the 'Launch interface' button to it. This window contains:

- SPI Clock:** 'Clock period' set to 20 us, with 'Rising' edge selected.
- Write Data:** A 'Send command' button and a table with columns 'Chip', 'Register', and 'Data'. The table contains: Chip: 01010, Register: 1, Data: 001100 0000 1111000011110000.
- Read Data:** A 'Send command' button and a table with columns 'Chip', 'Register', and 'Data'. The table contains: Chip: 01010, Register: 0, Data: 001100 0000 1111111111111111.

With the support of S. Franz from ATLAS DCS.



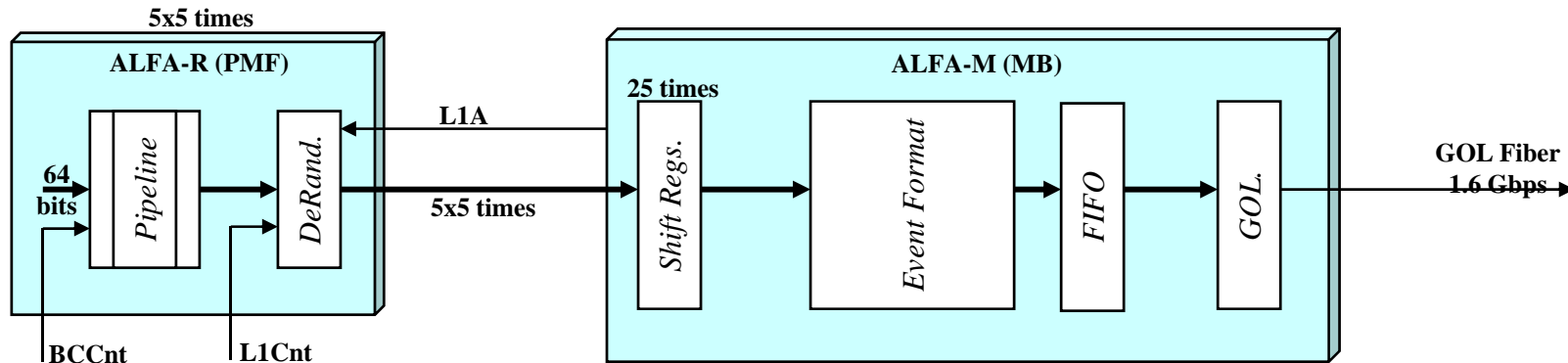
Status Register of Motherboard



- The *Status register* is the only register on the ALFA-M FPGA available in the DCS through the SPI port of the ELMB.
- It allows monitoring the status of key elements in the system:
 - Bit 15 – Test_Mode: indicates if the ALFA-M is running a test sequence.
 - Bit 14 – GOL_Ready: if set, the GOL is ready to transmit data.
 - Bit 13 – TTC_Ready: if set, the TTC is receiving signal and is driving the clock.
 - Bit 12 – QPLL_Error: if set, the QPLL is not initialized correctly.
 - Bit 11 – QPLL_Lock: if set, the QPLL is driving a stabilized clock on a locked phased.



Data Transmission



- Data (64 bits) is stored at 40MHz in a pipeline together with a local BC counter (4 bits).
- When L1A is driven, the derandomizer fetches the event from the pipeline, and it adds L1 counter information (3 bits).
- The 71 bits stored in the derandomizer are move serially at 40 MHz into a shift register of the motherboard.
- The L1A process requires about 80 clock cycles.

- The content of the 25 shift registers is combined together to form.
- BCCnt and EvCnt are compared to validate the data of each register.
- A framed event is built with header, data and end of frame 32 bits words.
- The event' words are pushed into an output FIFO.
- The GOL fetches the data available in the FIFO and transmits it over the fiber.

- The framed event can be received by any GOL compatible receiver.
- For testbeams, a FILAR card plugged into a PC is used.
- In ATLAS, a GOL compatible ROD will be used to build ATLAS events from the eight incoming fibers.

Refer to: "FPGA based Readout Logic of the Front-end Electronics of the Absolute Luminosity Monitor", W. Iwanski, TWEPP 2007.



Framed Data



- The data from each PMF validated by a L1A signal is framed to form an event by the ALFA-M FPGA:
 - Fixed SOF and EOF words delimit the beginning and the end of the frame.
 - BCID and EVNTCNT from the TTCrx chip is appended.
 - The error flags that resulted from the comparison of local BC and Event counters are appended.
 - The number of PMFs that conform the setup is appended.
 - All PMF information (2 words per PMF) follows.
 - Finally a parity word is appended for error tracking on the back-end.

	WORD	Byte 4	Byte 3	Byte 2	Byte 1
1	SOF	0xB0	0xF0	0x00	0x00
2	BCID	UNUSED[31..12]			BCID[11..0]
3	EVCNT	UNUSED[31..24]	EVCNT[23..0]		
4	PMFERR	UNUSED[31..25]	PMFERR[24..0]		
5	NPMF	UNUSED[31..8]			NPMF[7..0]
6	PMF1L	PMF1[31..0]			
7	PMF1H	PMF1[63..32]			
	...	Next PMFs data			
6 + (NPMF*2)	PARITY	Bitwise exclusive Or of all previous words except SOF			
7 + (NPMF*2)	EOF	0xE0	0xF0	0x00	0x00



Testbeam at CERN October 2006



2x2x64 + Final Trig.
Detectors

- Two ALFA trackers.
- Overlap Detectors

Beam

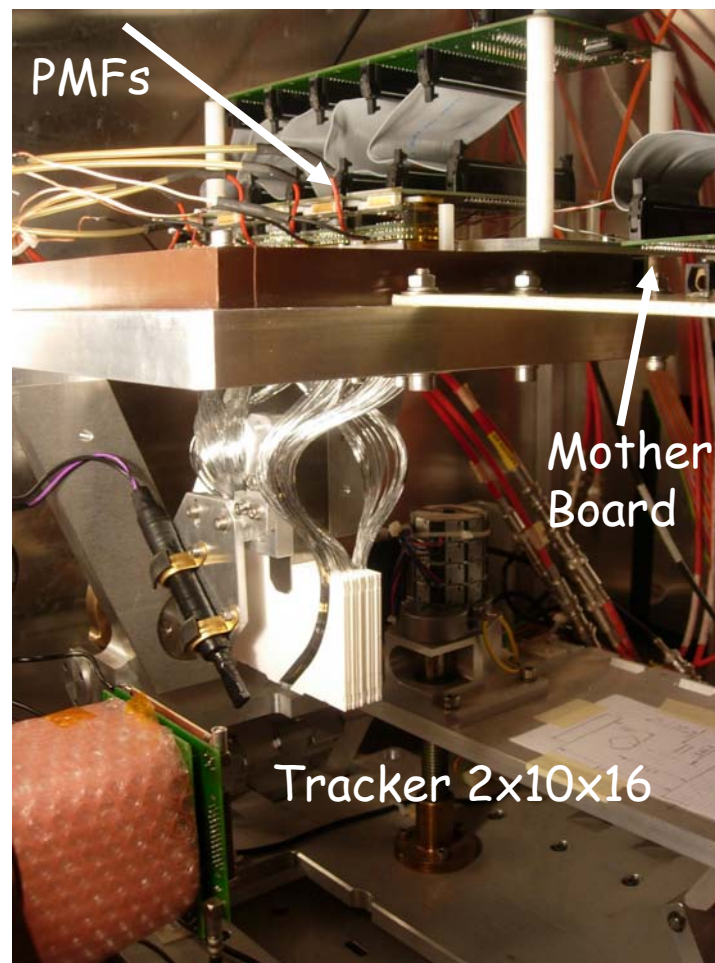
- 230 GeV protons ($\pi^{+/-}$)

Setup

- 5 x PMF - Motherboard - FILAR PC



Overlap Detectors





Conclusions



- A prototype for the front-end electronics of the ATLAS Roman Pots was built and successfully tested on a testbeam in 2006, new version is under development right now.
- A readout chain was designed to handle the data of 25 front-end chips and to send it into a single GOL fiber.
- The system is independently controlled by an embedded ELMB that allows full integration and reliable control from DCS.
- A data format was defined and is embedded on a FPGA, providing a data flow that can be handled in a ROD.