System Design of the ATLAS Absolute Luminosity Monitor

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Abstract

The ATLAS absolute luminosity monitor is composed of 8 roman pots symmetrically located in the LHC tunnel. Each pot contains 23 multi anode photomultiplier tubes, and each one of those is fitted with a front-end assembly called PMF. A PMF provides the high voltage biasing of the tube, the front-end readout chip and the readout logic in a very compact arrangement. The 25 PMFs contained in one roman pot are connected to a motherboard used as an interface to the back-end electronics. The system allows to configure the front-end electronics from the ATLAS detector control system and to transmit the luminosity data over Slink.

I. Introduction

The ATLAS detector will be provided with an absolute luminosity monitor (ALFA) composed of eight Roman Pots symmetrically located in the LHC tunnel (figure 1), between dump resistor boxes at 240 meters from the interaction point. The pots are arranged in pairs around the beam pipe, one located above and one below the beam.

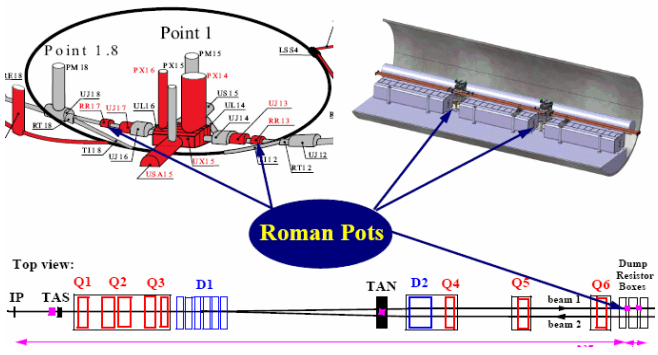

Figure 1: Location of the ATLAS Roman Pots in the LHC tunnel.

Each of these pots houses a scintillating fiber tracker that will detect the protons from elastic scattering at small angles [1]. Each fiber tracker is housed in its roman pot such that it will detect the scattered protons very close to the beam. The luminosity measurement and the requirements on the detector have been described in [2].

II. The ALFA Tracker

A fiber tracker prototype was built and tested on a test beam at CERN in October 2006 [3]. A detector plane consists of a ceramic substrate which supports on both sides Aluminum coated square fibers of 500 mm width in a so-called UV configuration, i.e. the two fiber layers have an angle of ±45◦ relative to the vertical axis. In the final detector, ten such UV planes with two times 64 fibers will be assembled (figure 2) with a relative staggering of multiples of $\sqrt{2} \cdot 50$ mm.

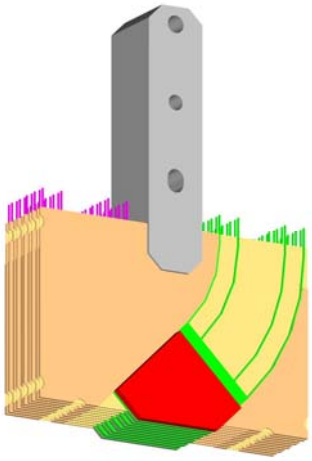

Figure 2: staggered planes of the ALFA scintillating fibers tracker.

The scintillating fibers are routed over typically 25 cm to custom designed fiber connectors with 64 channels in an 8×8 configuration, which matches precisely the segmentation of multi-anode photomultiplier tubes. The connectors fit in slots of the Roman Pot vacuum flange on the top (air) side of which are mounted the MAPMTs with their front-end electronics (figure 3) [3].

III. Front-End Assembly

The light from each fiber of the tracker is detected by 23 multi anode photomultiplier tubes, arranged on a 5×5 slots matrix in the vacuum flange (figure 3). Each MAPMT is coupled to a very compact photomultiplier front-end assembly (PMF), which performs the front-end signal processing for each of the fibers (figure 4).

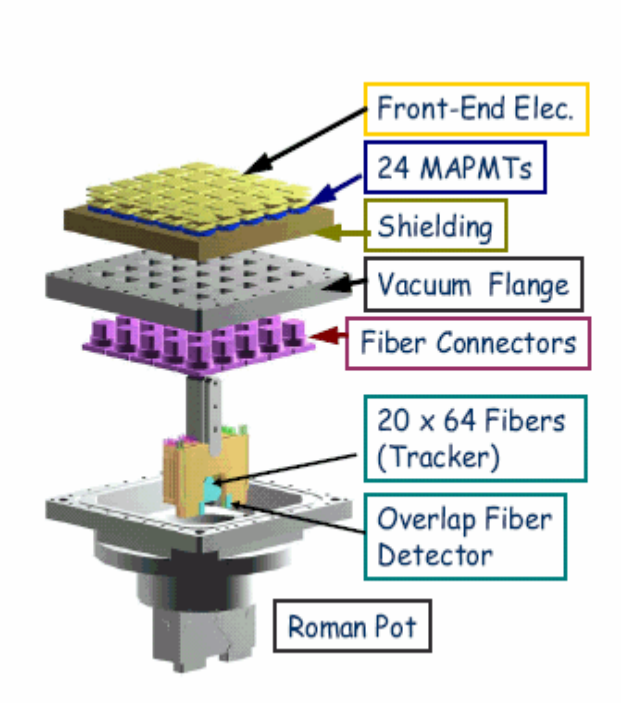

Figure 3: arrangement of the ALFA tracker with the front-end electronics inside a Roman Pot.

The front–end electronics must be fitted in a tight volume inside the Roman Pot. Because of this the PMF front-end electronics is mounted in the form of three staggered boards. The first board provides the high voltage distribution to the dynodes of the MAPMT that is biased around 1kV. This high voltage board is fitted with through-hole sockets such that the MAPMT is simply plugged into it. A socket adaptor board is plugged on top of the high voltage divider board, to redistribute the MAPMT pins matrix to a set of edge connectors that are located on the edge of the assembly. The transition board is provided with contacts sockets that allow here also to plug the MAPMT pins without soldered connections. The transition board allows then to plug the third board that contains the front end electronics. This arrangement allows plugging a third board underneath the adaptor that holds the front-end ASIC (MAROC) used to preamplify and to discriminate the pulses [4].

Figure 4: photomultiplier front-end module (PMF).

The 64 signals of the MAPMT enter the MAROC front-end chip where they are first preamplfied and shaped, and subsequently discriminated (figure 5). The gain of the preamplifier is programmable with 6 bits. The MAROC ASIC is provided with a variable slow shaper used for multiplexed charge sampling which is not used by the PMF, and with a fast CRRC bipolar shaper with 15 nsec shaping time followed by a programmable discriminator. The threshold is set by an internal 10 bit DAC composed by a 4 bits thermometer DAC allowing coarse tuning (200 mV per step) and a 7 bits mirror DAC used for fine tuning (3 mV per step). A trigger output is produced [4]. The gain and the threshold settings are configured in the MAROC ASIC through a serial interface.

The trigger outputs are fed into the front-end FPGA (ALFA-R) that implements the pipelining and the serial transmission of the 64 bits pattern into a motherboard, under the control of Level 1 trigger signals.

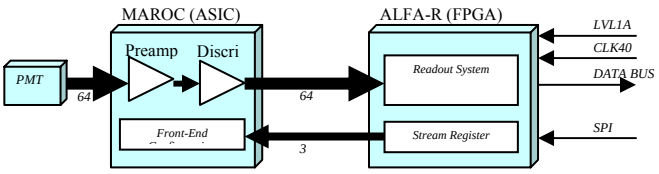

Figure 5: architecture of the front-end readout implemented on the front-end board of the PMF.

The MAROC chip is bonded on the fine pitch multilayered board and it is directly coupled to the readout FPGA that faces it on the back side of the board (figure 6). This assembly provides a very compact front-end block on the MAPMT area of 30 mm by 30 mm, in a total stack up of less than 40 mm (tube included). The blocks are arranged on a matrix of 5 by 5 slots provided with low voltage, high voltage and FPGA readout interfaces.

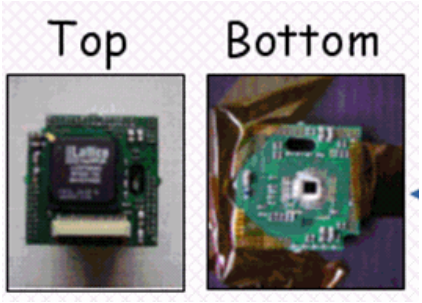

Figure 6: front-end readout COB board of the PMF.

The power and the signals needed to interface with the PMF have to fit in the limited area of the PMF front-end board, next to the FPGA (figure 6). A 60 pins 0.5mm narrow pitch, floating type connector was selected; the connector fits in 18 mm while providing the high density interconnects required by the system.

IV. Motherboard and Data Link

Five PMFs from the same row are grouped together, and there are five rows to cover the matrix of PMFs. Each of these rows is connected to a motherboard that centralizes the readout and the configuration systems.

The interconnection of the PMFs must be arranged on the width of one PMF that is 30 mm. A prototype of interconnection system was first built with a flat cable and IDC connectors mounted on adaptor boards to interface to narrow pitch connector mounted on the PMFs, but too wide for the final setup. In order to fit the interconnection system on top of the 5x5 matrix of PMFs, a flex-rigid Kapton based interconnection system is being developed. The Kapton cable will accommodate five 18 mm wide high density connectors that mate directly with the PMF connectors. A sixth header allows plugging the Kapton cable on the motherboard. The connectors are mounted on the rigid sections of the flex-rigid circuit, providing good mechanical strength for the connection. The flexible sections allow compensating the misalignments between PMFs and with the motherboard (figure 7).

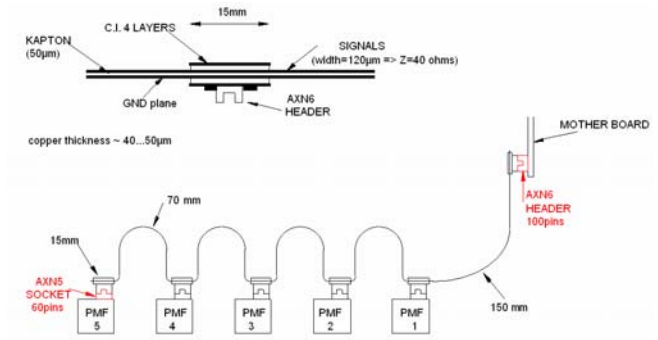

Figure 7: flex rigid Kapton circuit for the interconnection of a row of PMFs with the motherboard.

The 60 pins PMF interface implements a the power pins, a JTAG port to program the ALFA-R FPGA, a Serial Protocol Interface (SPI) to control the ALFA-R and to configure the MAROC front-end ASIC, and a serial data bus for the transmission of the data. The PMF is driven by the LHC clock of 40.08 MHz, and other signals needed to control the data flow are also provided, such as Level 1 Accept (L1A), Bunch Crossing reset and Event Counter reset of the TTC system [5].

The ALFA motherboard (figure 8) acts as a data concentrator and as configuration and control unit for the front-end PMFs. Each row of PMFs is handled separately by the ALFA-M FPGA. Upon each LVL1A trigger, the PMF assemblies deliver each a serial data stream formatted by the front-end FPGA (ALFA-R). The data streams are driven at the LHC clock rate and are collected by a readout FPGA (ALFA-M) interface located on a motherboard (figure 8). The data received from the PMFs is merged by the ALFA-M to form a data packet that is transmitted to the back-end system using a gigabit optical link transceiver based on the GOL serializer ASIC [6], operated in G-Link mode. The GOL and the ALFA-M are driven by the 40.08 MHz TTC clock, adequately stabilized by a QPLL ASIC [7]. This insures a stable transmission of the data through the GOL chip, and an accurate timing on the front-end side.

The front-end and the motherboard logic are powered by a set of radiation hard linear regulators, fed by 5VDC and 12VDC. A power monitoring circuit allows a clean startup of the motherboard chips.

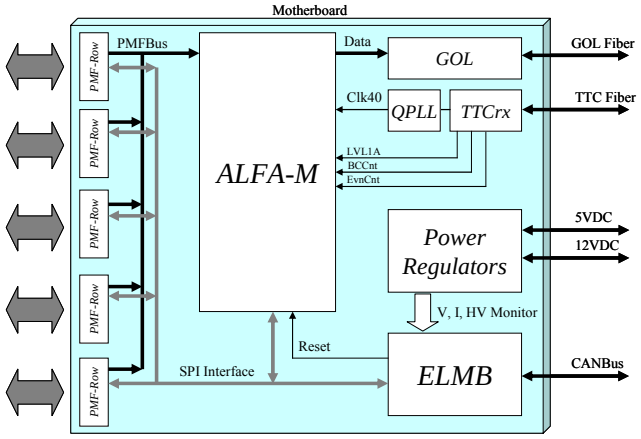

Figure 8: architecture of the ALFA motherboard.

The motherboard is equipped with a carefully designed reset logic chain that allows to handle the startup sequence during a cold startup, or when a local or a remote reset are requested. The status of the PMFs and of the motherboard circuitry is made available in the form of a status word that can be read asynchronously by the configuration and control system.

V. Configuration and Control

The whole system is configured and monitored by a standard ELMB [8], externally powered from the back-end system. This configuration allows monitoring the power parameters and the status of basic parameters such as TTC or QPLL chips, independently of the proper operation of the system, easing in this way the debugging and the remote monitoring of the system. The ELMB is the main source for asynchronous reset pulses that are hard wired to optically coupled outputs. This allows restarting remotely the system without cycling the power.

The ELMB is provided with an SPI interface that is used to broadcast the configuration commands to the PMFs, and to access the various registers of the ALFA-R and ALFA-M FPGAs. Because the SPI interface is entirely controlled by the ELMB, the status of all the system can be monitored in all circumstances, and in particular when the GOL or TTC links are down. The SPI interface allows also downloading the configuration data of the MAROC chips on the PMFs at the CANBus speed. Tests showed that it is possible to transmit a SPI frame of 32 bits in 12 msec with a CANBus link running at 250kbps; similarly a read cycle is processed in 17 msec at this same bus speed. This results in an effective configuration bit rate of almost 2.6 Kbps. The SPI interface was easily embedded into the ALFA-R FPGA.

A set of registers was defined in the ALFA-R and ALFA-M FPGAs readout logic [9]for configuration and control of the front end electronics, based on the 32 bits available on the SPI frames (figure 9). The sixteen upper bits of the frame

implement the addressing logic, the lower sixteen bits contains the data space for flags and data.

The ALFA-M on the motherboard supports a write-only control register and read-only status register. The control register allows enabling a test mode for the ALFA-M. The status register provides status information on the GOL, TTC and QPLL chips, together with the status of the test mode flag (table 1) [9].

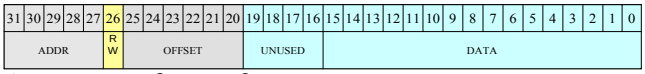

Figure 9: SPI frames format.

Bit	Control Flag	Default	Description
15	TEST_MODE	0	1 when the transmission of test vectors from ALFA-R is enabled.
14	GOL_READY	1	1 when the GOL is ready to transmit data.
13	TTC_READY	1	1 when the TTC is receiving a correct signal and is delivering the clock.
12	QPLL_ERROR	0	1 when the QPLL is not initialized.
11	QPLL_LOCK	1	1 when the QPLL delivers a stabilized clock.

Table 1: flags of the motherboard status register.

The readout logic of the ALFA-R on the PMF supports also a control and a status register. It also provides a set of mask registers and a configuration stream register, used to set up the PMFs [9].

The front-end MAROC chips need to have their gains and thresholds configured. This is done through the configuration stream register in each PMF. The data format of these configuration SPI frames was arranged in a way that maximizes the data throughput of the ELMB during the configuration cycle. To maximize the configuration speed, a stream of vectors is set up in the DCS back-end. These vectors are then transmitted by the ELMB through the SPI interface. The addressed ALFA-R FPGA latches the vectors into the stream register and applies them directly to the configuration port the MAROC chip [9].

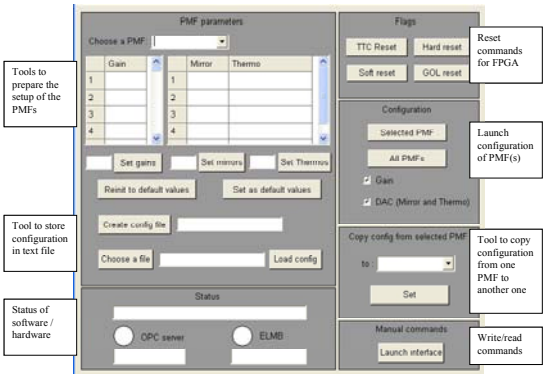

Figure 10: DCS user interface.

To handle these registers during laboratory tests and test beams, a user interface was implemented in the ATLAS DCS system (PVSS), allowing to set the configuration of the PMFs and to handle the motherboard control and status registers. This interface also provides the reset functionality that is implemented on the ELMB (figure 10).

VI. Data Transmission.

Each PMF pushes the 64 bits words, together with a local bunch crossing counter into a pipeline that is implemented in the ALFA-R at 40 MHz (figure 11). Upon reception of a level 1 accept from the TTC, the word available on the output of the pipeline is pushed in a derandomizer, together with a local event counter. The ALFA-M handles the serial transmission at 40 MHz of content of all the PMF derandomizers. Upon reception, the local bunch crossing and event counters are checked with the TTC counters; if a mismatch is detected, an error flag for the corresponding PMF is set [9].

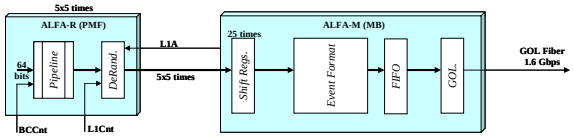

Figure 11: transmission of the PMF data.

The ALFA-M formats a data packet with the TTC counters and the PMF data. This packed is pushed in an output FIFO. The GOL chip recovers the data words and transmits them to the back end system over the optical link [9].

VII. Conclusion

The roman pots front-end system was implemented on a prototype made of a motherboard and five PMFs, readout out by a FILAR card into a PC. It was successfully tested on a test beam in October 2006. It allowed validating the control system and the readout chain, handled by a motherboard that formats and transmits the PMF data upon reception of a level 1 accept trigger. The GOL chip drives the optical transceiver using a LHC clock that is delivered by the TTC and that is stabilized by a QPLL chip. The motherboard FPGA and the TTC and GOL devices can be reset through hardwired connections to an ELMB that is separately powered by the back-end.

The serial peripheral interface of the ELMB was successfully linked to the FPGAs of the system that allowed configuring the PMFs while controlling the system directly from the DCS.

This scheme provides a convenient remote control on the system, independently of the LHC clock, that turned out to be essential for the debugging of the prototype and that will be useful once the system is installed in the LHC tunnel.

VIII. References

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