TWEPP-07 Topical Workshop on Electronics for Particle Physics

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System Design of the ATLAS Absolute Luminosity Monitor

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The ATLAS absolute luminosity monitor is composed of 8 roman pots symmetrically located in the LHC tunnel. Each pot contains 23 multi anode photomultiplier tubes, and each one of those is fitted with a front-end assembly called PMF. A PMF provides the high voltage biasing of the tube, the front-end chip and the local readout controller in a very compact arrangement. The 23 PMFs contained in one roman pot are connected to a motherboard used as an interface to the back-end electronics. The system allows to configure the front-end electronics from the ATLAS detector control system and to transmit the luminosity data over optical link.

Summary

Introduction.

The ATLAS detector will be provided with an absolute luminosity monitor composed of eight roman pots symmetrically located in the LHC tunnel at 240 meters from the interaction point. Each of these pots houses a scintillating fiber tracker (ALFA) whose light is detected by 23 multi anode photomultiplier tubes. Each MAPMT is coupled to a front-end assembly (PMF).

Front-end assembly.

Each MAPMT is biased by a high voltage divider board that is plugged straight on the tube high voltage pins using pin feed through contacts. The matrix of 64 signal pins of the tube passes through the high voltage board and reaches an adaptor board underneath, where it is then redistributed on edge connectors. This arrangement allows to plug a third board underneath the adaptor, that holds the front-end ASIC (MAROC) used to preamplify and to discriminate the pulses. The MAROC chip is directly bonded to the board and it is directly coupled to the readout FPGA that faces the ASIC on the back side of the board. This front-end assembly provides a very compact front-end block on the MAPMT area of 30 mm by 30 mm, in a total stack up of less than 40 mm (tube included). The blocks are arranged on a matrix of 5 by 5 slots provided with low voltage, high voltage and FPGA readout interfaces.

Motherboard and data link.

The PMF assemblies deliver each a serial data stream formatted by the front-end FPGA (ALFA-R). The data streams are driven at the LHC clock rate and are collected by a readout FPGA (ALFA-M) interface located on a motherboard. The 25 streams are bundled together to form a front-end packet that is transmitted to the back-end through an optical gigabit link. The link is implemented with a GOL ASIC configured in G-Link mode. The timing information is handled by a TTCrx chip on the motherboard; the system clock is stabilised with a QPLL.

The motherboard houses all the necessary low voltage radiation hard regulators that it needs and also that are needed by the PMFs.

The motherboard is equipped with a carefully designed reset logic chain that allows to handle the startup sequence during a cold startup, or when a local or a remote reset are requested. The status of the PMFs and of the motherboard circuitry is made available in the form of a status word that can be read asynchrounously by the configuration and control system.

Configuration and Control.

The motherboard and the PMFs are controlled by an independent link built with a standard ELMB. The ELMB is self powered from the back end and it allows to drive remote reset signals to the various motherboard circuits. The embedded SPI interface of the ELMB is used to communicate with the motherboard and with the PMF logic circuits. Because the SPI interface is driven at a clock rate controlled by the ELMB, the status of all the system can be monitored in all circunstances, and in particular when the GOL or TTC links are down. The SPI interface allows also to download the configuration data of the MAROC chips on the PMFs at the CANBus speed.

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