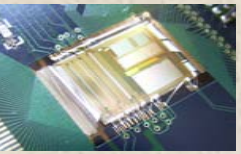
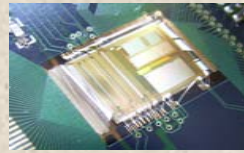


VFAT 2



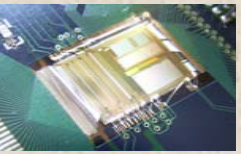
VFAT2 : A front-end system on chip providing fast trigger information, digitized data storage and formatting for the charge sensitive readout of multi-channel silicon and gas particle detectors.

P.Aspell [a], G.Anelli [a], P.Chalmet [b], J.Kaplon [a], K.Kloukinas [a], H.Mugnier [b], W.Snoeys [a]

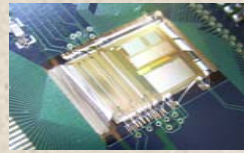
[a] CERN, 1211 Geneva 23, Switzerland

[b] C4I Le Salève Site d'Archamps 74160 France

Presented at the :
2007 TWEPP Workshop
September 3 - 7, 2007 · Prague, Czech Republic



Talk Outline



- Design Application
- VFAT2 architecture
- Design of key modules
- General design precautions
- Measured results
- Summary

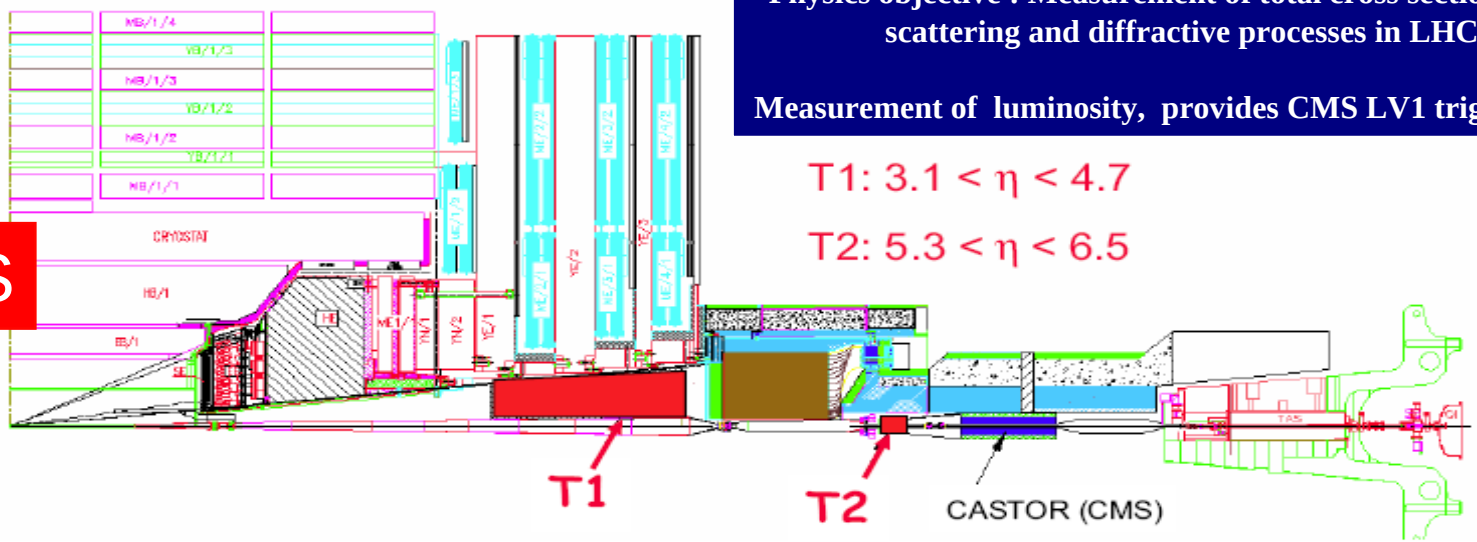
VFAT2 Design Application

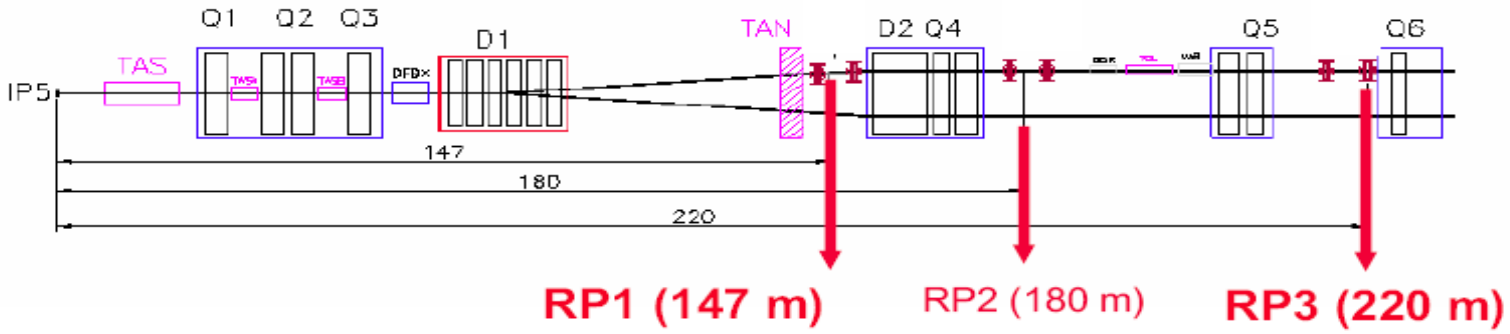
TOTEM in LHC

Physics objective : Measurement of total cross section, elastic scattering and diffractive processes in LHC.

Measurement of luminosity, provides CMS LV1 trigger input.

CMS



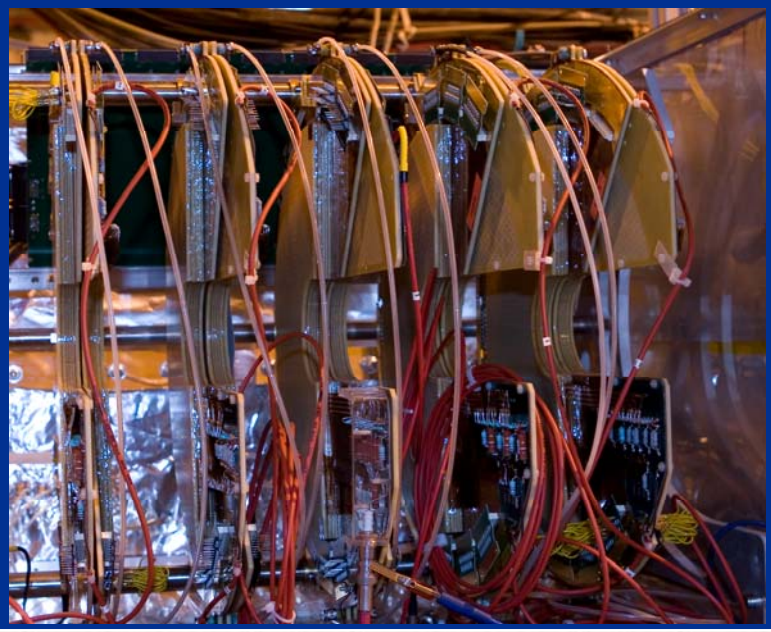


K.Eggert/CERN

TOTEM's 3 different detector technologies

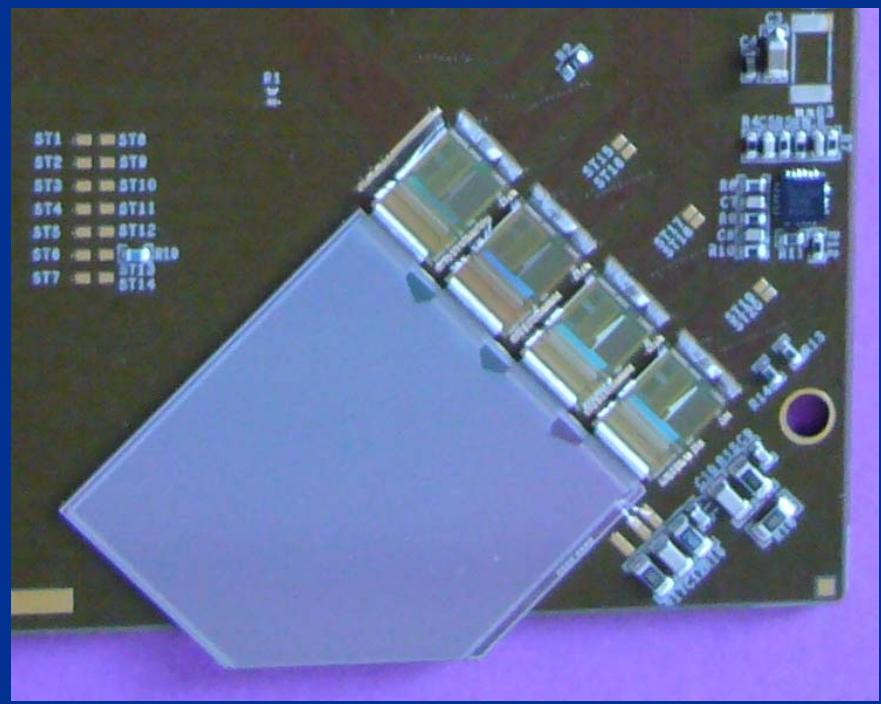
T1
CSCs

T2
GEMs

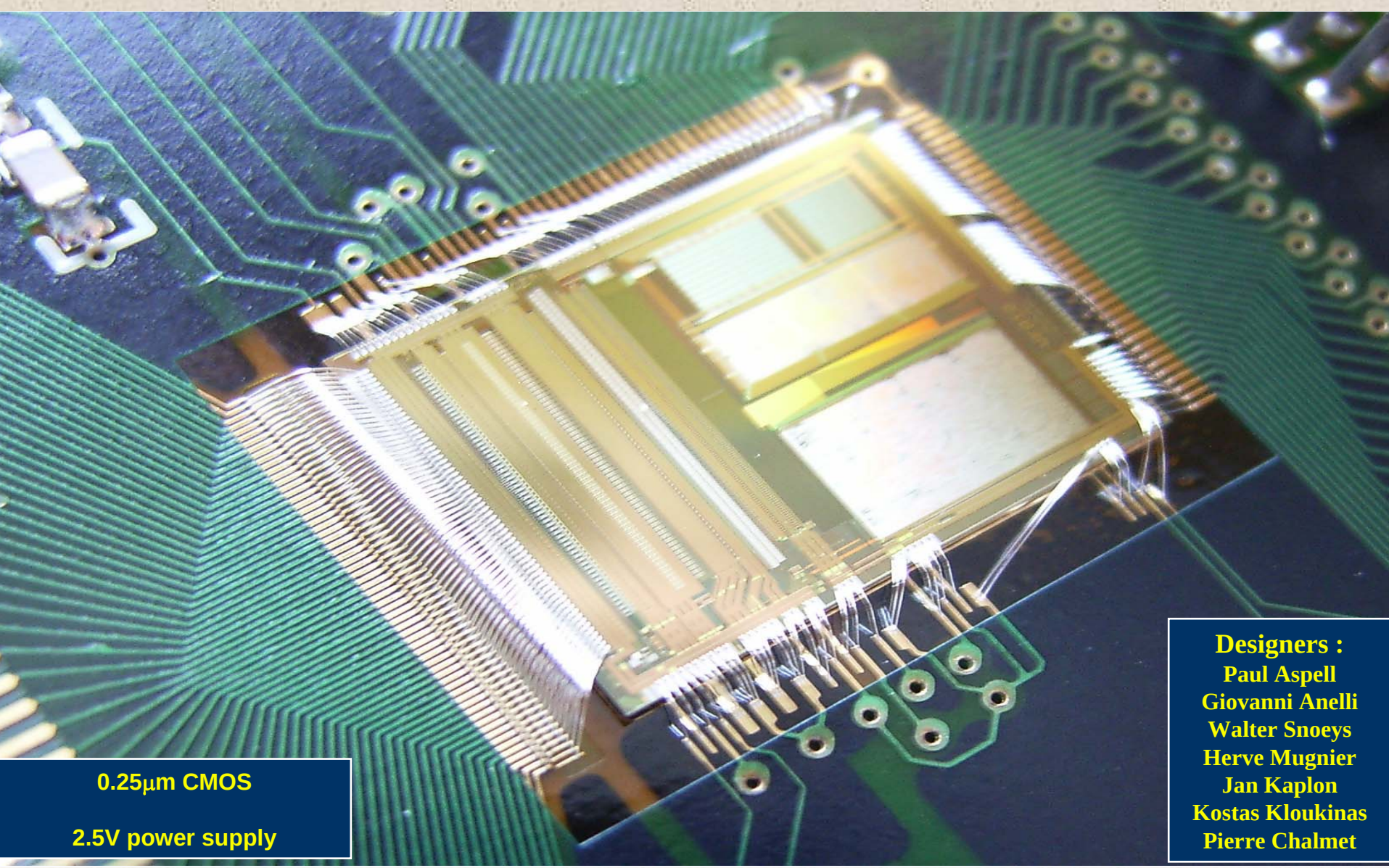


VFAT2 is used with all 3 detector technologies

Roman Pot – Silicon strips



Totem - VFAT2

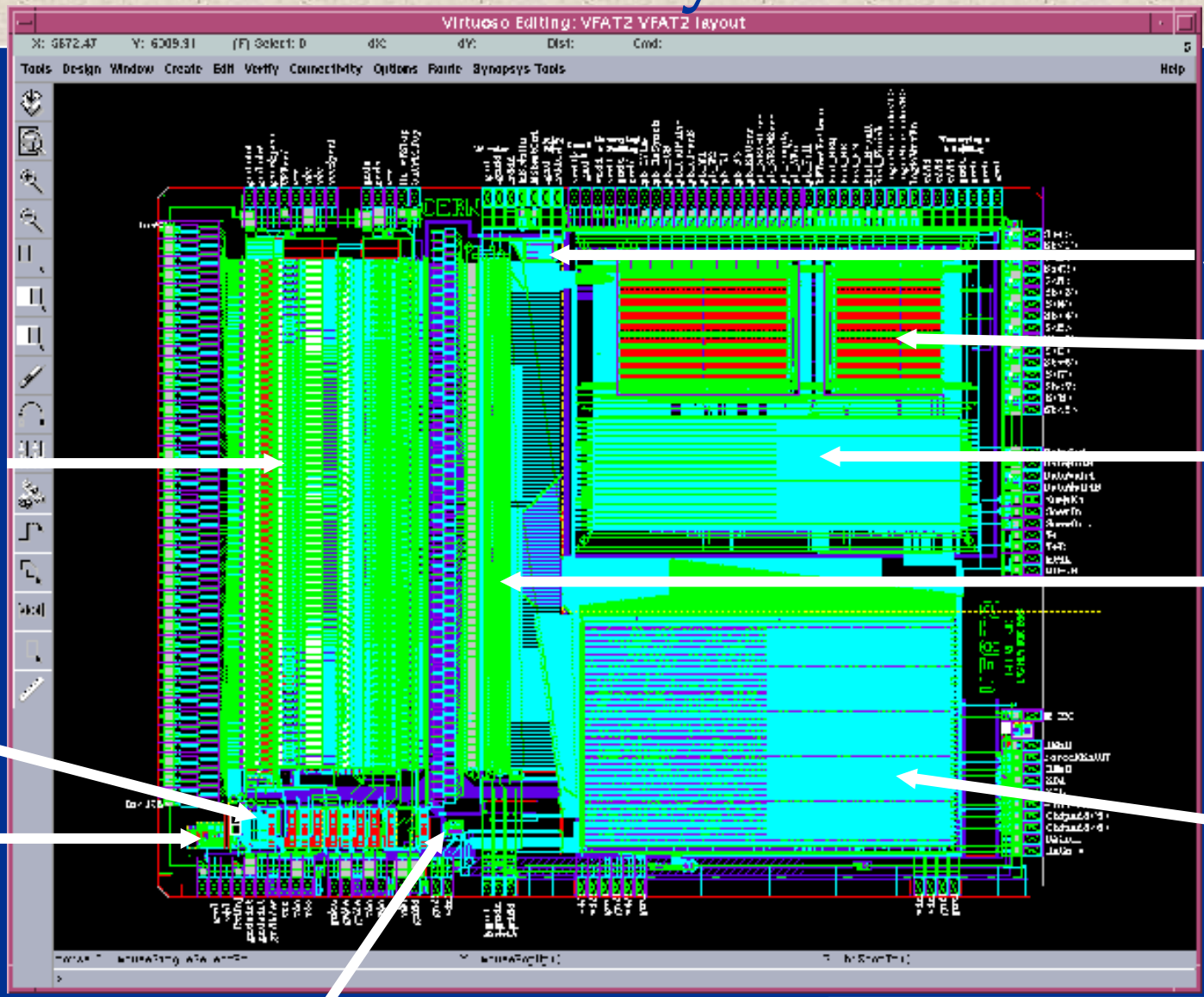


0.25μm CMOS

2.5V power supply

Designers :
Paul Aspell
Giovanni Anelli
Walter Snoeys
Herve Mugnier
Jan Kaplon
Kostas Kloukinas
Pierre Chalmet

VFAT2 layout



Sector Logic

SRAMs

Analog Front-end

Memory Logic

Sync. & Pulse Stretching

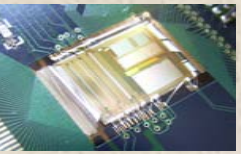
DACs

Band Gap Ref.

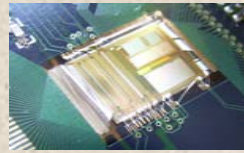
I^2C

DACo circuit

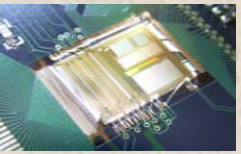
Size = 9.43mm * 7.58mm



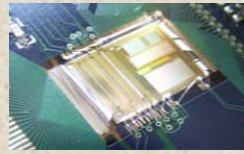
VFAT2 Functions



- **Trigger ……..**
  - Provide intelligent “FAST OR” information as an input for the first level trigger (LV1A).
  - Programmable segmentation for Roman Pot and GEM configurations.
- **Tracking …….**
  - Binary “hit” information for each of the 128 channels as triggered by the LV1A.



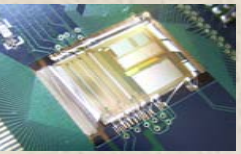
VFAT2 Key Features

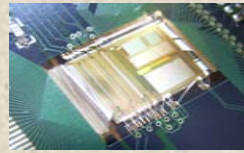


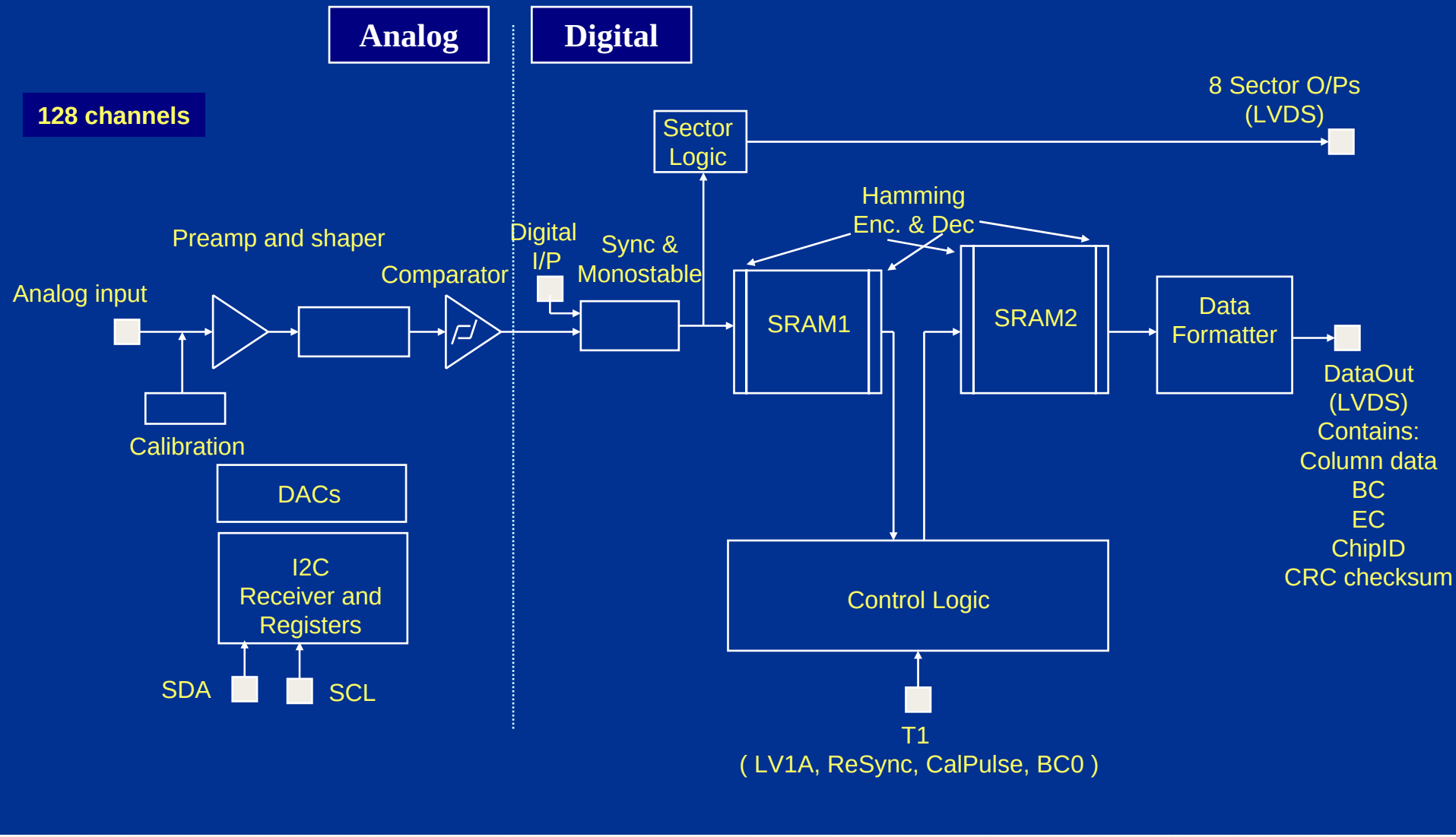
Trigger and Tracking Functions

- **128 channel** low noise front-end chip for binary readout of capacitive sensors.
- **40MHz signal sampling** (dead time free)
- **Digital memory** Programmable LV1A latency up to 256 clock periods. Simultaneously storage of up to 128 triggered events.
- **Trigger building** Programmable "fast-OR" trigger building outputs
- **Internal calibration** via internal test pulses with programmable amplitude
- **Fully programmable** through an I^2C interface.
- **Data packet output** includes headers, counters, flags and CRC check
- **Radiation tolerant** design – suitable for use in demanding radiation environments both with respect to ionising radiation and Single Event Upset.

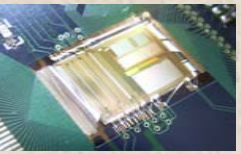
VFAT2 Signal Flow

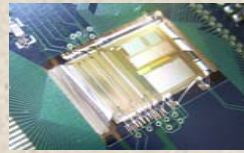


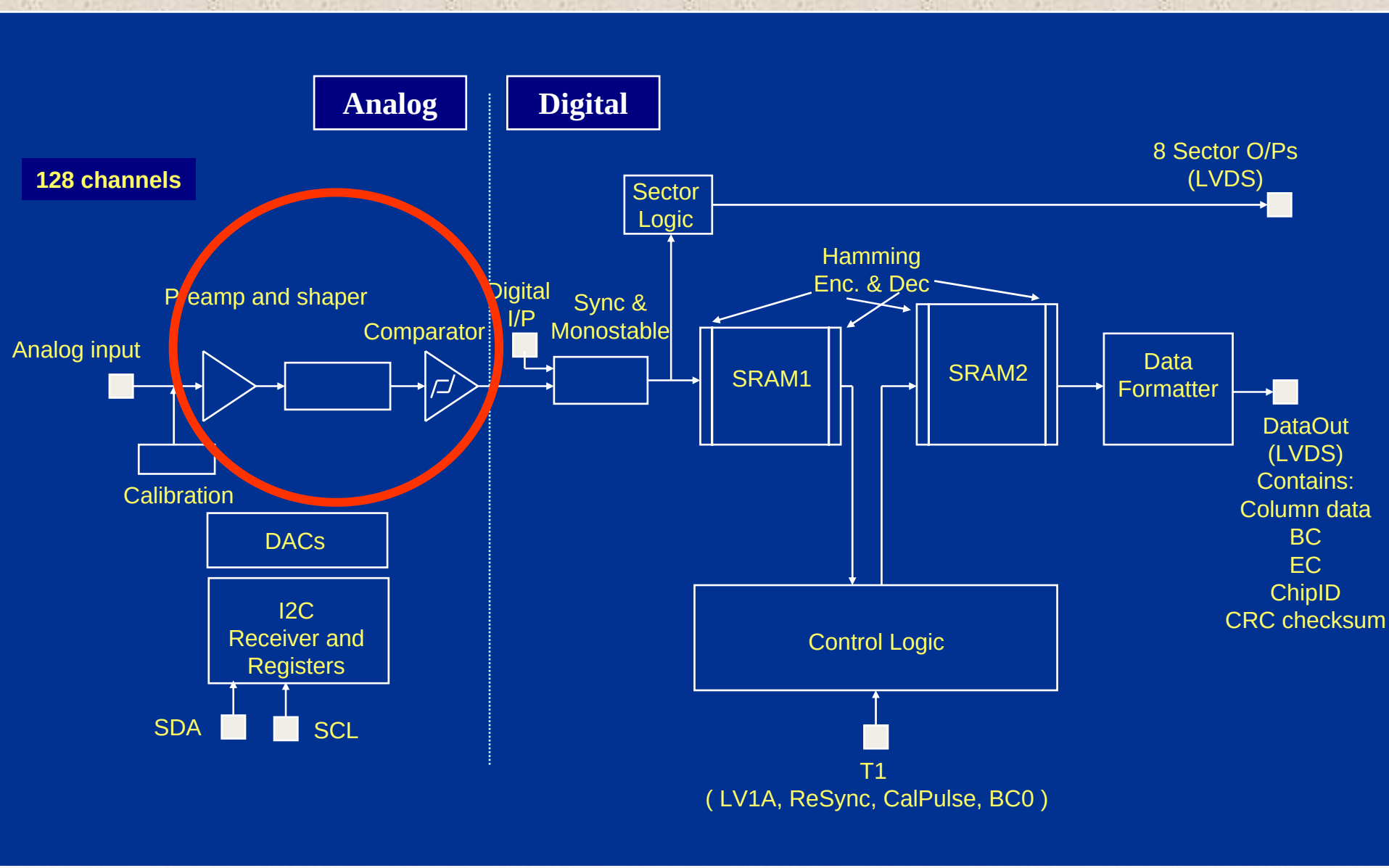




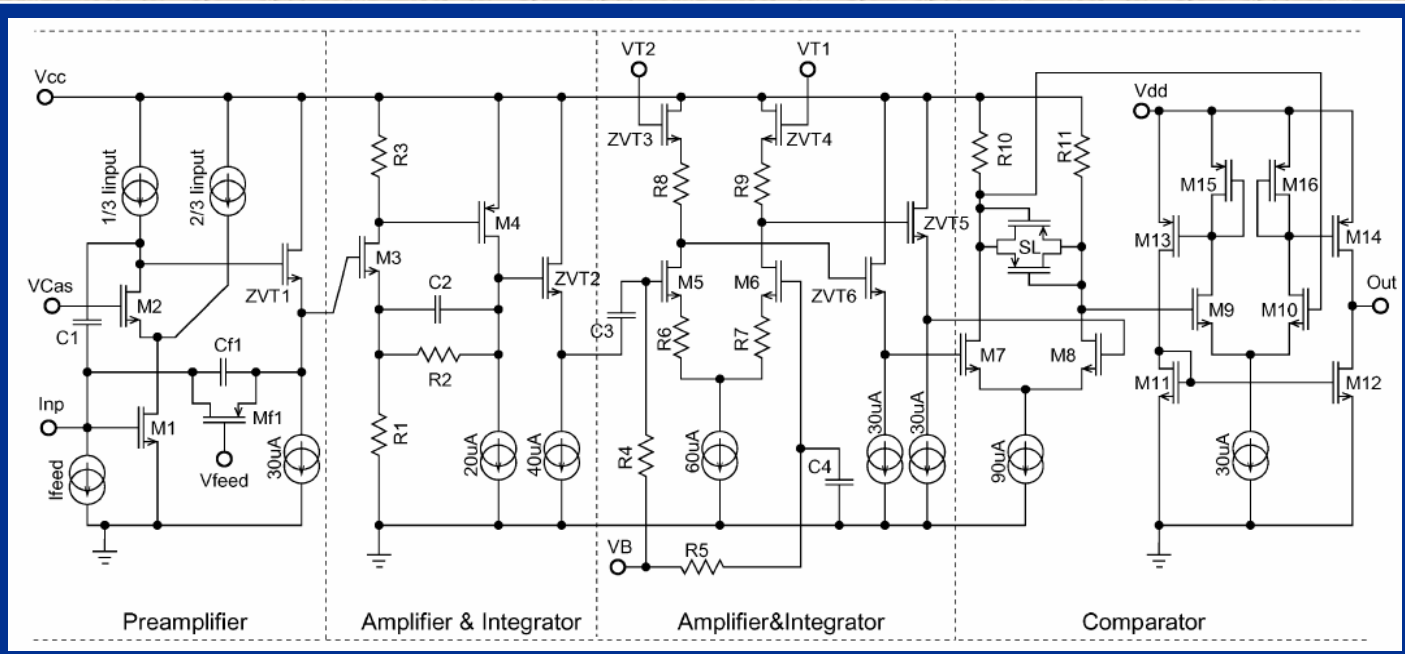
The Front-end







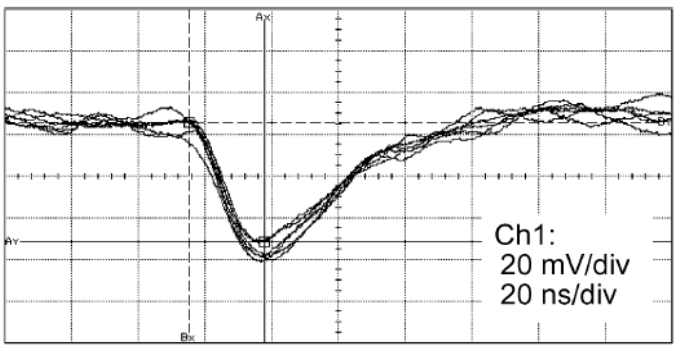
VFAT2 front-end

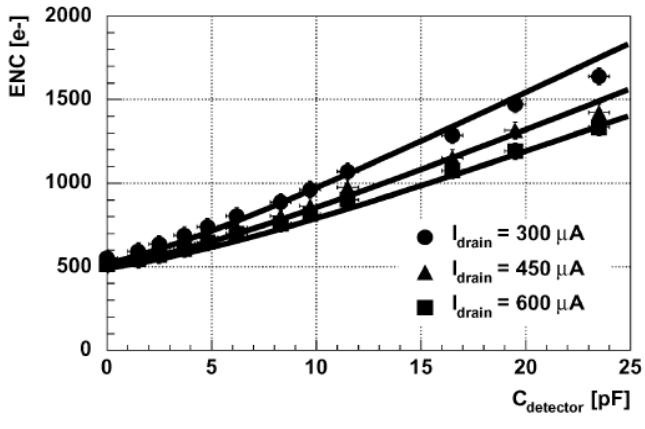


Also includes a 5 bit trim-DAC on each channel

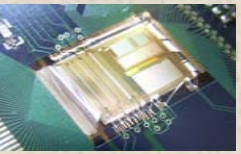
Gain	60mV/fC
Shaping Time	22ns
Power consumption	1.5 mW/channel
Linearity	± 12 fC
Time walk (for 1.2 to 10fC with 1fC threshold)	12ns
ENC (at 20pF)	<1500 e
Parallel noise	400e
Noise slope	40 – 60 e/pF
Radiation resistance	< 10 Mrads

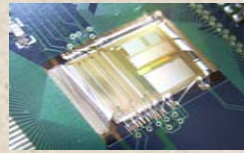
J.Kaplon, W.Dabrowski "*Fast CMOS Binary Front End for Silicon Strip Detectors at LHC Experiments* ,"
IEEE Transactions On Nuclear Science,
Vol. 52, No. 6, December 2005

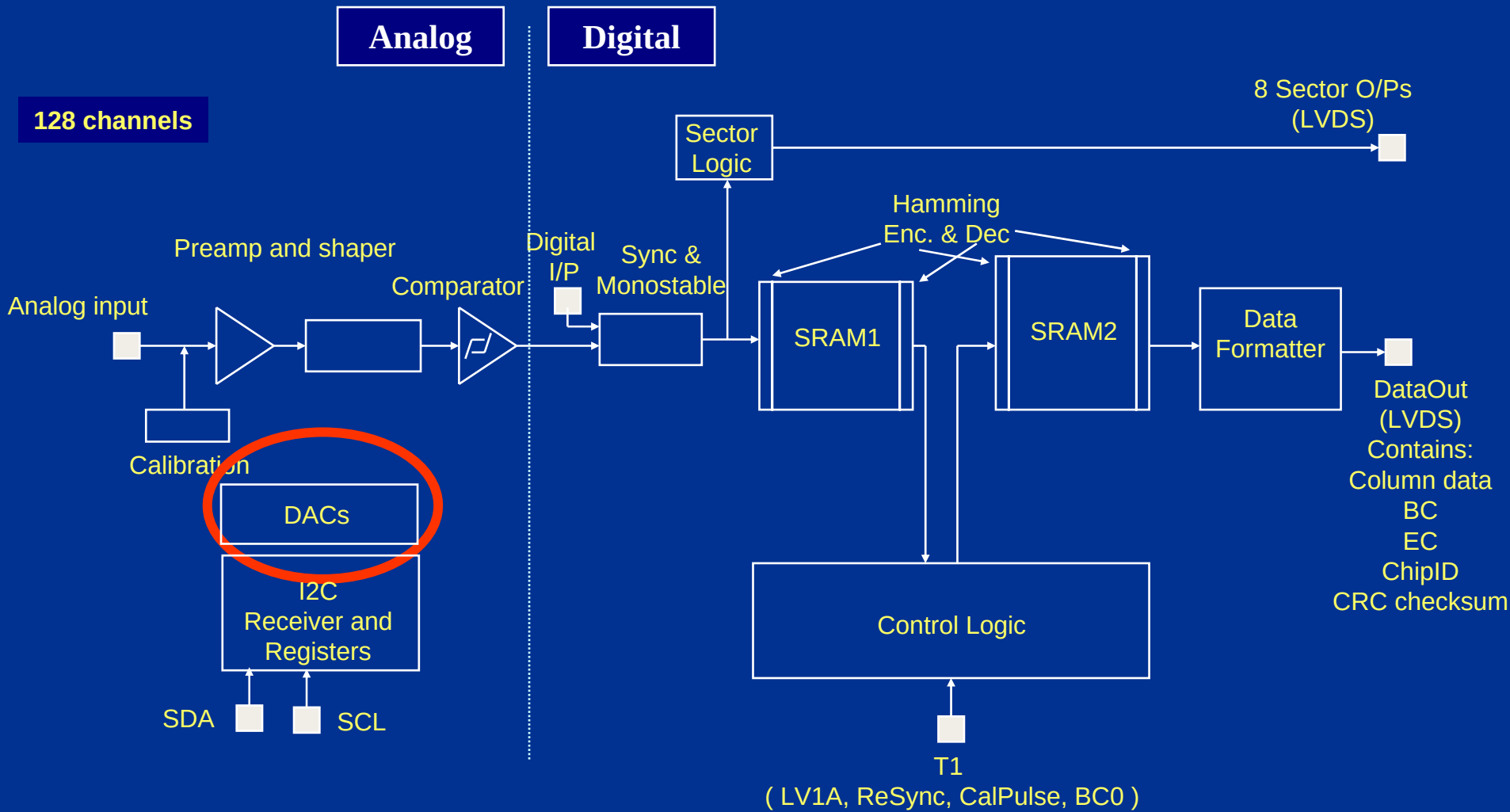




DACs

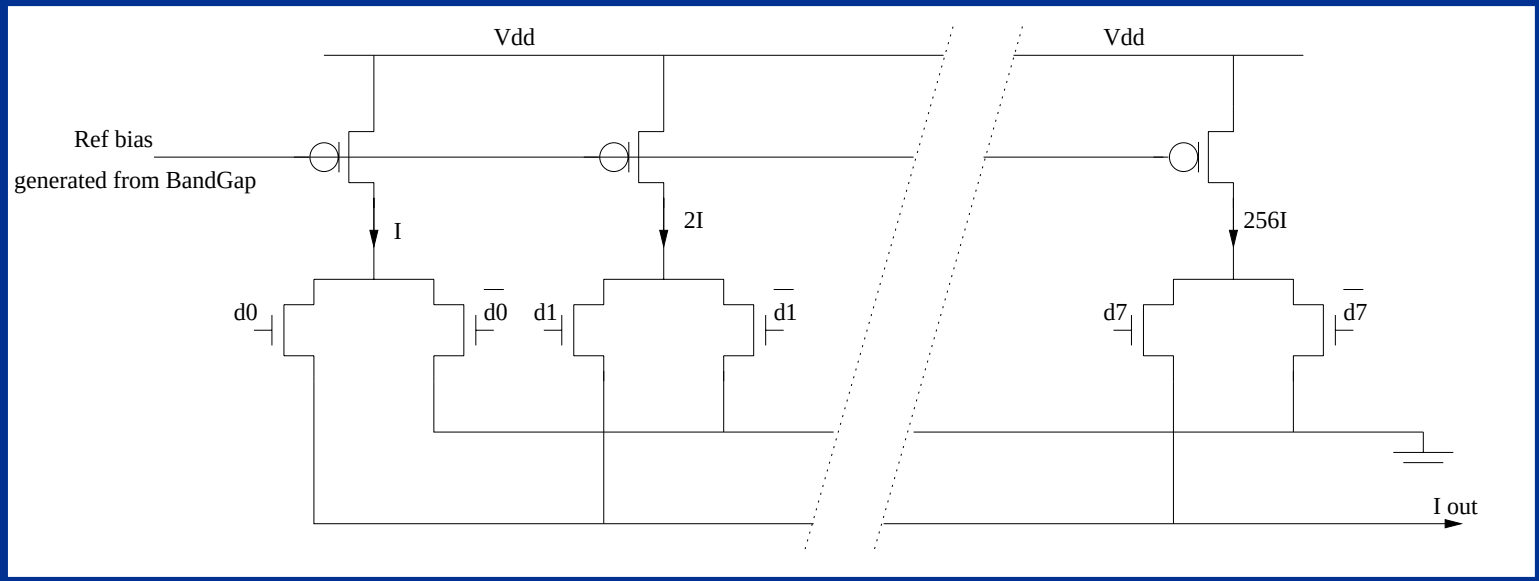





Analog
Digital
128 channels
8 Sector O/Ps
(LVDS)
Sector
Logic
Hamming
Enc. & Dec
Preamp and shaper
Digital
I/P
Sync &
Monostable
Comparator
Analog input
SRAM1
SRAM2
Data
Formatter
DataOut
(LVDS)
Contains:
Column data
BC
EC
ChipID
CRC checksum
Calibration
DACs
I2C
Receiver and
Registers
Control Logic
SDA
SCL
T1
(LV1A, ReSync, CalPulse, BC0)

DACs

6	8-bit current DACs for biasing of front-end.
2	8-bit voltage DACs for coarse threshold adjustment.
1	8-bit voltage DAC to control the calibration injection test pulse.
1	5-bit Trim DAC per channel to fine tune thresholds.

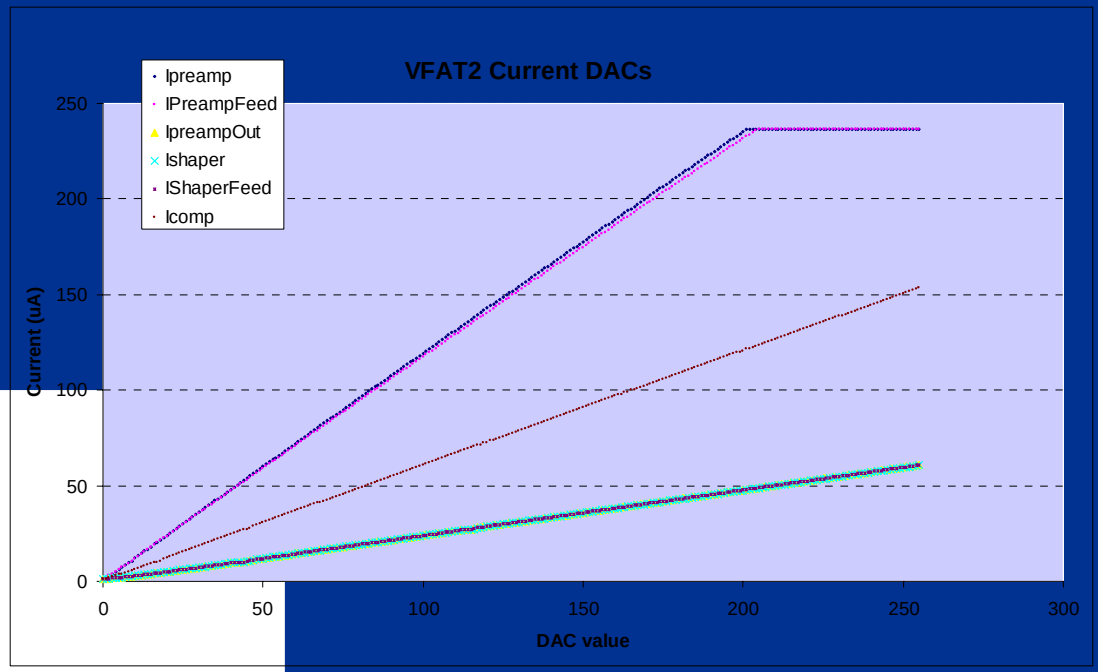


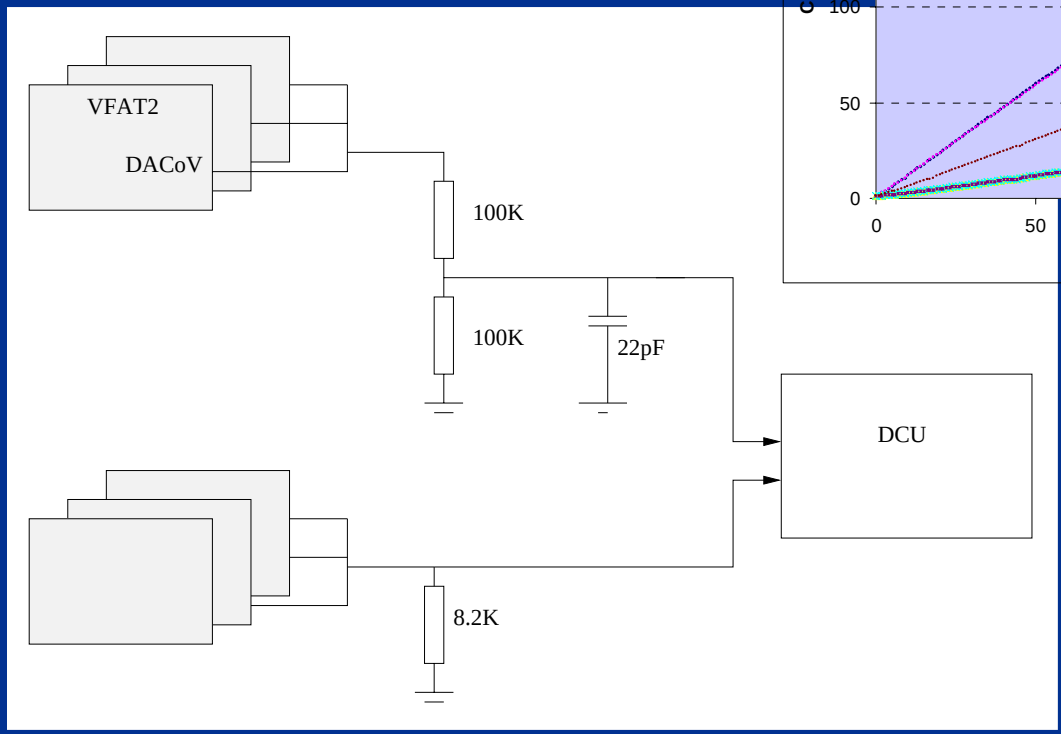
DAC design is a 8 stages of binary weighted current sources.
Reference bias for the DACs is a bandgap reference.

DAC values programmed via I^2C.

Characterisation of DACs

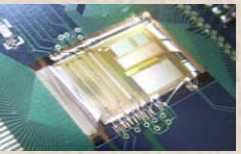
Each VFAT2 DAC response can be characterised.

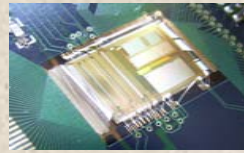


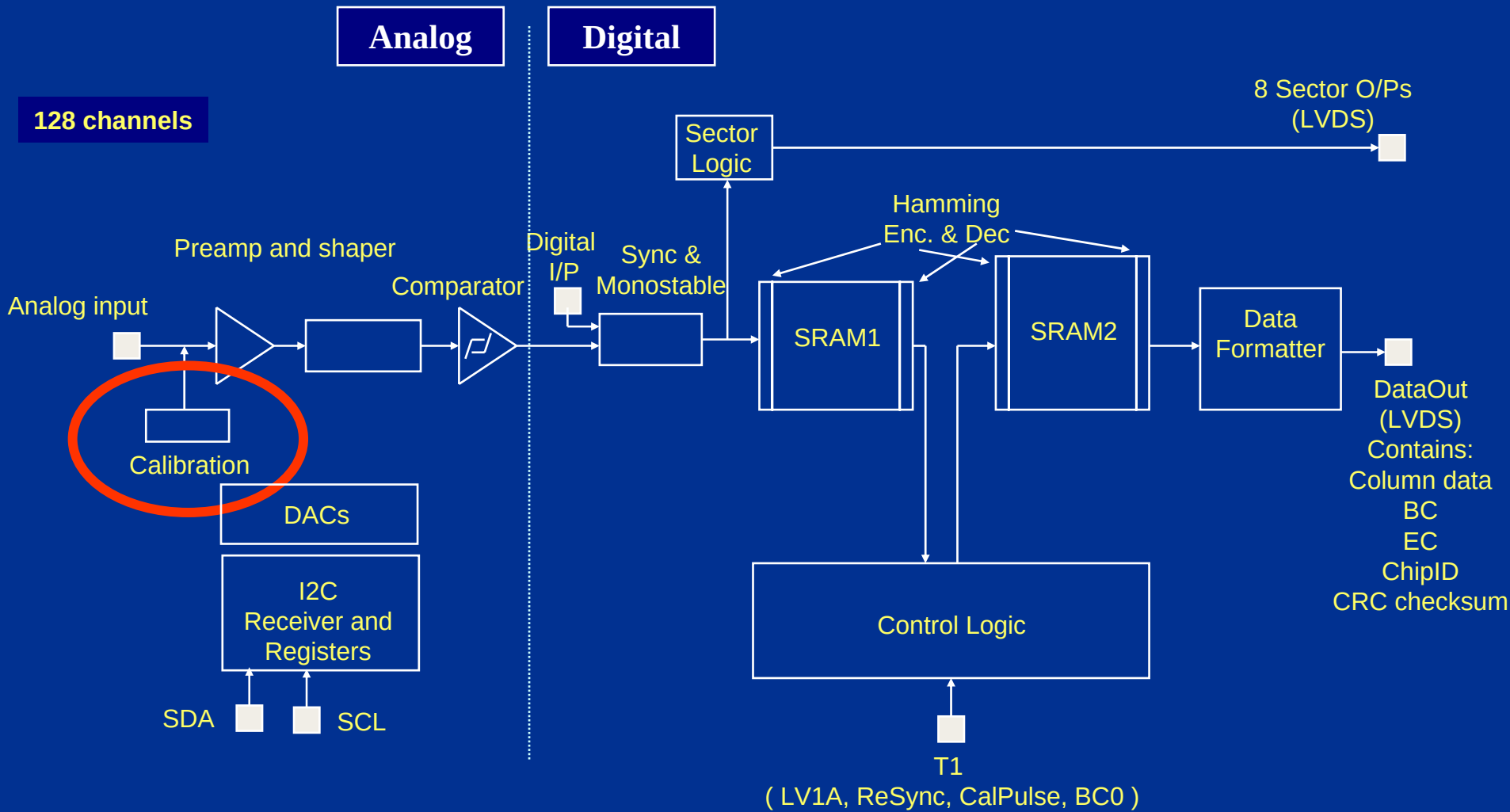


I2C commands route one by one each DAC V or I signal outside of the chip for measurement by the DCU. Also read by I2C.

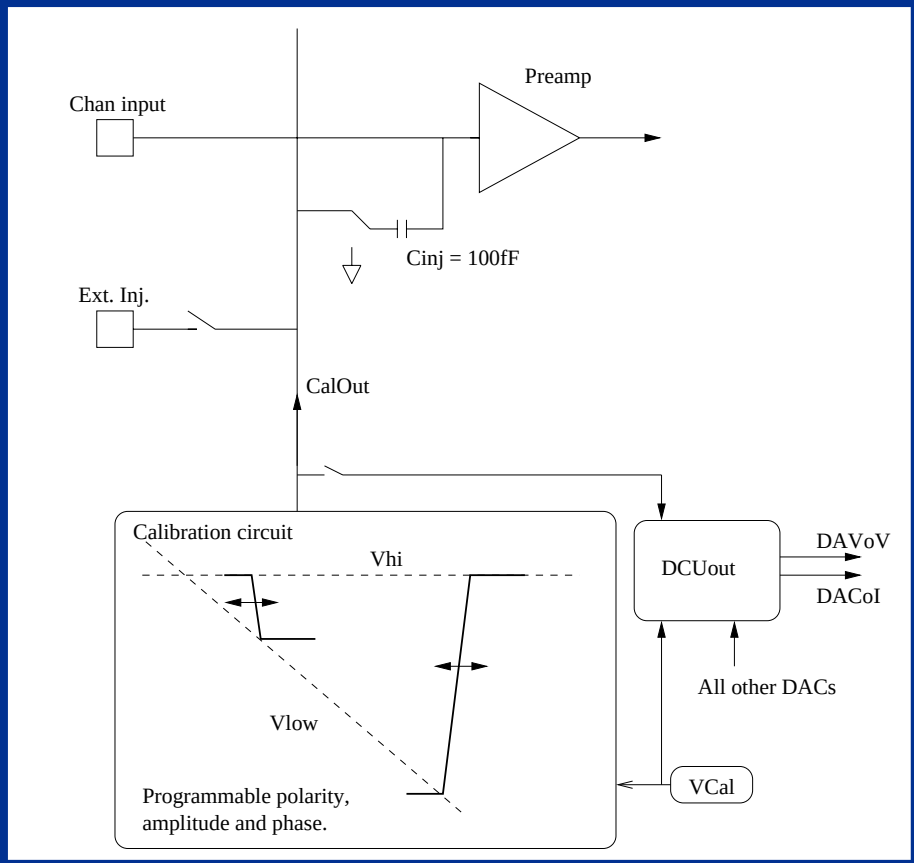
Calibration







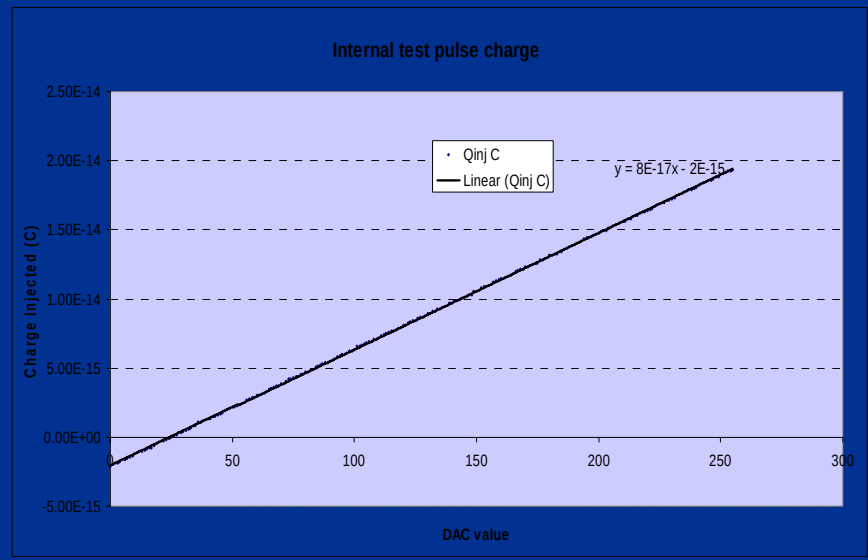
Internal Calibration Circuit



Injects a charge pulse to any one channel or group of channels selected by I²C.

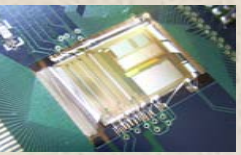
8 bit range

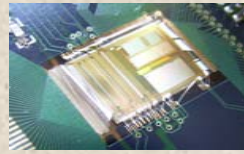
Linear fit Q-inj = $8^{-17}x - 2^{-15}$

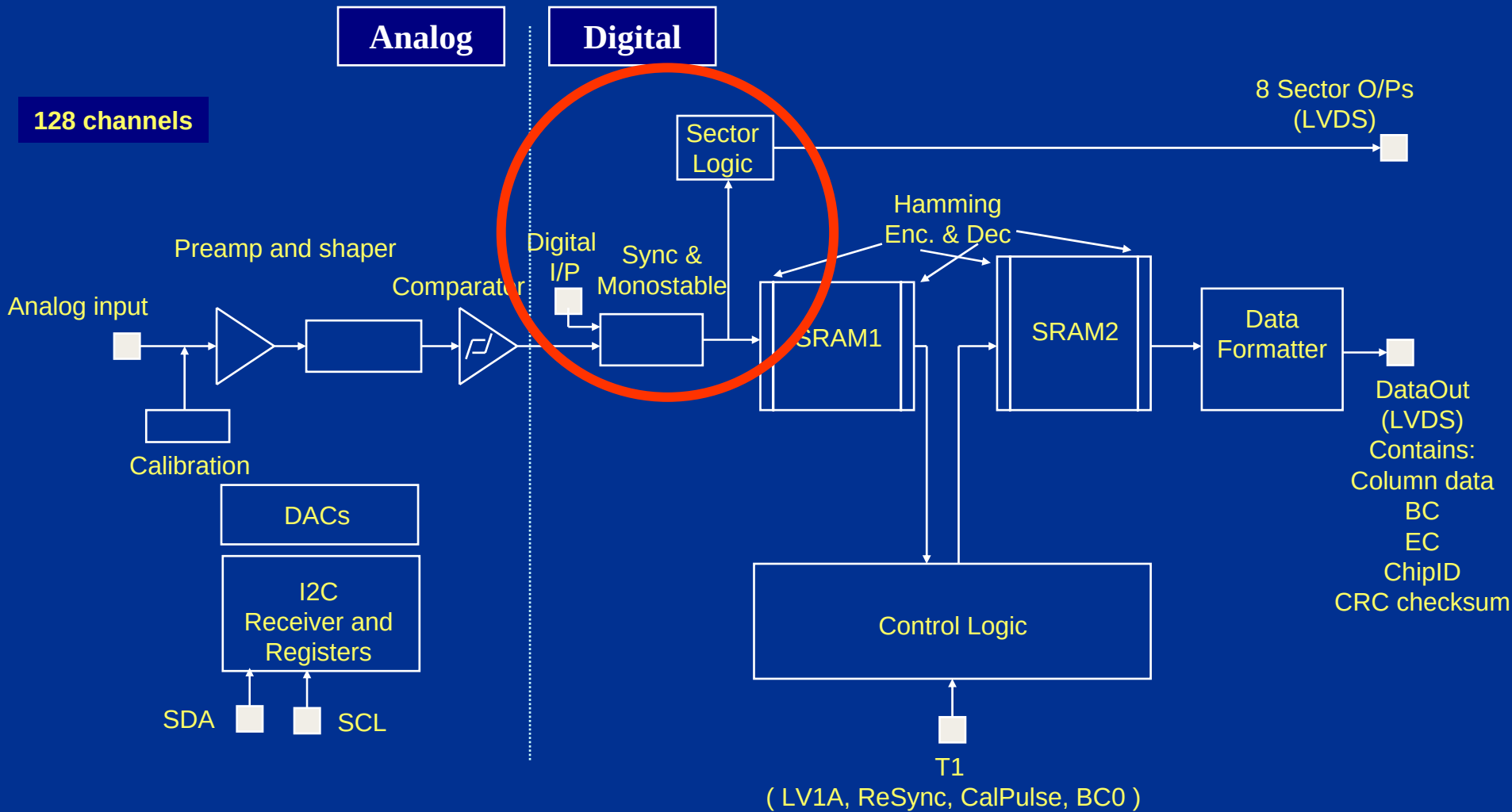


	Injection Range	LSB	σ (LSB)
Q	-2 fC to 18.5 fC	0.08 fC	0.3 fC

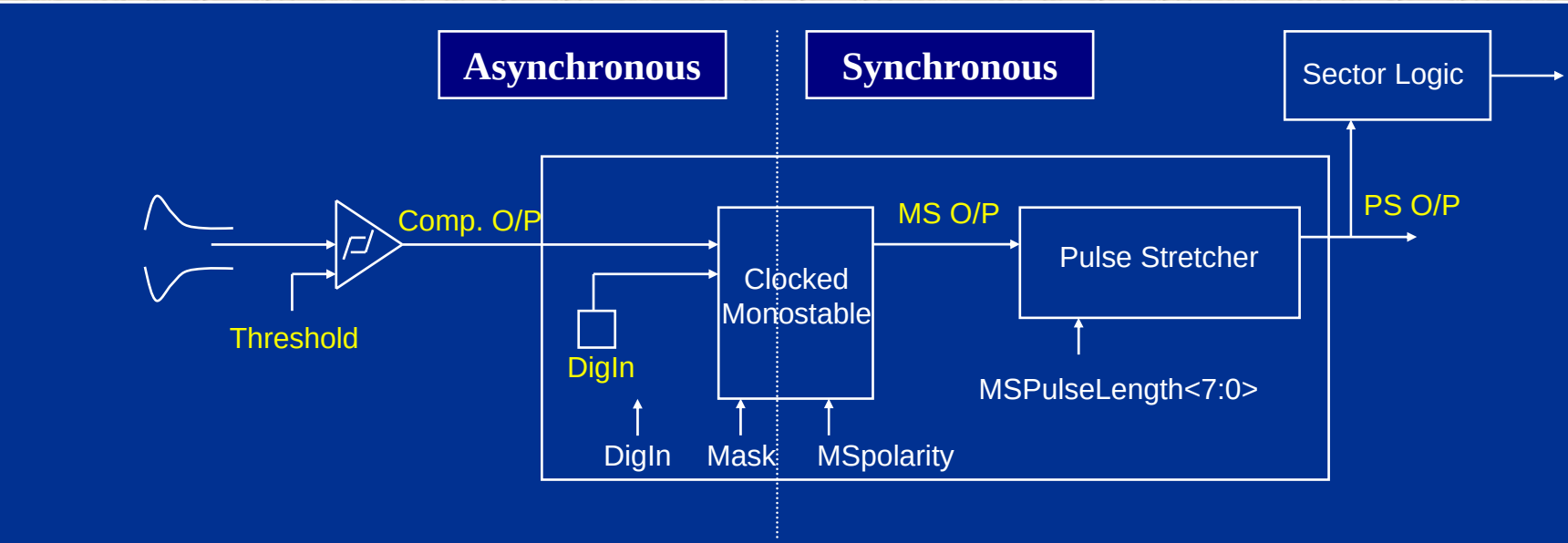
Synchronisation, Pulse Stretching & Sector Logic

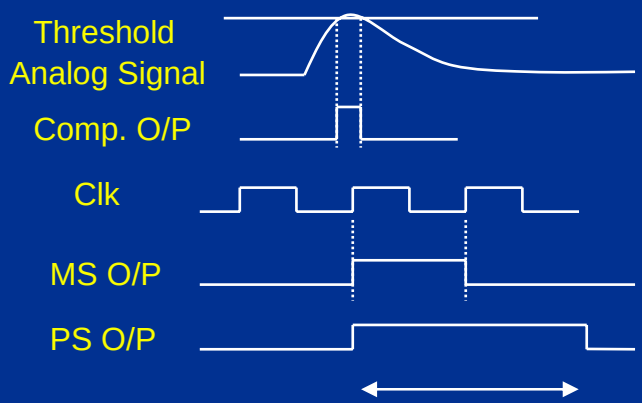


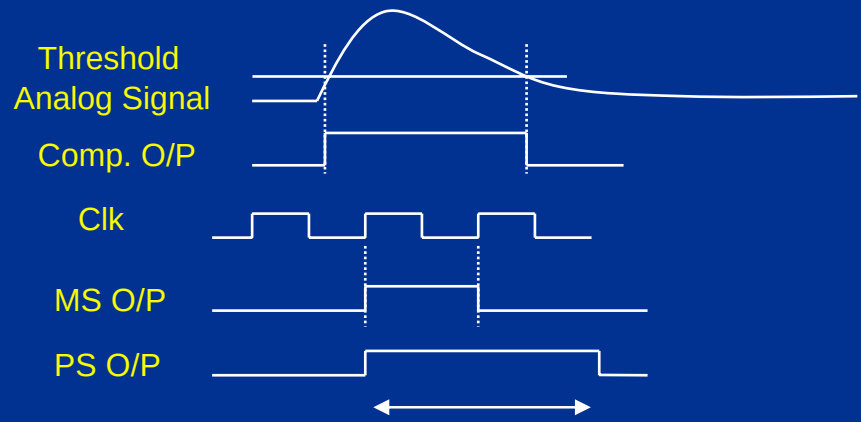




Synchronisation & Pulse stretching

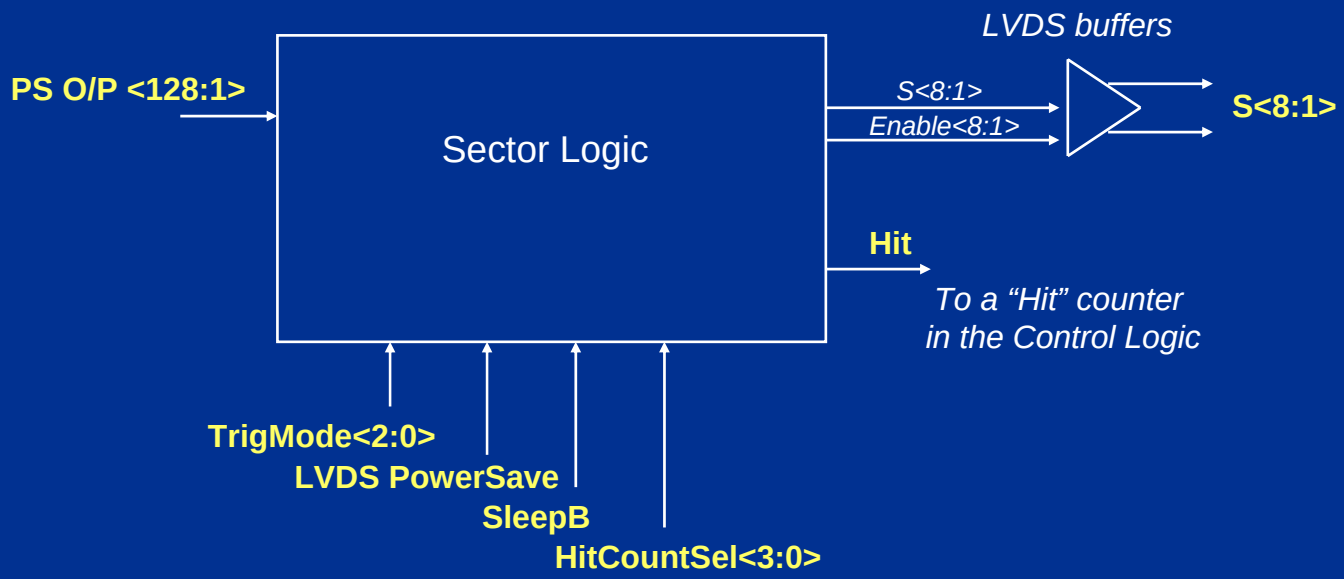




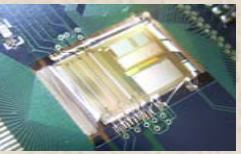


Pulse Stretcher O/P pulse length programmable from 1 to 8 clock periods

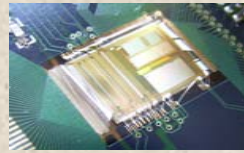
Sector Logic (Fast "OR")



TrigMode :	Defines 1 of 5 different Sector configurations.
LVDSPowerSave:	Turns unused LVDS drivers off to save power.
HitCountSel:	Selects 1 of 9 "FastOR" configurations for "Hit" counter.



VFAT2 Sector Configurations



TrigMode<2>	TrigMode<1>	TrigMode<0>	Function
0	0	0	No Sectors
0	0	1	One sector (S1)
0	1	0	Roman Pot Mode Four sectors (S1-S4)
0	1	1	Eight sectors (S1-S8)
1	X	X	GEM Mode Eight sectors (S1-S8)

S1-S8 unused

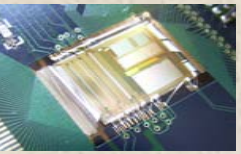
S1 = chan 1-128,
S2-S8 unused

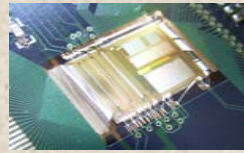
S1 = chan 1-32,
S2 = chan 33-64 etc
S5-S8 unused

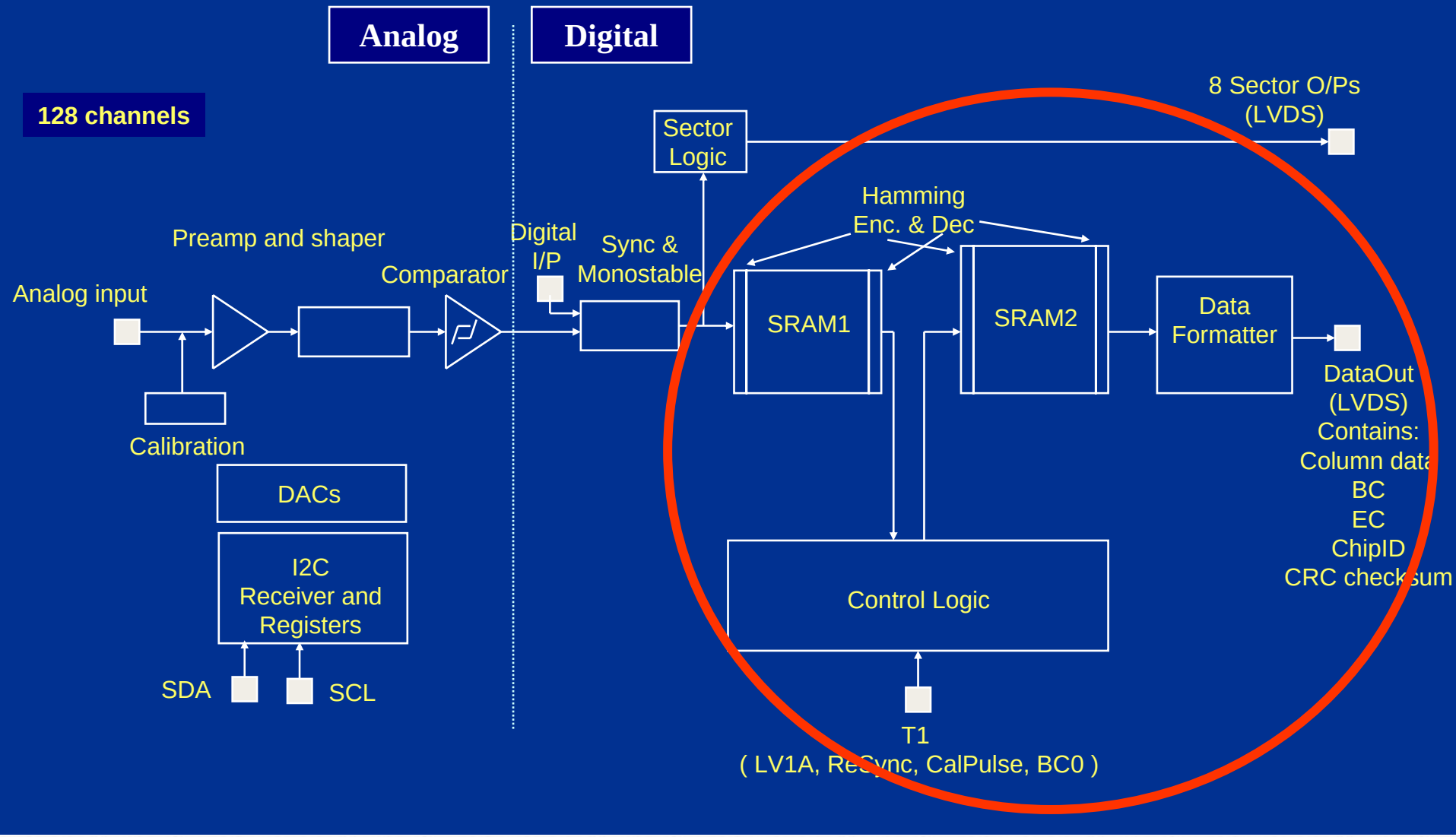
S1 = chan 1-16,
S2 = chan 17-32 etc

(Unused Sector outputs have powered-down LVDS drivers to save power)

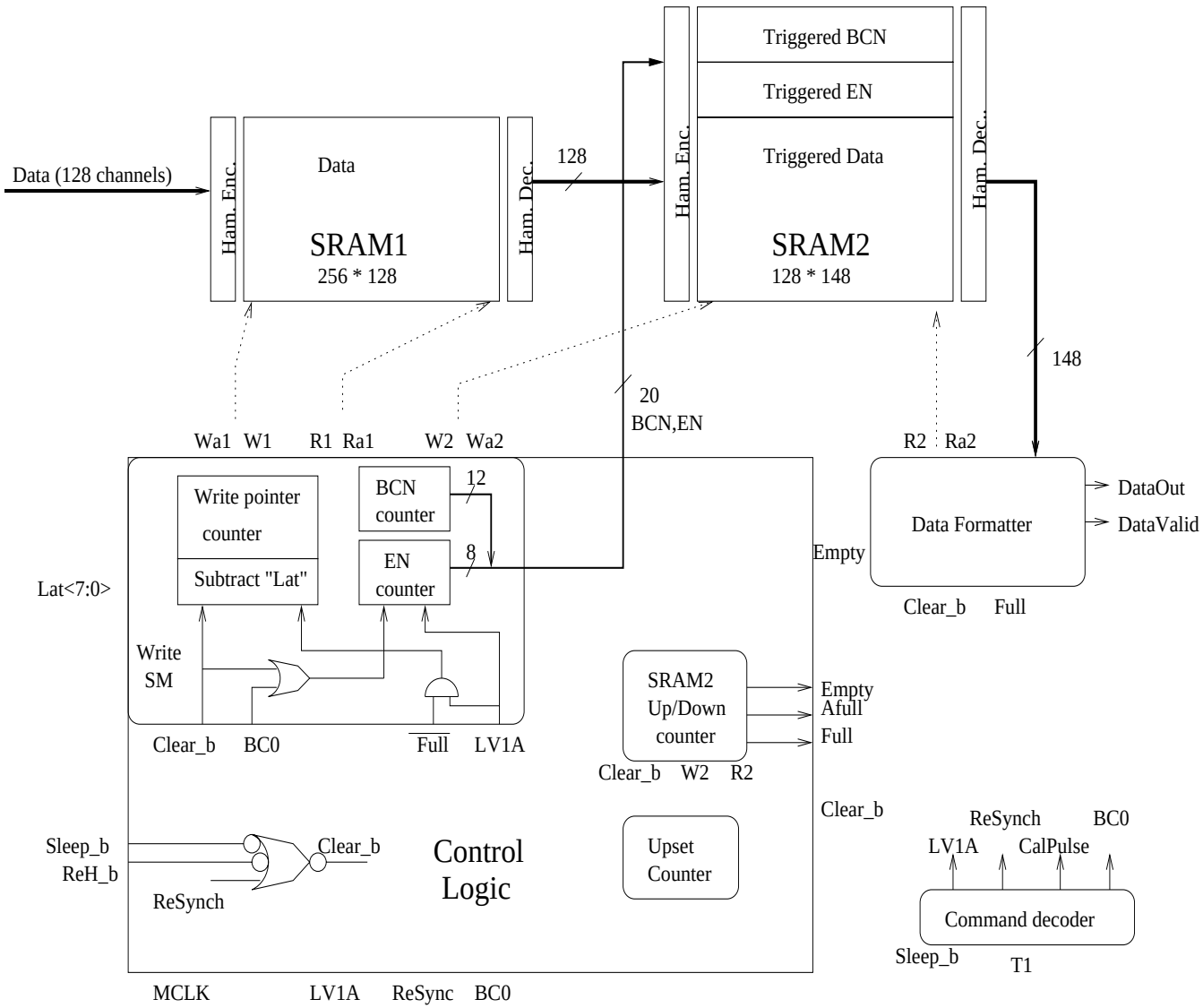
SRAMs, Control Logic and Data Formatter







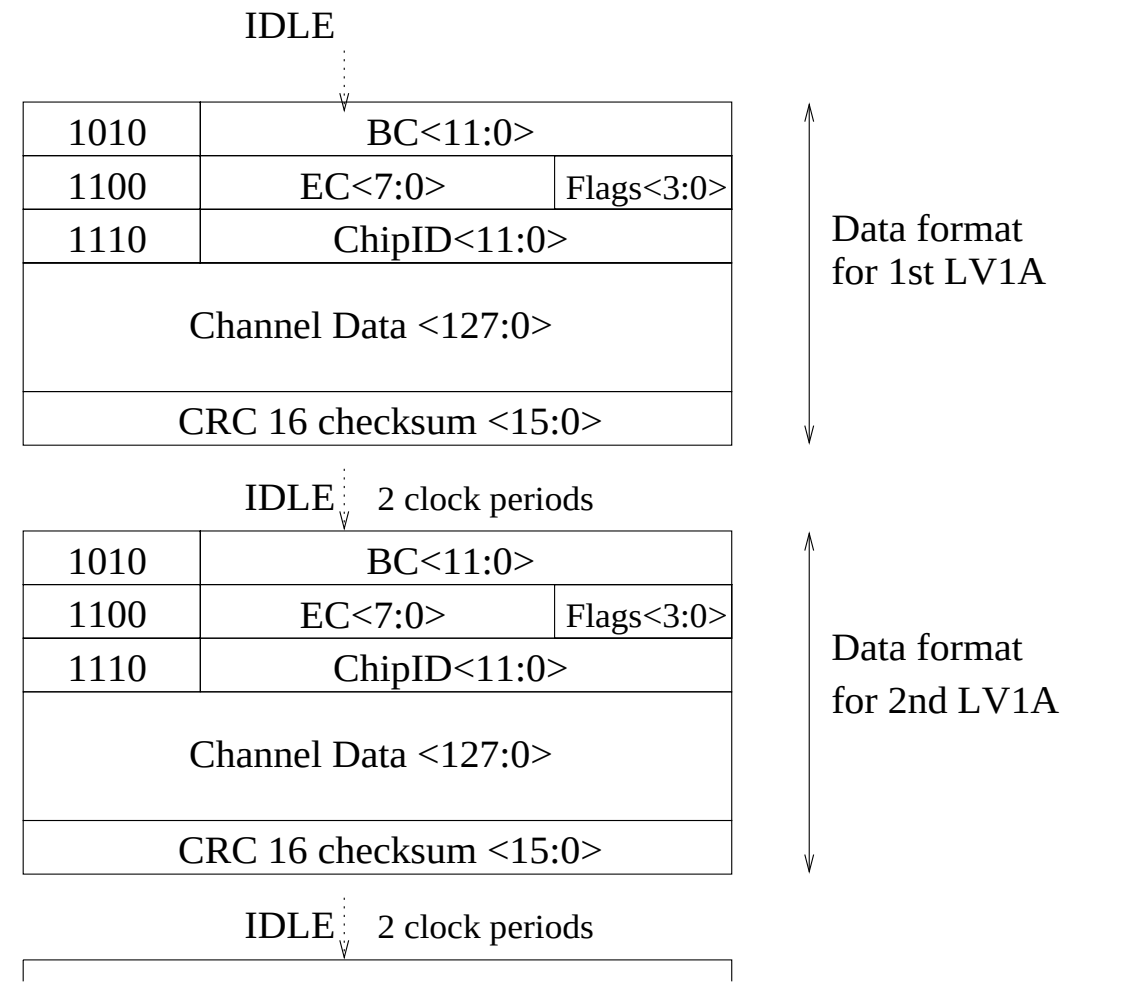
Control Logic & SRAMs



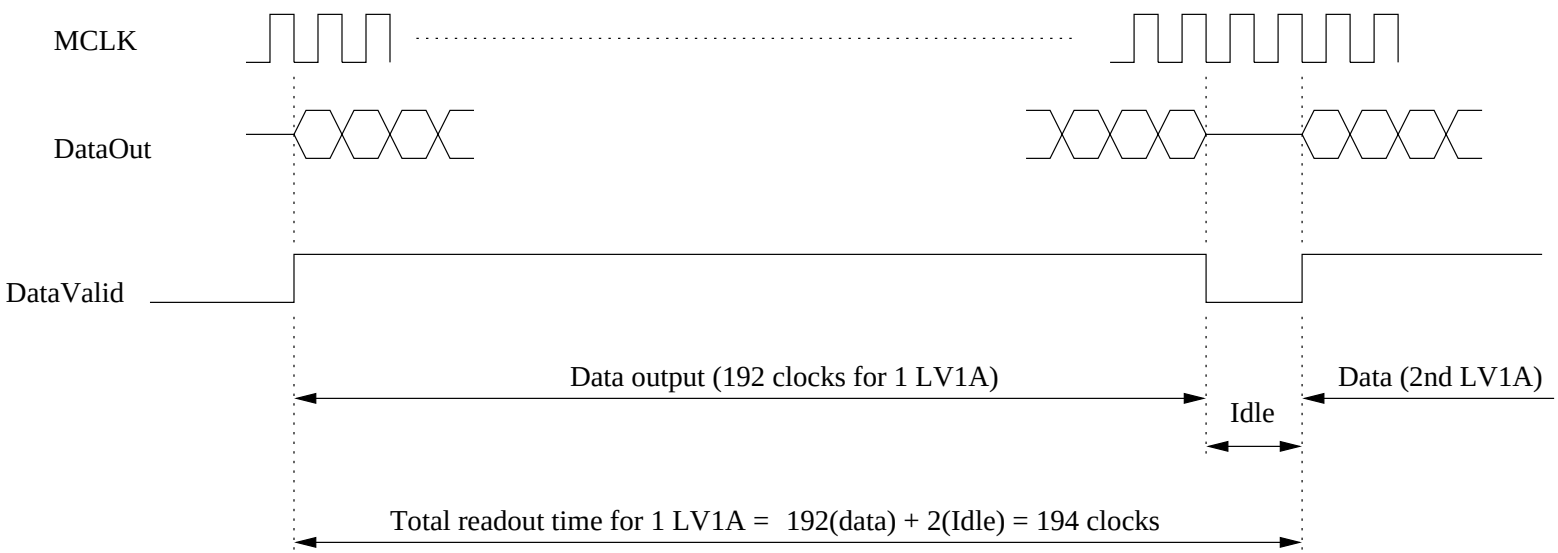
Command Decoder of T1

100 LV1A
111 CalPulse
110 ReSync
101 BC0 Bunch crossing
zero

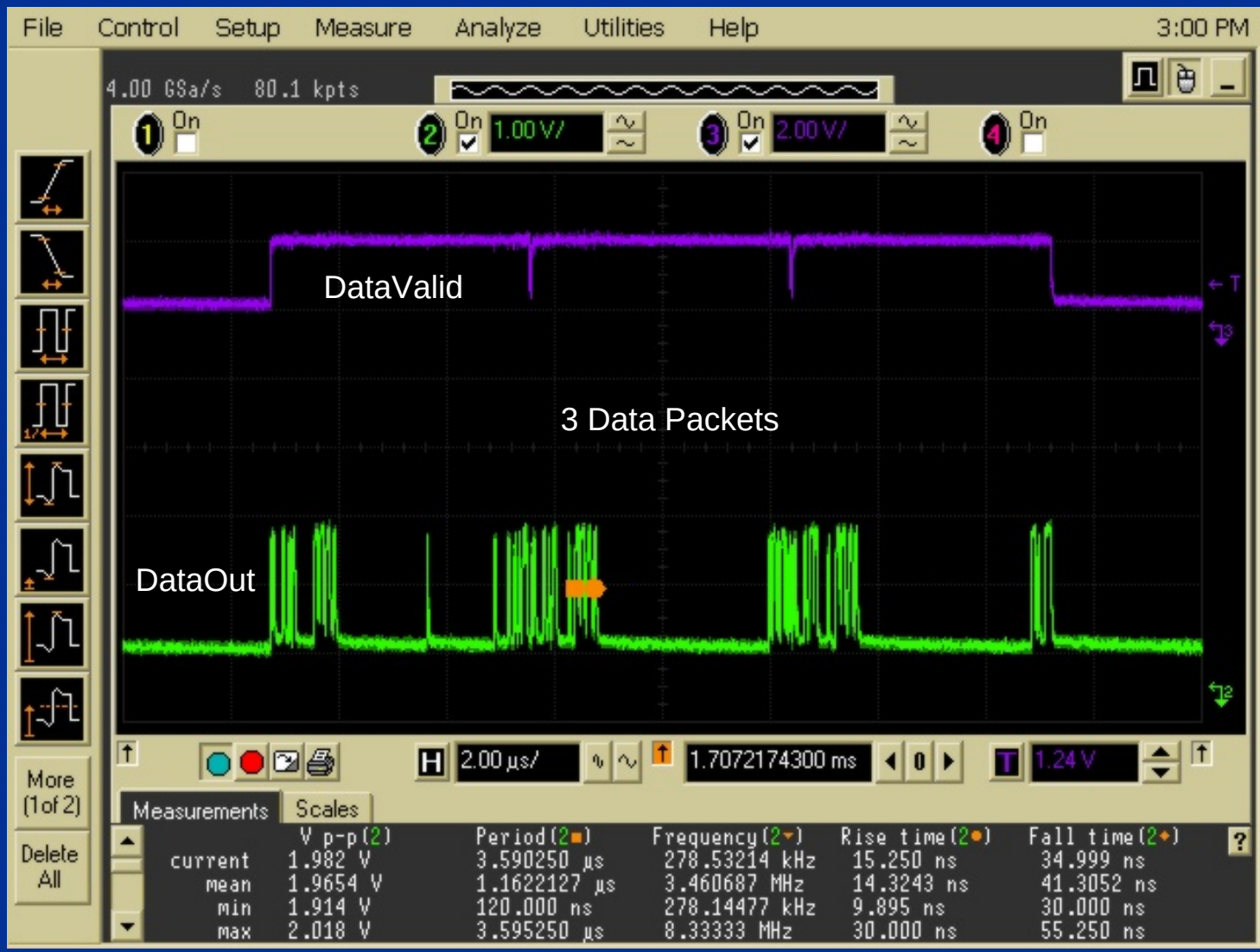
VFAT2 Data Format



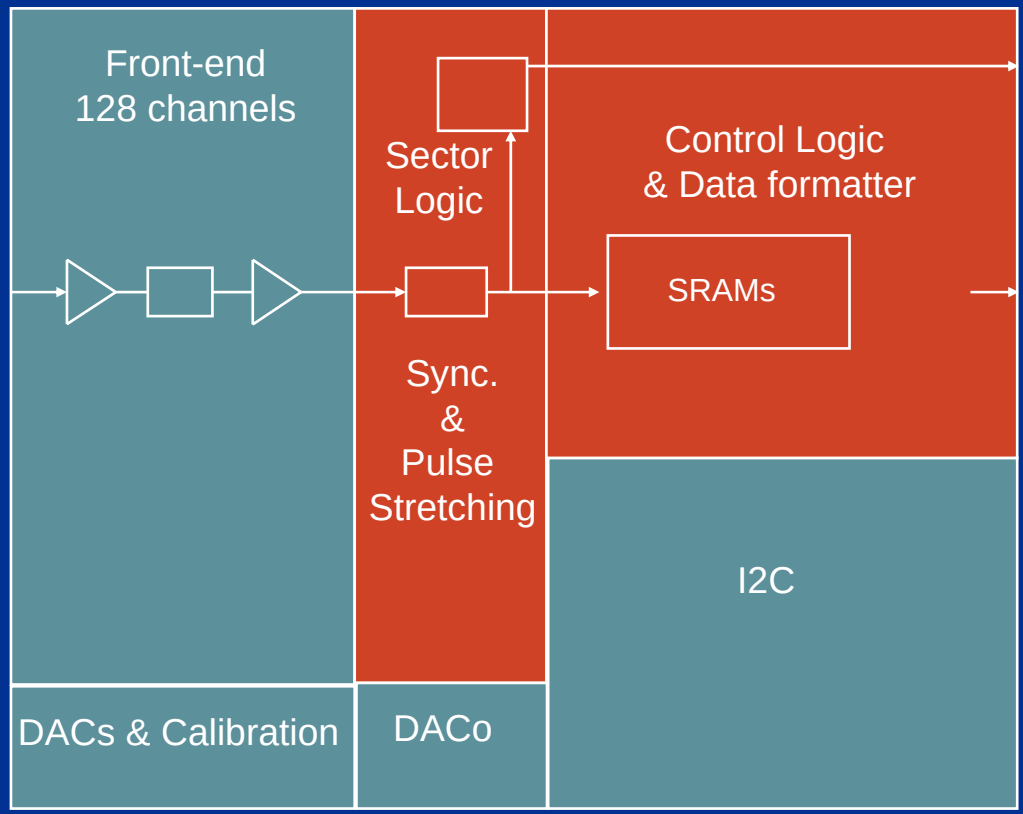
VFAT2 Data Format



VFAT2 Data Packet on the output



Reducing Substrate Noise



Power Supplies

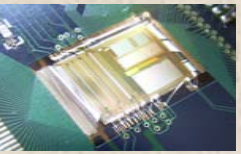
Analog

Digital

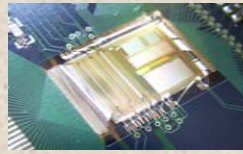
Each module has it's own power supply pads (as many as possible).

All modules have heavy guard-rings.

Digital powered modules have separated gnd and return paths. New digital library developed.



Digital Testability Functions



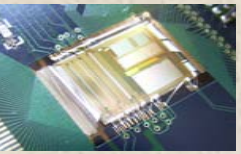
Scan Path :
Scan path in Control logic flip flops.

Probe Pads :
Probe pads enabled by an I2C command to access critical internal nodes.
ReSync, LV1A, CalPulse, W1, Clear, R1, W2, SEUerr, R2, Hamming err1, Hamming err2, AFull, Empty, Full

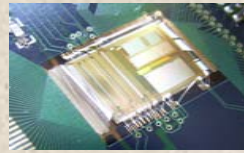
BIST :
Using external pins it checks the SRAMs with internally hardwired test patterns and returns a result within 2ms. Intended for use in production testing.

ATPG (Automatic test pattern generator) :
Predefines the channel input to the SRAMs with either
all 0s,
all 1s,
101010
and alternating 0101 and 1010.
Results seen in DataOut packet

Automatic Data Packet Generator :
Can be set by either an I^2C command or by and external pin.
“Where is the Higgs ?” in ASIC



Design for Radiation

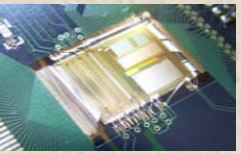


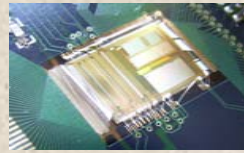
Total Dose : All circuits designed with structures proven to withstand total dose levels up to 100MRads.

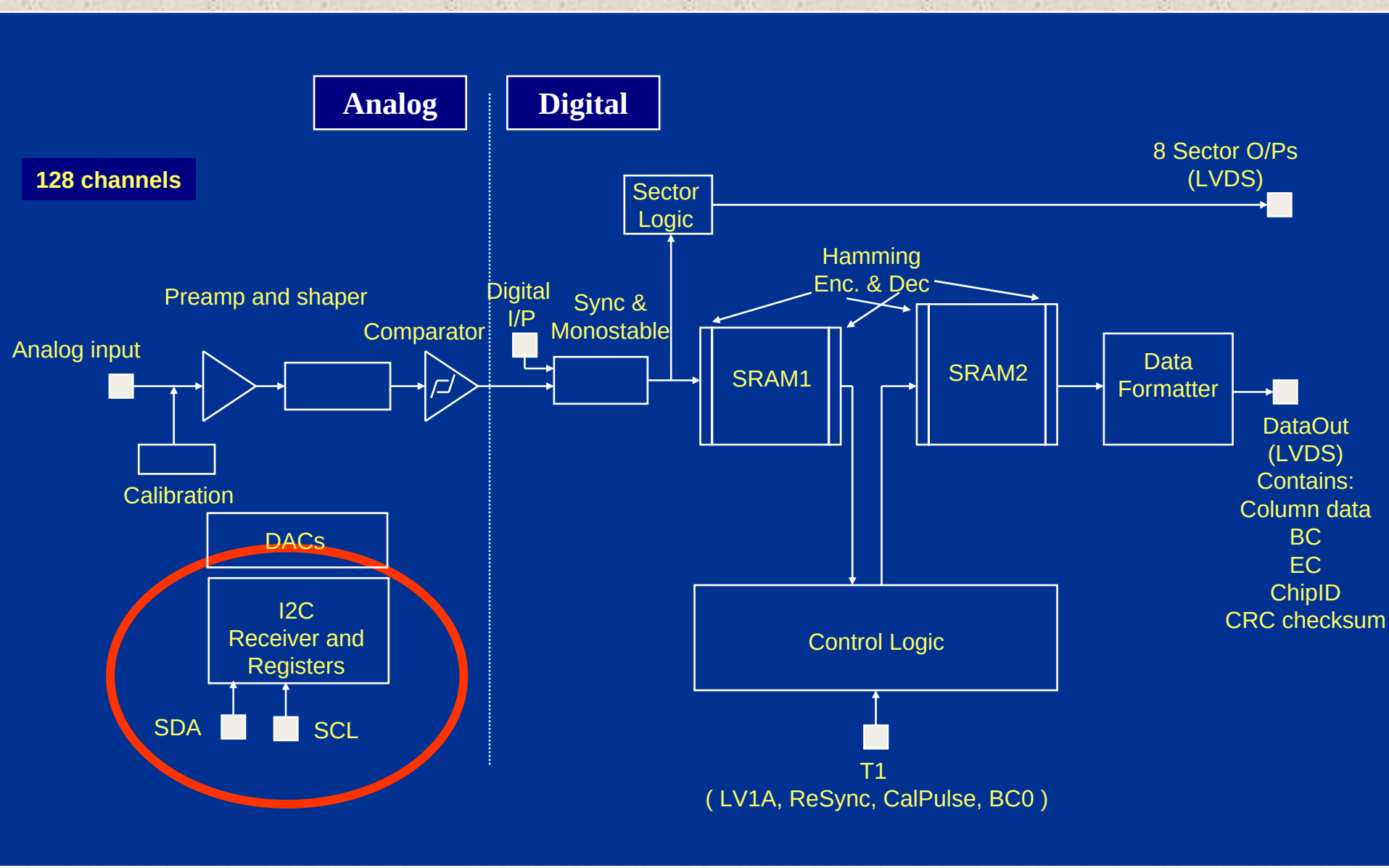
SEU in logic circuits :

I2C:	Triplication and Majority Voting
Control Logic & Data Formatter:	Triplication and Majority Voting
SRAMs:	No triplication. Data protected by “Hamming” encoding.

I²C Interface







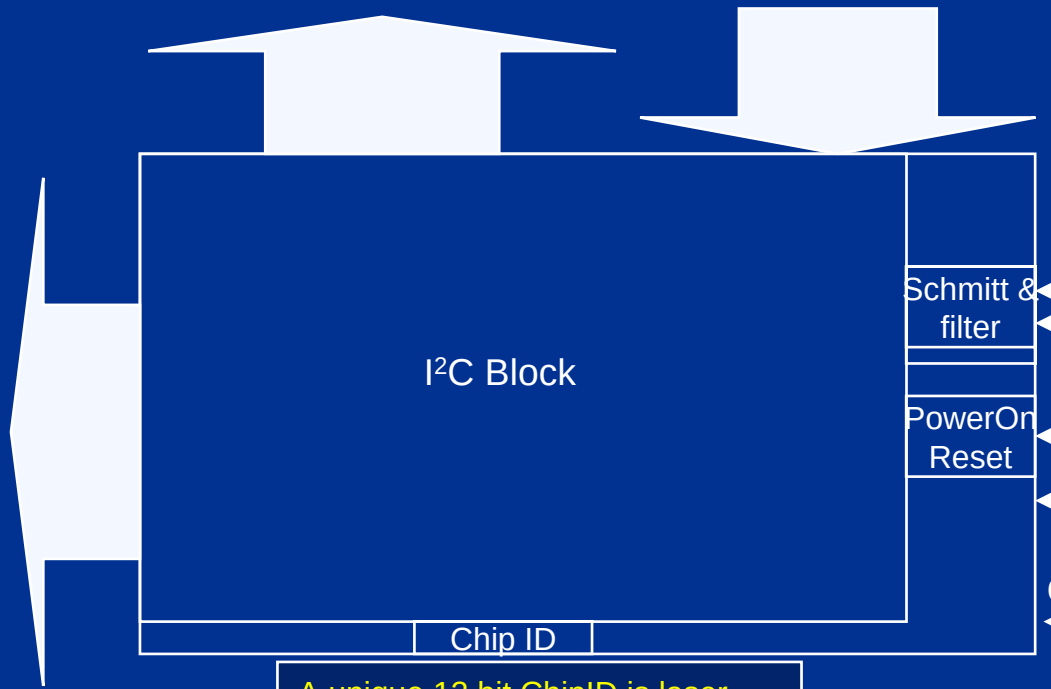
The I²C Interface

VFAT2 is a highly flexible chip thanks to the programmability through the I²C interface.
It incorporates **152 * 8** bit programmable “Write/Read” and “Read Only” registers.

The I²C has asynchronous logic hence does not use a sampling clock.

W/R registers to program and verify bias and operational mode settings.
R/O registers to monitor internal status conditions.

Noise rejection and rail to rail glitch protection on SCL and SDA pads.



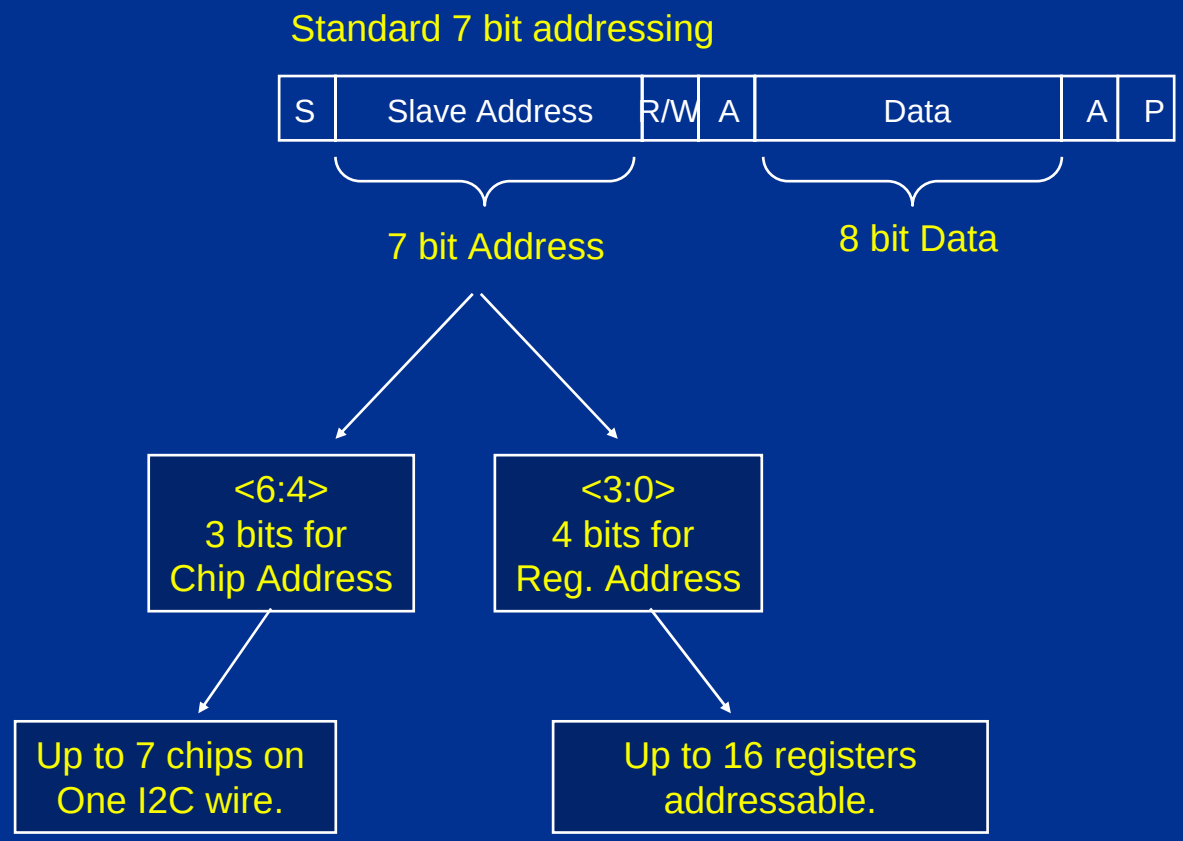
REhB :
Hard reset > Sleep Mode
(activated on Power Up)

REsB :
Soft reset > Resets just I2C logic but not the register contents.

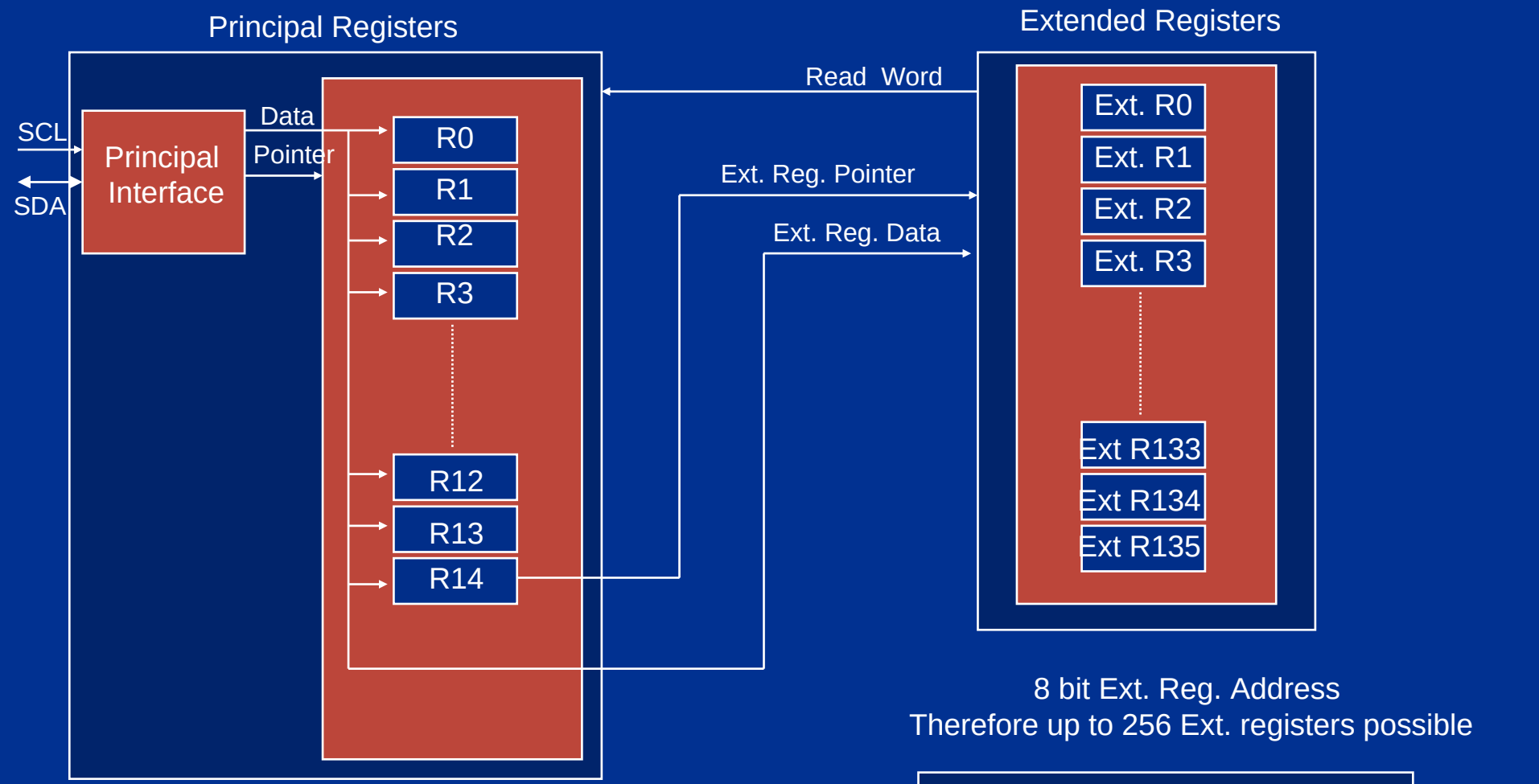
A unique 12 bit ChipID is laser blown during fabrication.

A 3 bit Chip Address is defined from outside by bonding.

Principal I²C Interface



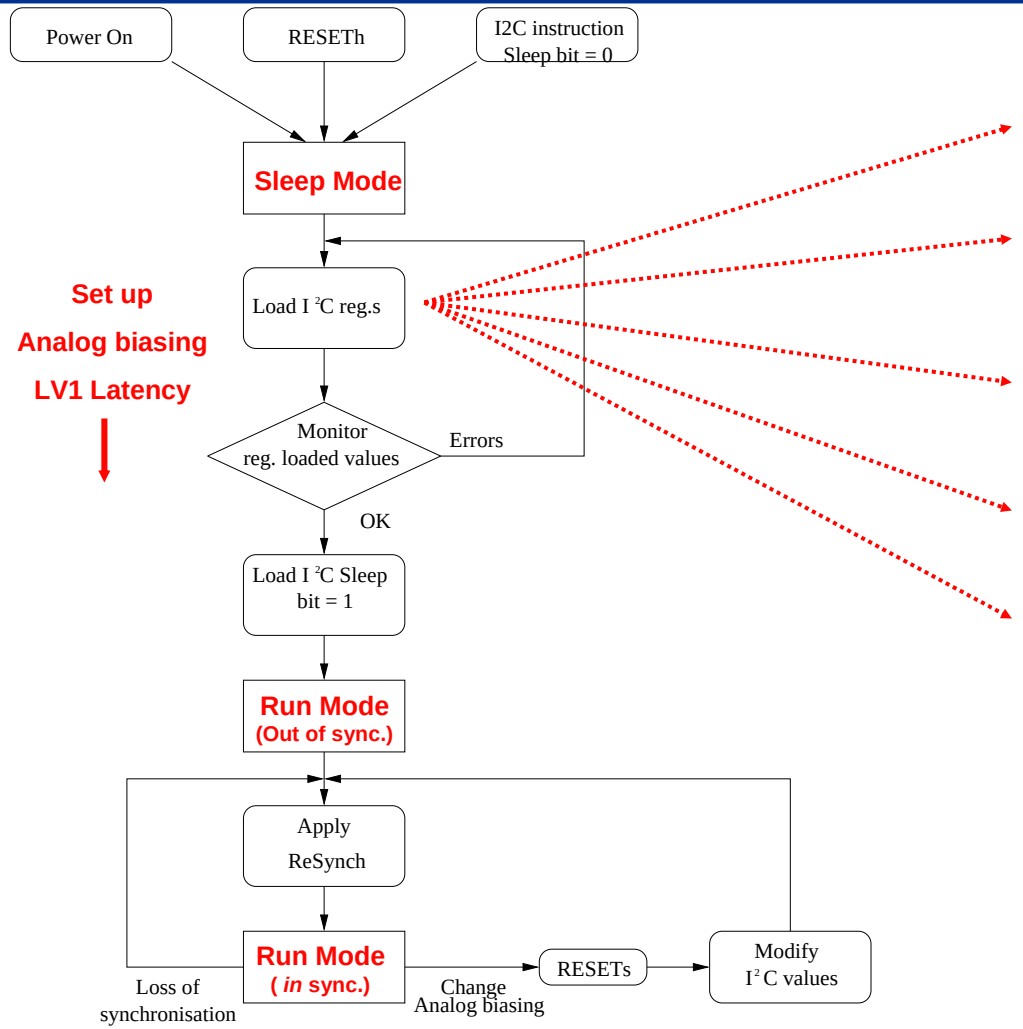
Extended Registers



8 bit Ext. Reg. Address
Therefore up to 256 Ext. registers possible

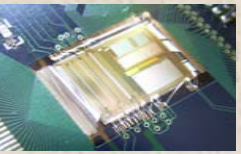
VFAT has 136 Extended Registers
CC has 8 Extended Registers

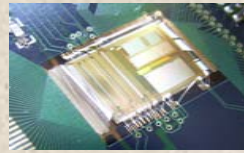
Programmability & Modes of Operation



- **Internal DAC calibration mode**
- **Channel calibration mode**
- **Lab Test mode**
- **Production Test - Read chip ID**
- **Scan chain mode**
- **SEU upset monitoring**
- **Occupancy monitoring**

VFAT2 I²C Control Panel





VFATDebugger - Beta Version

Control | Tests

Chip ID: 0xee73

Position

FEC: 0,0 | CCU: 0x7F | I²C Channel: 0x10 | Device: 0x10

Control Registers

	CalMode	CalPol	MSPol	TrigMode	Run
CR0 :	Normal	+ve	+ve	No Trig	Run
	ReHitCT	LVDSPowerSave	ProbeMode	DACsel	
CR1 :	6,4 µs	OFF	OFF	OFF	
	DigInSel	MSPulseLength	HitCountSel		
CR2 :	An I/P	1 clock	Fast OR		
	DFTestPattern	PbBG	TrimDAC-range		
CR3 :	OFF	OFF	0		

Biasing

IPreampIn	0	Latency	0
IPreampFeed	0	VCal	0
IPreampOut	0	VThreshold 1	0
IShaper	0	VThreshold 2	0
IShaperFeed	0	CalPhase	135 °
IComp	0		

Counters

Upset	0
HitCount 0	0
HitCount 1	0
HitCount 2	0

Read Counters

Channel Register #1

Cal 0 | Cal 1 | Mask | TrimDAC: 0

Other Channel Registers

CH #: 2 | Cal | Mask | TrimDAC: 0

Change this one | Change to all

Commands

Scan for FECs and CCUs

Initialize VFAT access

Chip

Read | Write

Compare written values

Select all registers

Select none

XML

File :

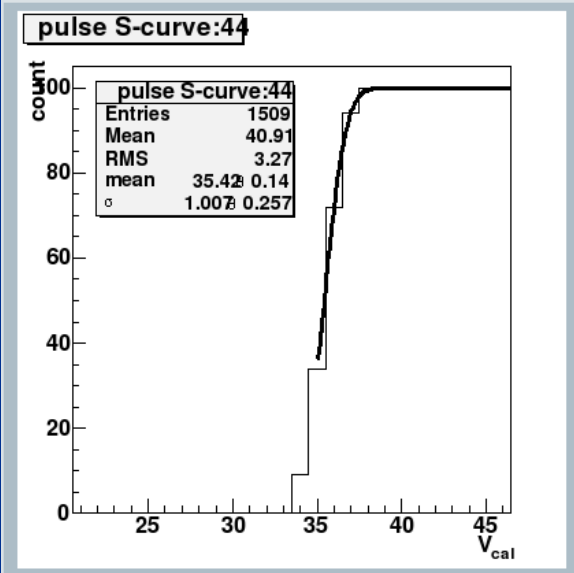
Load | Save

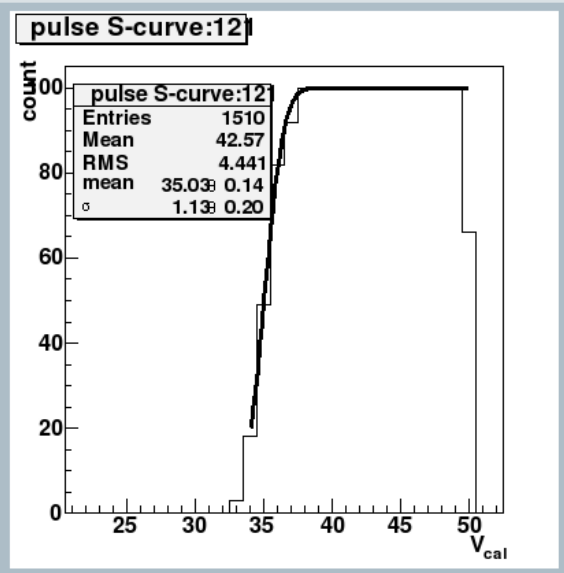
Show Array in Console

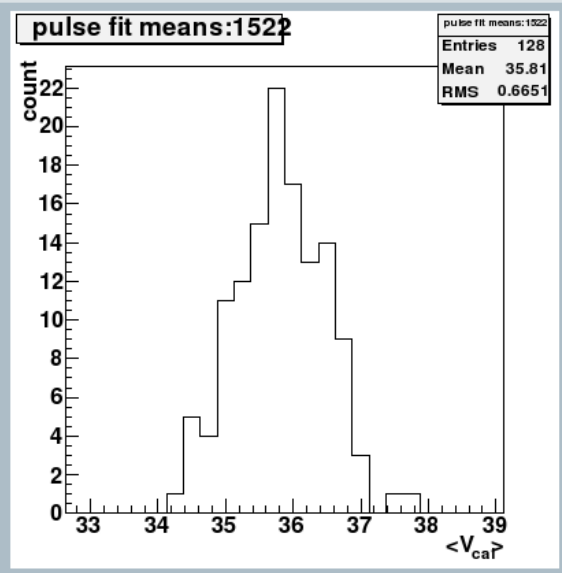
About | Quit

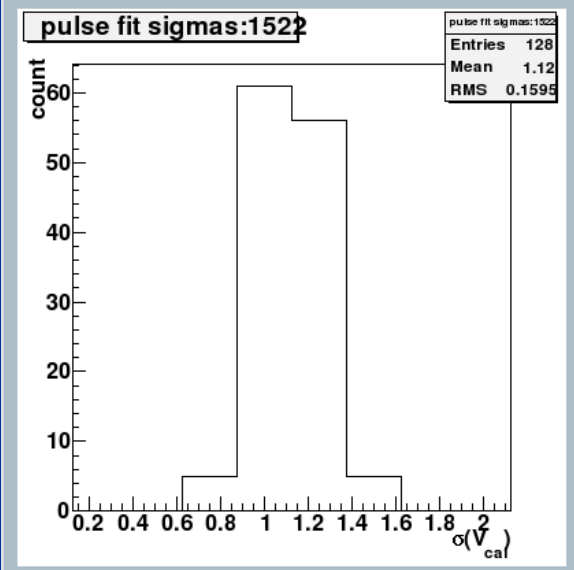
Software written by Juha Petaejaejaervi

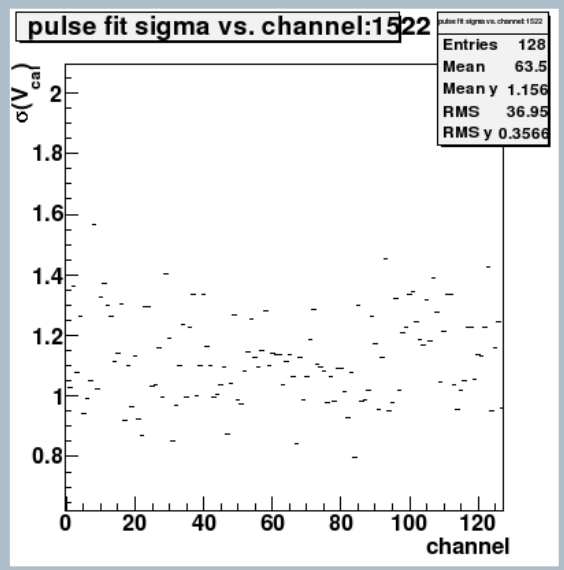
S-Curve on all channels

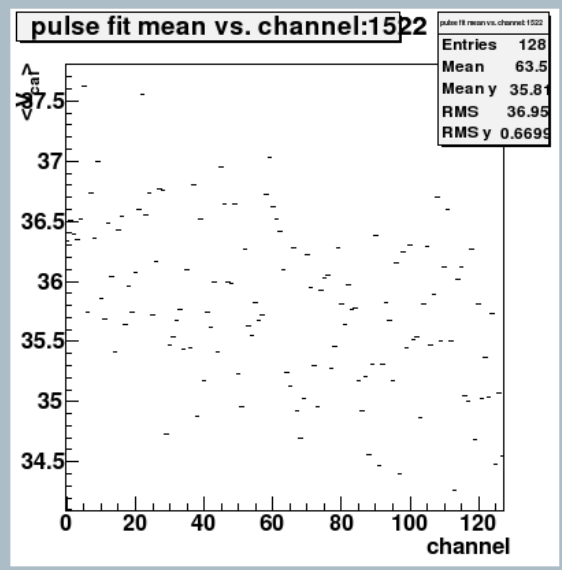












VFAT2 noise results with &without detector

Noise Results without detector

Noise over all 128 channels ……. <ENC> = 589 electrons rms, ENC spread (σ) = 14.26%

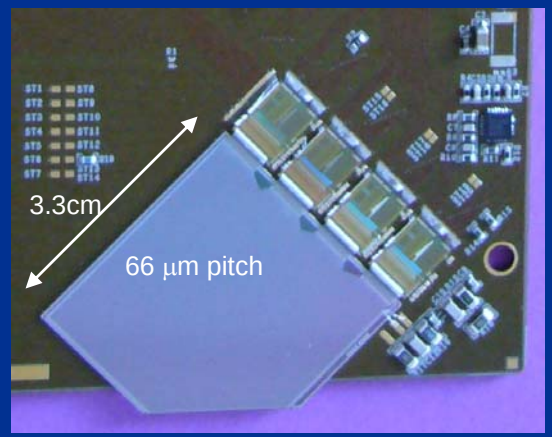
Threshold chosen = 5909 electrons (0.945 fC)

Threshold spread over 128 channels = 1.8% (without trimming DACs)

Min. Threshold = 0.7 fC (4375 e)

Max. Threshold = 18.7 fC (116875 e)

Noise Results with a silicon detector

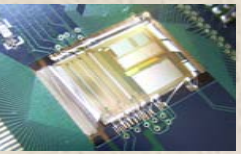


Noise over all 128 channels ….. <ENC> = 933 electrons rms, ENC spread (σ) = 9%

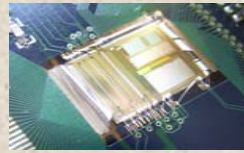
Threshold spread over 128 channels = 1.7% (without trimming DACs)

Noise increase of 344e

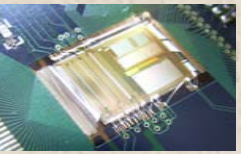
For 50 e/pF indicating additional capacitance < 7pF



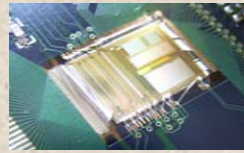
VFAT2 power consumption



POWER CONSUMPTION	Sleep Mode	Run Mode Nominal	Run Mode (max. activity)
Analog	33 mW	378 mW (2.95 mW/ch)	378 mW
Digital	135 mW	194 mW	237 mW
Total	168 mW	572 mW (4.47 mW/ch)	615 mW



VFAT2 Summary



VFAT2 : A Trigger and Tracking front-end detector readout ASIC has been designed, fabricated and tested.

Number of channels	128
Front-end shaping time	22 ns
ENC	~ 400 e + 50 e/pF
Linearity	± 12 fC
Internal Calibration test pulse	-2 fC to 18.5 fC, LSB = 0.08 fC with σ(LSB) = 0.3fC
Sampling frequency	40 MHz
LV1A Latency	Up to 6.4 us
Storage capacity	128 triggered events
Slow Control interface	I^2C
Testability features	Scan Chain, BIST, Probe pads, Auto test patterns, Auto Data Packet,
Power Consumption	168 mW (Sleep Mode) 572 mW (Run Mode)